# Characterizing the Linearity Sweet-Spot Evolution in FET Devices

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***Abstract*— In this paper, a complete characterization of the linearity sweet-spot evolution in MESFET/HEMT devices is presented. A global experimental extraction of the $I_{ds}$($V_{gs}$,$V_{ds}$) Taylor series coefficients is used to introduce the small-signal behavior in the linear and saturated regions. The possibility of taking advantage of these points in different applications is also discussed. For the first time, a characterization of the influence of both bias voltages on the device transition towards the large-signal regime is presented. Finally, a technique for improving the linearity-efficiency tradeoff in a class B/C power amplifier (PA) is introduced.**

## I. INTRODUCTION

Mobile communication systems impose a strong linearity-efficiency tradeoff to the PA stages. Thus, special interest has appeared on accurately controlling the intermodulation distortion (IMD) behavior of active devices, being reported the existence of low IMD points (linearity sweet-spots) either on small- [1], [2] or large-signal regimes [3], [4]. Most of these works have been based on a dedicated device nonlinear characterization through the experimental extraction of the $I_{ds}$($V_{gs}$,$V_{ds}$) derivatives, following procedures like the one proposed by Pedro and Pérez in [5].

Although the causes that determine this kind of optimum linearity performance in small- [1], [5], [6] and large-signal regime have been discussed [4], none reference provides a complete study of the IMD sweet-spot evolution with both control voltages, $V_{GS}$ and $V_{DS}$, when moving from small- to large signal operation.

In this paper, a complete description of the IMD evolution in FET devices is presented. A global experimental extraction of the $I_{ds}$($V_{gs}$, $V_{ds}$) Taylor-series coefficients for a typical FET is used to completely describe the small-signal IMD linearity sweet-spot behavior with the bias voltages. Then, the possibility of taking advantage of the optimum linearity points is discussed. Looking for extending the use of these points in power applications, an accurate characterization of the influence of both bias voltages on the device large-signal operation is presented. Finally, a technique for improving the linearity-efficiency tradeoff in a class B/C amplifier, to be used as output stage of a power control topology, is introduced.

## II. SMALL-SIGNAL OPERATION

In small-signal regime the main non-linearity of a FET device, the drain current source, may be approximated by the following two-dimensional Taylor series

$$\begin{aligned} I_{ds} = {} & I_{DS}(V_{GS},V_{DS}) + G_m v_{gs} + G_{ds} v_{ds} + G_{m2} v_{gs}^2 \\ & + G_{md} v_{gs} v_{ds} + G_{d2} v_{ds} + G_{m3} v_{gs}^3 + G_{m2d} v_{gs}^2 v_{ds} \\ & + G_{md2} v_{gs} v_{ds}^2 + G_{d3} v_{ds}^3 + \cdots \end{aligned} \quad (1)$$

where $I_{DS}$($V_{GS}$,$V_{DS}$) is the DC component. The remaining terms represent the dynamic component of the drain current, $i_{ds}$, as a function of the dynamic gate-source, $v_{gs}$ and drain-source $v_{ds}$ voltages. In this $I_{ds}$ representation, the $i_{ds}$ series coefficients are related with the drain current derivatives as follow

$$\begin{aligned} G_m &\approx \frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{GS},V_{DS}} & G_{ds} &\approx \frac{\partial I_{ds}}{\partial V_{ds}}\Big|_{V_{GS},V_{DS}} \\ G_{m2} &\approx \frac{1}{2!}\frac{\partial^2 I_{ds}}{\partial {V_{gs}}^2}\Big|_{V_{GS},V_{DS}} & G_{md} &\approx \frac{\partial^2 I_{ds}}{\partial V_{gs}\partial V_{ds}}\Big|_{V_{GS},V_{DS}} \\ G_{d2} &\approx \frac{1}{2!}\frac{\partial^2 I_{ds}}{\partial {V_{ds}}^2}\Big|_{V_{GS},V_{DS}} & G_{m3} &\approx \frac{1}{3!}\frac{\partial^3 I_{ds}}{\partial {V_{gs}}^3}\Big|_{V_{GS},V_{DS}} \\ G_{m2d} &\approx \frac{1}{2!}\frac{\partial^3 I_{ds}}{\partial {V_{gs}}^2 \partial V_{ds}}\Big|_{V_{GS},V_{DS}} & G_{md2} &\approx \frac{1}{2!}\frac{\partial^3 I_{ds}}{\partial V_{gs} \partial {V_{ds}}^2}\Big|_{V_{GS},V_{DS}} \\ G_{d3} &\approx \frac{1}{3!}\frac{\partial^3 I_{ds}}{\partial {V_{ds}}^3}\Big|_{V_{GS},V_{DS}} \end{aligned} \quad (2)$$

In order to get a direct relation between the dynamic drain current and the input signal ($v_i$), a representation as a nonlinear transfer characteristic (3) would be preferred rather than (1).

$$i_{ds} = G_1 v_i + G_2 v_i^2 + G_3 v_i^3 + \cdots \quad (3)$$

Using the non-linear current source approach of the Volterra series analysis, the coefficients $G_{p=1,2,3,..}$ can be computed as functions of the drain current derivatives. For a common source amplifier, these are given by

$$G_1 = \frac{G_m}{\Delta} \quad (4)$$

$$G_2 = \frac{1}{\Delta}\begin{bmatrix} {k_{gs}}^2 & k_{gs}k_{ds} & {k_{ds}}^2 \end{bmatrix}\begin{bmatrix} G_{m2} \\ G_{md} \\ G_{d2} \end{bmatrix} \quad (5)$$

$$\begin{aligned} G_3 = {} & \frac{\begin{bmatrix} 2k_{gs}k_{gs}^{(2)} & k_{gs}k_{ds}^{(2)} + k_{gs}^{(2)}k_{ds} & 2k_{ds}k_{ds}^{(2)} \end{bmatrix}}{\Delta}\begin{bmatrix} G_{m2} \\ G_{md} \\ G_{d2} \end{bmatrix} \\ & + \frac{\begin{bmatrix} {k_{gs}}^3 & {k_{gs}}^2 k_{ds} & k_{gs}{k_{ds}}^2 & {k_{ds}}^3 \end{bmatrix}}{\Delta}\begin{bmatrix} G_{m3} \\ G_{m2d} \\ G_{md2} \\ G_{d3} \end{bmatrix} \end{aligned} \quad (6)$$

$$\Delta = 1 + G_m R_S + G_{ds}\left(R_L + R_D + R_S\right) \tag{7}$$

where $R_L$, $R_D$, and $R_S$ are the load, drain, and source resistances. The coefficients $k_{gs}$ and $k_{ds}$ are the ratio between the first order component of the control voltages, $v_{gs}^{(1)}$ and $v_{ds}^{(1)}$, and the input signal $v_i$ from the linear equivalent circuit. The other coefficients ($k_{gs}^{(2)}$, $k_{ds}^{(2)}$) are computed from de second order equivalent circuit as the relation between the second order control voltage, $v_{gs}^{(2)}$ and $v_{ds}^{(2)}$, and the squared input ($v_i{}^2$). In this way, the linear components of $i_{ds}$ are proportional to $G_1$, while the second and third order non-linear ones depend on $G_2$ and $G_3$ respectively.

Considering this model, for a two-tone input signal, $v_i = V_i(cos(2\pi f_1 t) + cos(2\pi f_2 t))$, the power of the in-band third order intermodulation distortion products (IM3) is given by

$$\begin{aligned} P_{IM3}(f_1, f_2) &= \frac{1}{2} R_L \left| i_{ds}^{(3)}(f_1, f_2) \right|^2 \\ &= \frac{1}{2} R_L \left( \frac{9}{4} G_3 V_i^3 \right)^2 \end{aligned} \tag{8}$$

$$\begin{aligned} P_{IM3}(2f_1 - f_2, 2f_2 - f_1) &= \frac{1}{2} R_L \left| i_{ds}^{(3)}(2f_1 - f_2, 2f_2 - f_1) \right|^2 \\ &= \frac{1}{2} R_L \left( \frac{3}{4} G_3 V_i^3 \right)^2 \end{aligned} \tag{9}$$

As it could be expected, the local minima of the in-band IM3 distortion products are exactly at the zeros of $G_3$. The pairs ($V_{GS}$, $V_{DS}$) at which the minima appear are the so called small-signal intermodulation distortion sweet-spot (SS-IMDSS). As a practical approach the SS-IMDSS used to be approximated to the $G_{m3}$ zeros [6]; although these points are actually slightly shifted to the right from the SS-IMDSS position, it is a good practice since the $G_{m3}$ zeros are at the inflexion points of the transconductance, $G_m$, which is a more familiar parameter for the designers.

To introduce the sweet-spot evolution, the drain current derivatives of a HEMT transistor from NEC (NEC3210s01) were extracted, following the procedure proposed in [5], and used to compute the coefficients of the $i_{ds}$ power series given by (3).

In Fig. 1, the SS-IMDSS evolution for this transistor is plotted. Two zones of low in-band intermodulation distortion are perfectly defined. The *First SS-IMDSS* curve defines the $V_{GS}$ pinch-off voltage, its position is approximately constant, although it actually follows the widely known $V_{DS}$ pinch-off modulation equation: $V_p \approx V_{po} + \gamma V_{DS}$.

The *Second SS-IMDSS* curve has a behavior that can be perfectly divided in two zones, corresponding to the linear and saturated operating conditions. In the linear region, it can be roughly related with the $V_{GD} \approx V_{po} + \gamma V_{DS}$ curve, while in saturation follows approximately a constant $V_{gs}$ value.

Considering the sign of $G_3$, the SS-IMDSS curves divide the $V_{GS}$-$V_{DS}$ plane in three zones. These zones, as will be seen, determine where the large-signal sweet-spot appears.

### A. Gain and efficiency performance

Along the *First SS-IMDSS*, the transconductance presents low values and exhibits only a little variation. Due to these characteristics, the *First SS-IMDSS* loses interest for developing highly-linear small-signal amplifier applications.

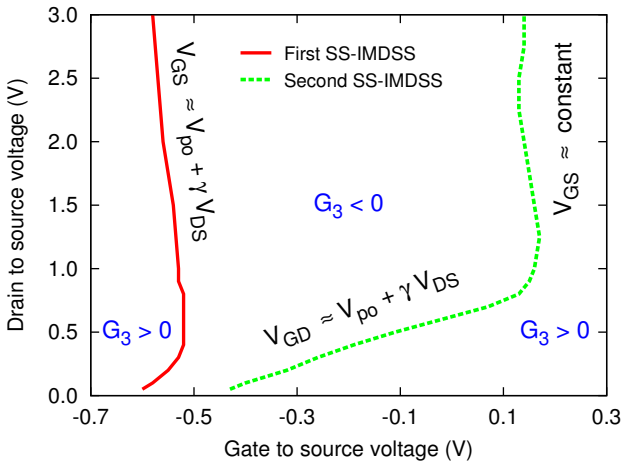


Fig. 1. SS-IMDSS locus for a 50Ω load condition.

Following the $V_{GD} \approx V_{po} + \gamma V_{DS}$ *Second SS-IMDSS* curve, the transconductance has a gradual variation associated both to low DC power consumption and low bias voltage. At higher $V_{GS}$ voltage values, where the drain current is high, the DC power consumption is similar to that obtained for the transistor working in the saturation region at the same gain level. However, for those points where the gate voltage is low enough, such that the power consumption is equal or lower than that of the transistor working in saturation, a good control range could be reached. These features make this zone attractive for implementing a highly linear and low voltage gain control strategy, as it was suggested by the authors in [7].

Along the constant $V_{GS}$ curve, the transconductance value is relatively high and approximately constant. This makes this zone useful for improving the linearity of class A small-signal amplifiers, particularly for those based in MESFET devices where the second zero appears at the flat region of its transconductance versus gate voltage characteristic.

## III. Large-Signal Operation

Although the existence of large-signal intermodulation distortion sweet-spots (LS-IMDSS) had been reported for FET devices many years ago [3], its behavior was not clearly addressed. In a recent paper, Carvalho and Pedro [4] determined that one LS-IMDSS appears when the gate terminal is biased below the $V_{GS}$ pinch-off voltage, corresponding this region with the low current knee of the $i_{ds}$ versus $v_i$ transfer characteristic. The other LS-IMDSS appears when the transistor is biased in the triode region, at the high current knee of the transfer characteristic. Thus, two LS-IMDSS zones are perfectly defined, which agreed with the region where $G_3$ is positive in the $V_{DS}$ versus $V_{GS}$ plane, see Fig. 1.

Even though the bias conditions that determine the apparition of a LS-IMDSS have been established, none reference about its evolution with both control voltages has been found. Thus a characterization is necessary in order to use efficiently these optimum linearity points.

Using the same HEMT device, the behavior of the first and second IMDSS regions were characterized when increasing the input power level out of the small-signal operation.

In Fig. 2, the sweet-spot loci are represented under a 50Ω load condition for different $V_{DS}$ values. As can be easily appreciated, two power level zones may be differentiated. For

low power values, the sweet-spot positions stay at the values defined in Fig. 1, corresponding to the operation in small-signal regime. However, for higher input power values, when the transistor gets into the large-signal regime, the influence of the power level becomes strong. Thus, the *Second SS-IMDSS* evolves towards higher $V_{GS}$ values, approaching the region of gate conduction. Since the operation under this condition could really affect the reliability of the device, this region seems to lose interest for high power amplifier applications.

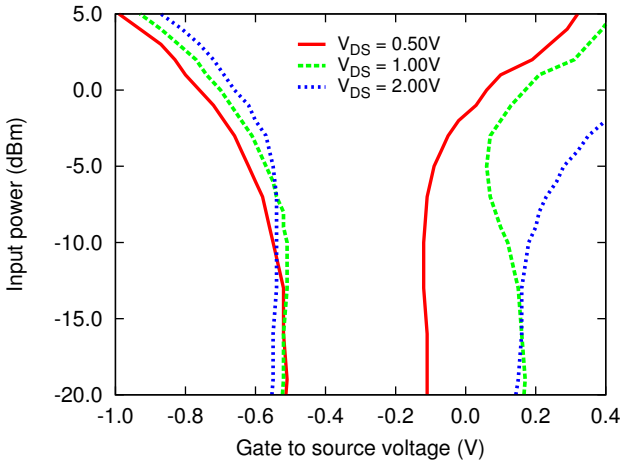


Fig. 2. IMD sweet-spot evolution from small- to large signal regime.

On the other side, the *First SS-IMDSS* moves into the operating conditions of the high efficiency amplifiers (classes B and C), and will be studied in detail for a power device.

### A. Device performance in the LS-IMDSS region

In Fig. 3, the trajectory of the first sweet-spot is plotted together with the constant gain loci for a power MESFET from Fujitsu (FLL177ME). The constant gain loci were measured adjusting the gate voltage to fix 6dB gain at each input power level, for a given $V_{DS}$ voltage.

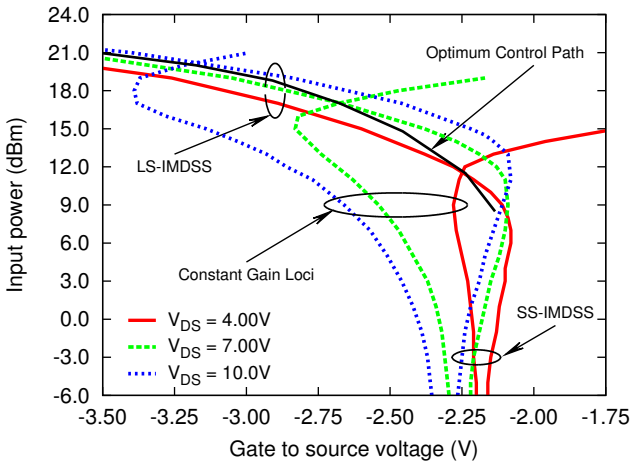


Fig. 3. IMDSS and 6dB constant gain loci for the FLL177ME.

From this figure, the following conclusions may be remarked:

1) For a given $V_{GS}$ value, the $V_{DS}$ voltage controls the power level at which the LS-IMDSS appears and vice versa.
2) For a fixed input power level, it is possible to control the output power level adjusting the drain voltage. In this case, an additional adjustment of $V_{GS}$, along the new $V_{DS}$ sweet-spot locus, must be done in order to assure the high linearity performance.
3) For a given bias condition in the LS-IMDSS region, the gain locus is intercepted at two different input powers. This means that the LS-IMDSS are associated with a gain expansion phenomenon.
4) Under input power level variation, the set of points resulting from the interception between the LS-IMDSS locus and the corresponding constant gain one, define an optimum high linearity control path.
5) The LS-IMDSS appear in a region with associated low DC current value (typical of the pinch-off condition), which guarantee the drain efficiency.

## IV. Improving The Linearity-Efficiency Tradeoff In Power Control Applications

The conclusions of the last section suggested us the idea of implementing a class B/C amplifier with improved linearity-efficiency tradeoff to be used as the output stage of a power control strategy, something interesting for modern wireless communication standards.

This kind of envelope tracking amplifier [8] would be able of adapting the bias voltages to the long-time RMS values of the input signal envelope (the average input power level) following the $V_{GS}$ intersection points between the LS-IMDSS and gain loci at different $V_{DS}$ values. For this approach, the previously characterized power MESFET was considered in a 900MHz band amplifier design. This amplifier was tested under a two-tone and an IS-95 QPSK input signal.

The nominal value of the output power would correspond to the intersection point of the curves at the highest $V_{DS}$ value ($V_{DS} = 12.0$V, $V_{GS} = -3.50$V, $P_{out} = 24.83$dBm at a 6dB gain level, for the two tone case). In order to keep a high efficiency when the average input power is reduced, the drain-to-source voltage is diminished up to the value where a $V_{GS}$ optimum point could be assured for the new input power level. Thus, the maximum control range (about 15dB) would be limited by the lowest $V_{DS}$ where an intersection between the LS-IMDSS and gain loci exists ($V_{DS} = 3.00$V, $V_{GS} = -2.13$V, $P_{out} = 11.83$dBm). The optimum control path for the two-tone input signal is shown in Fig. 3. For the IS-95 QPSK signal, the optimum control path resulted slightly shifted to the left and down in the $V_{GS}$-input power plane.

In Fig. 4, the control strategy is illustrated. The lines represent the Pin-Pout characteristic for a fixed bias condition (LS-IMDSS bias condition), while the dots remark how the desired output and the IM3 components evolve at four points in the optimum control path.

As can be easily appreciated, the desired component follows a linear relation with the input signal (1dB/dB), even tough the bias point is moving from one LS-IMDSS to another. This solves one of the problems presented in some efficiency improving techniques, like the envelope tracking [8], where the single or dual bias adjustment required to control the power consumption, produces a gain variation. At the same time, the efficiency is kept near the highest values obtained for the fixed bias condition, see Fig. 5.

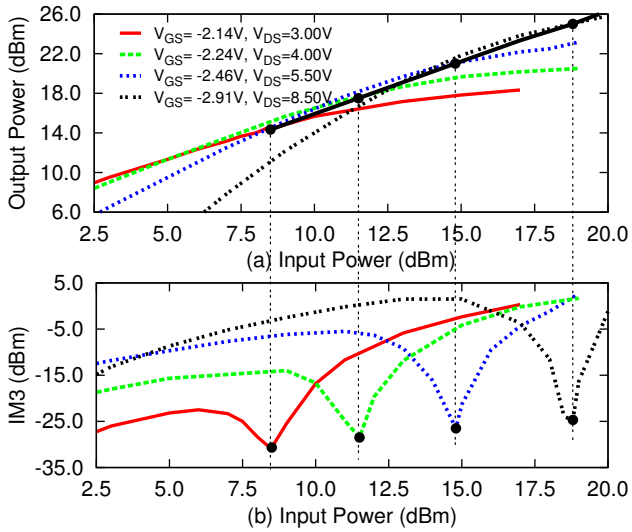


Fig. 4. Pin-Pout characteristic for the two-tone experiment. a) Desired output and b) Third order IMD component.

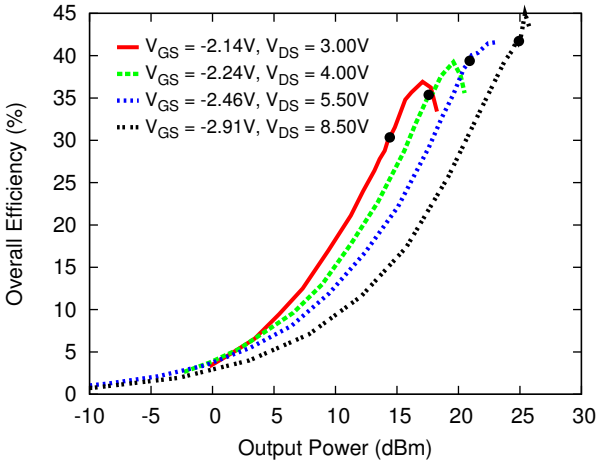


Fig. 5. Overall efficiency at a fixed bias condition, lines, and following the optimum control path, dots.

In table I, the experimental results are summarized for different input/output power levels. The C/I and ACPR were measured for the adjacent channel with the highest power level in any case (worst case). For the two-tone test, it can be remarked that the C/I value is kept over 31.16dB even at the highest power level, while the efficiency stays over 30.34%.

For the IS-95 QPSK signal, the ACPR values were computed as the ratio of the power over a 30KHz bandwidth in the adjacent channel to the power in the desired channel bandwidth. As it can be expected, the efficiency values are reduced for this complex input signal. In any case, they stay over a 14.31%, while the ACPR was always better than -45.97dB. In Fig. 6, the output spectrum for the IS-95 QPSK signal at three different output power levels is shown along the proposed control path.

## V. Conclusion

A complete characterization of the IMD small- and large-signal sweet-spots has been presented for FET devices. The device behavior in the two optimum linearity regions was described, paying particular attention to the gain and DC current consumption. For the small-signal operation, the second region presents good potentialities for its use in variable gain and class A amplifiers, with improved linearity. In large-signal regime, the sweet-spot bias control with both bias voltages has been presented for the first time, and a strategy for improving the linearity-efficiency tradeoff of a class B/C amplifier has been suggested.

TABLE I

Efficiency Improved Power Control Application

| Two-Tone | | | IS-95 QPSK | | |
|---|---|---|---|---|---|
| $P_{out}$ (dBm) | $C/I$ (dB) | $\eta$ (%) | $P_{out}$ (dBm) | $ACPR$ (dB) | $\eta$ (%) |
| 11.33 | 42.00 | 30.34 | 11.33 | -53.11 | 14.31 |
| 18.00 | 44.50 | 39.39 | 17.30 | -48.77 | 18.11 |
| 20.17 | 47.00 | 41.84 | 20.09 | -47.23 | 20.23 |
| 22.00 | 46.67 | 41.73 | 21.63 | -47.04 | 20.09 |
| 23.33 | 38.83 | 42.38 | 23.36 | -46.53 | 21.27 |
| 24.83 | 31.16 | 40.24 | 25.16 | -45.97 | 21.77 |

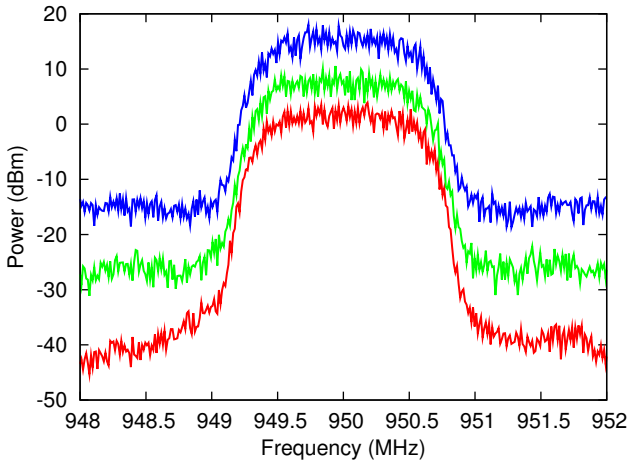


Fig. 6. Output Spectrum for the IS-95 QPSK signal at three different output power levels ($11.13dBm, 20.09dBm, 25.16dBm$).


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