Distributed Amplifiers for Transmitter and Receiver of a 40 Gbit/s DPSK Optical Transmission System

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***Abstract* - For a 40 Gbit/s DPSK optical transmission system, two circuits are reported. The first circuit is a high frequency, high power modulator driver based on a twin traveling wave amplifier (combiner) with an active power divider circuit and measured output voltages greater than 7 V_{pp}. A second circuit consisting of a differential preamplifier and TWA main stages is presented with concept and simulation results.**

I. INTRODUCTION

Even in recent years of economic turbulences the needs for higher speed, capacity and bandwidth of wireless and optical fiber systems have continuously increased. Pushing the limits of optic fields further leads to the introduction of new modulation schemes, such as Differential Phase Shift Keying (DPSK) which has considerable advantages (3 dB less signal-to-noise ratio needed) compared to the conventional Amplitude Shift Keying (ASK). This means that substantially larger transmission distances can be achieved with unchanged optical amplifier spacing, and DPSK has hence emerged as a strong candidate for modulating 40 Gbit/s signals.

In order to implement the next generation of optical transmission systems, special high speed ICs are required.

In this paper we present two circuits that could be employed as electronic modulator driver and front-end in a DPSK transmission system [1].

II. MODULATOR DRIVER

Fig. 1 shows a practical 40 Gbit/s transmission system based on DPSK modulation. A Mach-Zehnder modulator (MZM) is used because it guarantees a better chromatic dispersion tolerance than the simple phase modulator. The Mach-Zehnder modulator driver is a critical component with its high gain and output voltages. Its role is to amplify the 40 Gbit/s multiplexed signal to an output voltage of 6 V_{pp}.

The bit error rate as the final optimization goal strongly depends on the modulator driver. A high modulator driver bandwidth for a good transmitted signal form with a low differential group delay is required.

Concept and simulation results of a 40 Gbit/s 7 V_{pp} modulator driver based a on source follower type active divider and two combined traveling wave amplifiers (TWAs) have been proposed in [2].

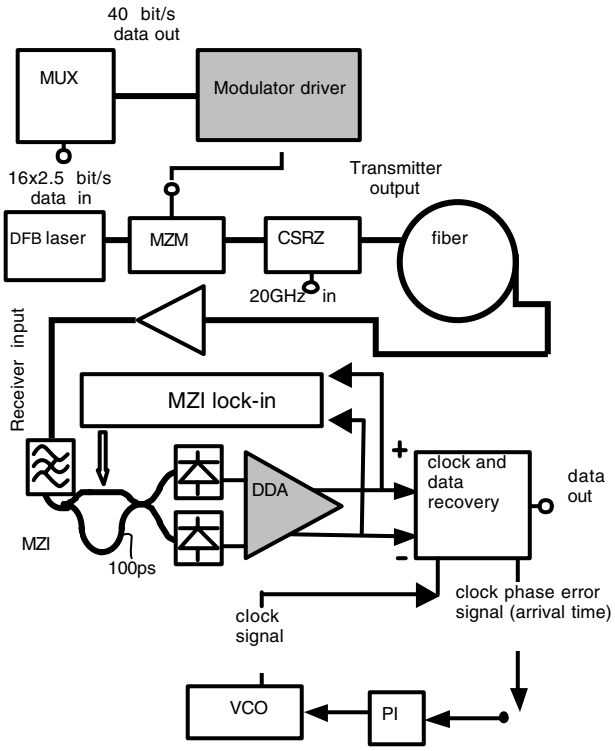

Fig. 1. Modulation scheme of a practical 40Gbit/s DPSK transmission system

The circuit has now been fabricated (Fig. 2) using the OMMIC D01PH process, a pseudomorphic AlGaAs / InGaAs HEMT technology with 0.13 mm mushroom gate length and 105 GHz transit frequency. The drain breakdown voltage is -11 V and DFET characteristics allow operation with unbiased input signal.

The input signal is fed into an active power divider circuit consisting of two source follower stages for each branch. The two signals are then used as input signals for two identical traveling wave amplifiers sharing a common drain line on which their output power is combined. The additional capacitive loading of this common drain line causes a lower phase velocity and thus enables a design

with similar length of the gate and the drain line between two stages. Therefore, a simple layout without meander

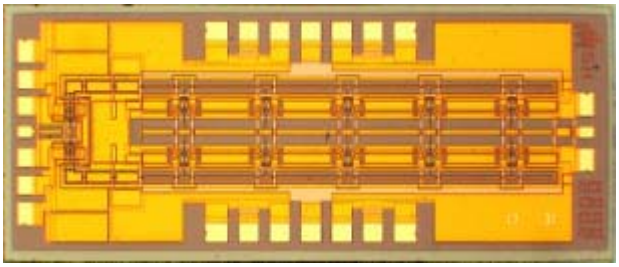

Fig. 2. Chip micrograph of the modulator driver (3mmx1mm)

lines was possible. Each half of the combiner consists of 5 stages in coplanar wave-guide technology. A single stage contains a pair of two finger HEMTs in a cascode configuration with a gate width of 30 µm, designed as a single cell in order to save space and reduce parasitics.

A drain bias voltage of 6 V is applied through an external bias tee. This voltage is also used on chip for the drain line termination resistor, avoiding the DC losses that would result from termination to ground.

Simulation and Measurement results

The S-parameter measurements have shown a good match to simulated curves. Fig. 3 shows the magnitude of S_{21} for two typical chips in comparison to the simulation and re-simulation. A power gain of more than 16 dB was achieved with a 3 dB frequency of 35 GHz.

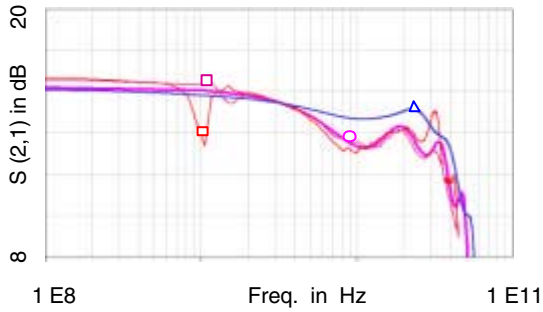

Fig. 3: Comparison of simulated (Δ) , measured (□), (□), and re-simulated (○) data for the magnitude of S_{21}

Figs. 4 and Fig. 5 show the magnitudes of S_{22} and S_{11}, again with a comparison of the simulated, measured and re-simulated curves. The output reflection coefficient S_{22} is below –5 dB up to 45 GHz. Neither in simulation nor in measurement, stability problems occurred.

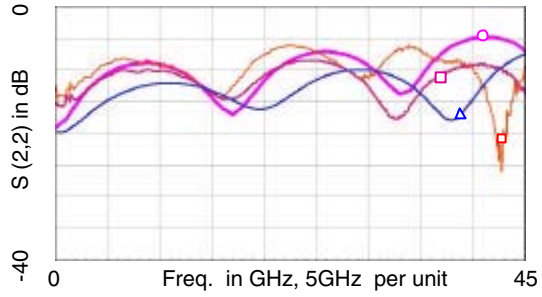

Fig. 4: Comparison of simulated (Δ), measured (□), (□), and re-simulated (○) data for the magnitude S_{22}

In general, the very small magnitudes differ slightly, and the frequency dependence is modeled quite well in the re-simulation. The re-simulation obtained a slightly improved match by additional 10 fF capacitors in each coplanar T-junction and 50 fF in parallel to the drain line termination resistor.

Time domain measurements could only confirm indirectly a good match to the simulation since the

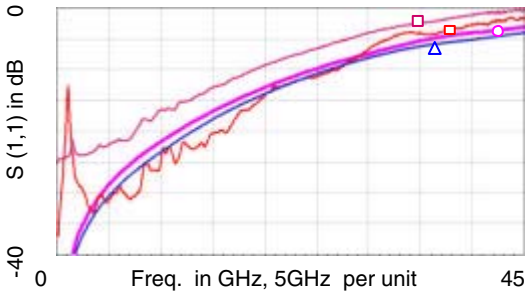

Fig. 5: Comparison of simulated (Δ) , measured (□), (□), and re-simulated (○) data for the magnitude of S_{11}

influence of the test set-up cannot be calibrated here. Actually it has an accumulated f_{3dB} corner below 8 GHz although each of in total 9 K-components is specified up to 40 GHz. For an input voltage at the limit defined by the Schottky diodes, i.e. approximately 1.5 V_{pp}, a maximum output voltage well above 7 V_{pp} results (Fig. 6). The power consumption of the amplifier was 2.7 W.

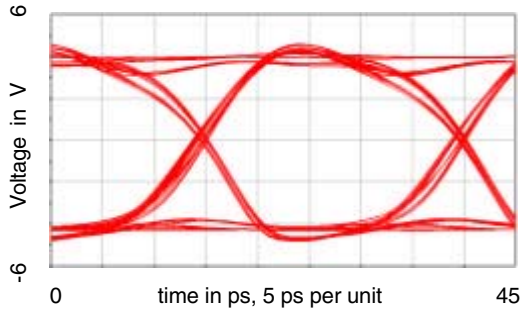

Fig. 6: Simulated eye diagrams at 1.5 V_{PP} input voltage

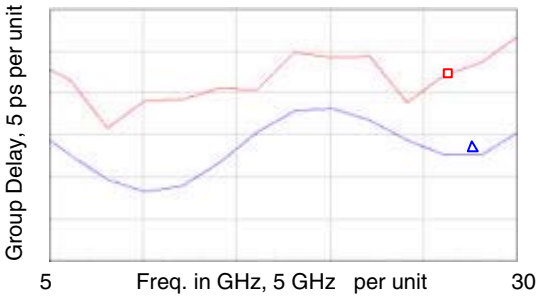

Fig. 7: Comparison of simulated (Δ) , measured (□), data for the group delay

Good match between the simulated and measured group delay spread was also achieved (Fig. 7).

III. Differential Distributed Amplifier

On the receiver side a low noise high-speed circuit is required for the amplification of the 40Gbit/s photodiode output signals.

In the DPSK transmission scheme (Fig. 1), the differential interferometer outputs are connected to two photodiodes. The signal should be demultiplexed in a clock-and-data recovery with differential input. Since amplification of the differential photodiode output signals is required and the following demultiplexer also needs a differential input signal, the simplest solution would be to employ a differential amplifier for that purpose. Our approach combines the advantages of a differential design with its noise suppression capability and a distributed amplifier with its flat gain and good terminal match.

The Differential Distributed Amplifier (DDA) consists of a differential preamplifier circuit with two differential outputs, each driving the gate line of a TWA with four stages (Fig. 8).

The differential preamplifier has a simulated CMRR better than 16.5 dB up to 40 GHz .

The maximum number of TWA stages is limited by the gate line losses.

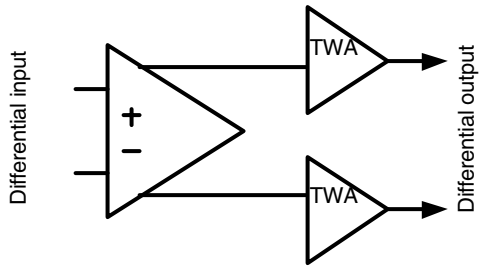

Fig. 8: Block diagram of the differential distributed amplifier

Similar to the modulator driver circuit, a TWA stage consists of two HEMTs (40 µm gate width) in a cascode cell. The main drawback of the cascode cell is caused by resonance in S_{22} of the amplifier, which may lead to stability problems.

In simulations, this circuit turned out to be less stable than the modulator driver circuit. Inserting a series-damping resistor at the gate of the common-gate transistor solves this problem. Simulation results confirm that the DDA is unconditionally stable – both stability factors k and µ are > 1 (Fig. 9).

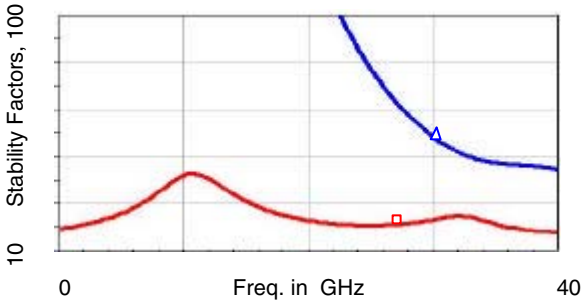

Fig. 9: Stability factors k (Δ) and µ (□)

The simulated output reflection coefficient S_{22} is below −15 dB up to 40 GHz. (Fig.10).

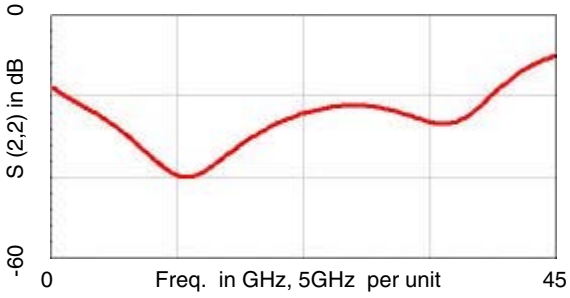

Fig.10: Simulated DDA data for the magnitude S_{22}

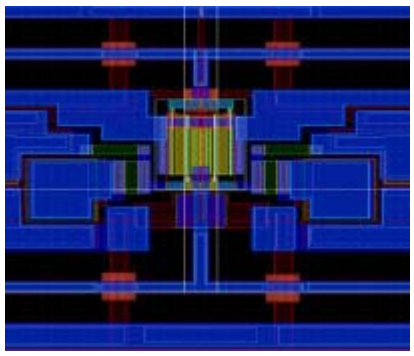

Fig. 11: Layout detail for the new cascode cell

The employed CPW lines are calculated to have 65 Ω characteristic impedance. Simulated drain and gate line lengths for optimum gain in respect of bandwidth are 200 µm and 150 µm, what is not feasible in the layout. As an alternative to a longer drain line, a small capacitor was used to slow down the signal. Therefore, a capacitor of 0.03 pF is integrated in the T-junction of the drain line (Fig.11).

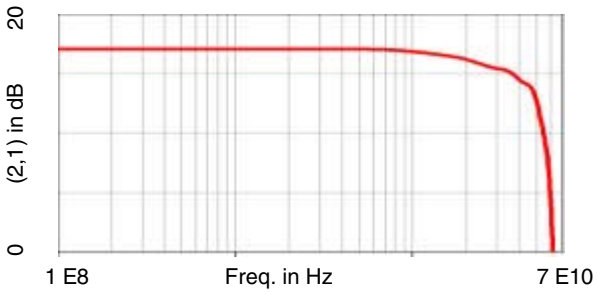

Fig. 12: Simulated forward transmission for DDA

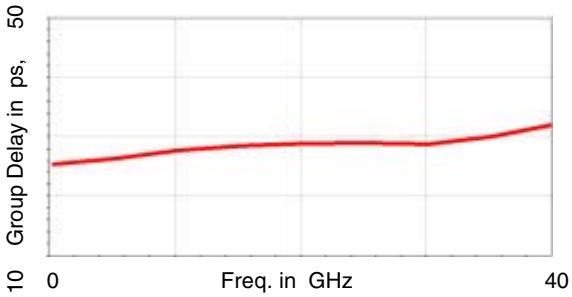

Fig.13: Simulated group delay for DDA

Figs. 12 and 13 show the forward transmission of the differential distributed amplifier and simulated group delay, respectively. The gain at 40 GHz is 15 dB and the f_{-3dB} bandwidth is 46 GHz.

The simulated eye diagram (Fig. 14) has a 0.7 V_{PP} output amplitude for 0.15 V_{PP} of input voltage.

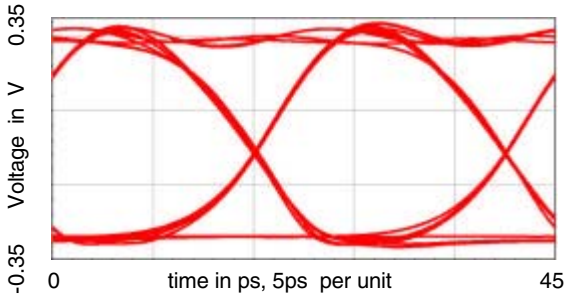

Fig. 14: Simulated eye diagram at 0.15 V_{PP} input voltage

The 3mm x 1mm DDA layout is realized to fulfil the important high-frequency circuit design goal - a total layout symmetry (Fig.15).

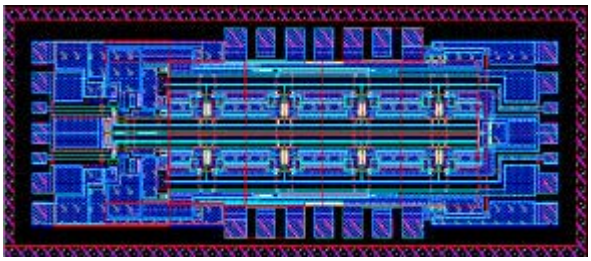

Fig. 15: Realized layout for DDA

VI. CONCLUSION

Output voltages above 7 V_{pp} at 40 Gbit/s could be experimentally obtained by a combiner circuit based on two TWAs sharing a common drain line with input signals from an active divider based on source followers on the same chip. Simulation results for a differential TWA in the same technology indicate 15 dB gain up to 46 GHz with 16.5 dB of CMMR.

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