Integration of components in a 50 nm InGaAs-InAlAs-InP HEMT process with pseudomorphic $In_{0.65}Ga_{0.35}As$ channel

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***Abstract* — The basic active and passive elements for a 50 nm InGaAs-InAlAs-InP HEMT process with pseudomorphic InGaAs channel have been realized. The design and fabrication of 50 nm gate length InP HEMTs, MIM capacitors and thin film resistors have been studied. The integration of the components in a microstrip-based MMIC process has been proven by the successful demonstration of a wideband amplifier.**

I. Introduction

The highest performance mm-wave systems are based on InP HEMT MMIC technology [1]. The most advanced commercial InP HEMT processes are now qualified for 70 nm gate length [2]. However, details in the issues of component design and integration for deep sub-100 nm InP HEMT MMIC are rarely reported in the literature. We here report design and realization of 50 nm HEMTs, MIM capacitors and thin film resistors (TFRs) in an InGaAs-InAlAs-InP HEMT process. The MMIC integration is validated by the successful demonstration of a wideband amplifier.

II. Design and realization of MMIC Components

A. 50 nm InP HEMTs

The epitaxial structure, grown by MBE on semi-insulating InP bulk, consisted of an InAlAs buffer, a 150 Å thick strained $In_{0.65}Ga_{0.35}As$ channel, a strained InAlAs spacer layer, a Si doping plane, a strained InAlAs Schottky layer, and an n^+ InGaAs cap layer. Hall measurements revealed a 2D electron gas sheet density of 2.72×10^{12} cm^{-2} and a room temperature mobility of 10,100 $cm^2V^{-1}s^{-1}$. More information on the epitaxial structure can be found in [3].

Two- and four-finger 50 nm devices with widths ranging from 30 to 200 µm were fabricated by a combination of optical and electron beam lithography techniques. After mesa isolation, source and drain ohmic contacts with 2 µm spacing were defined by a lift-off procedure and subsequently annealed. The mushroom-shaped gates were defined in a two-layer resist system using a single exposure in a 100 kV JEOL JBX9300FS electron beam lithography system. The gate recess etch was performed using a selective citric acid hydrogen peroxide solution. Titanium, platinum, and gold were

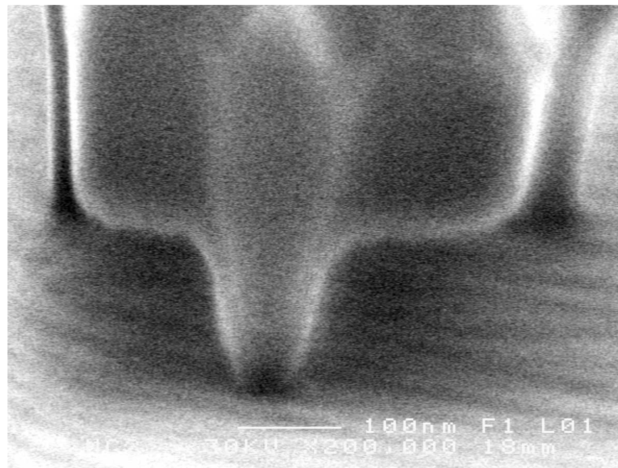

Fig. 1 SEM micrograph of a 50 nm InP HEMT gate.

evaporated to form the gate electrodes (Fig. 1). The devices were passivated by a 700 Å thick reactively sputtered silicon nitride layer. Openings for transistor pads were formed by a reactive dry etch using NF_3. Gold was grown by electro-plating on the transistor pads and air bridges for source interconnections were formed.

The DC current-voltage characteristics of (unpassivated) HEMTs were measured on-wafer. I-V and g_m curves are shown in Figs. 2 and 3, respectively. The devices showed good pinch-off characteristics. A 2x15 µm HEMT showed an extrinsic peak transconductance of 1130 mS/mm at a drain-source voltage of 2.0 V.

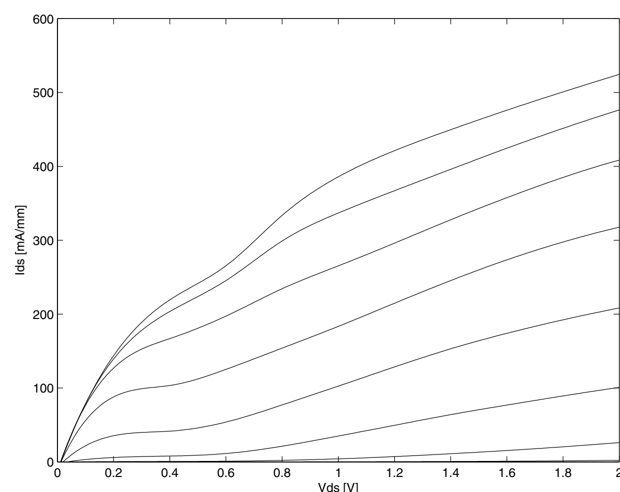

Fig. 2. I_{ds} (V_{ds},V_{gs}) of a 2x15 µm 50 nm InP HEMT. V_{gs}: -0.6 V to +0.3 V in steps of 0.1 V.

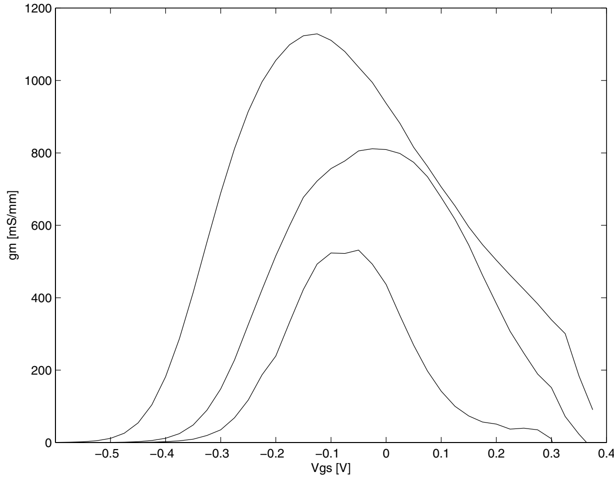

Fig. 3. DC $g_m(V_{gs})$ of a 2x15 µm 50 nm InP HEMT. V_{ds} = 0.2, 0.8 and, 2.0 V.

The S-parameters were measured on-wafer up to 50 GHz using a probe station and a HP8510C vector network analyser. Current gain ($|h_{21}|^2$) and unilateral power gain (U) versus frequency were extracted from the data ending up in an extrapolated f_t=199 GHz and f_{max}= 309 GHz at V_{ds} = 1.1 V and V_{gs} = 0.1 V for a 2x35 µm HEMT.

B. MIM Capacitors

The metal-insulator-metal capacitors were fabricated using reactively sputtered silicon nitride or silicon dioxide, typically between 1000 and 3000 Å thick. For electric fields below 1 MV/m, the capacitors exhibited a resistivity of about 10^{13} Ωcm for both the deposited silicon nitride and silicon dioxide films, which is fully adequate for MMIC capacitors.

To check the validity of the scalable models, different capacitor geometries were studied. We have used the distributed model shown in Fig. 4. The key elements are two coupled transmission lines with end effects. The air bridge and the capacitor plate to transmission line transitions are also accounted for by transmission line models (Fig. 5). Note that no fitting of model parameters have been made, only physical dimensions and constants have been used.

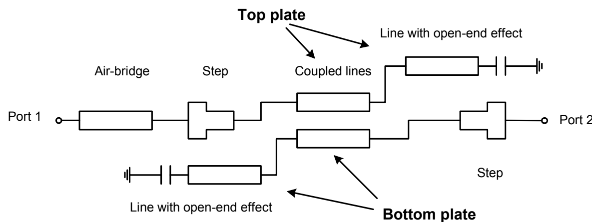

Fig. 4. Distributed model of a MIM capacitor.

C. TFRs

We have fabricated TFRs with reactively sputtered tantalum nitride (TaN) as the resistive material. TaN has been shown to display many of the qualities desired in a TFR material for microwave devices such as a high resistivity, a low temperature coefficient of resistivity,

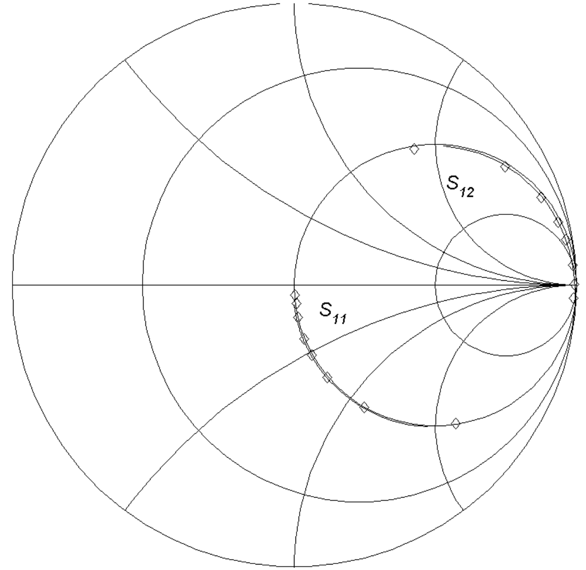

Fig. 5. Measured (diamonds) and modelled (line) S-parameters from 5 to 50 GHz for a 25x25 m^2 silicon nitride MIM capacitor.

simplicity of fabrication and chemical and temperature stability [4, 5]. The film thickness was 550 to 700 Å corresponding to resistances of 80-85 Ω/sq, which represent convenient values for circuit design. The TFRs were modelled as microstrip lines with lossy metal (Fig. 6).

III. MMIC PROCESS FLOW

The microstrip MMIC fabrication process followed the HEMT fabrication, with the following additions (Fig. 7). Prior to the gate definition, the TFRs were fabricated with a lift-off procedure.

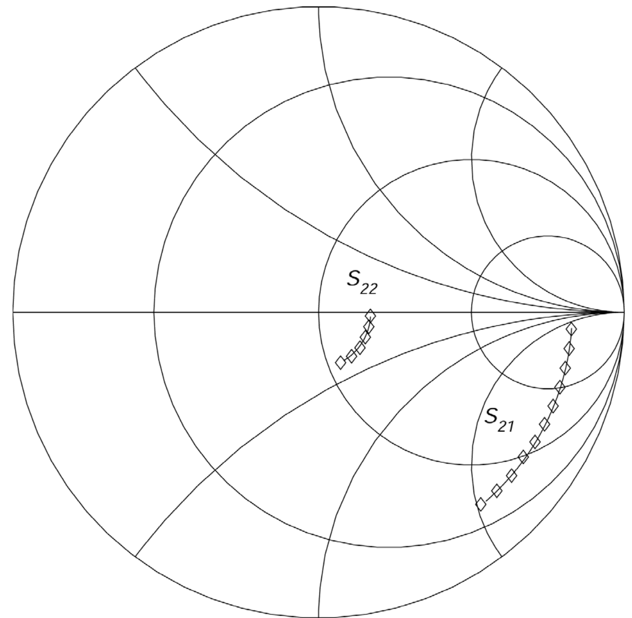

Fig. 6. Measured (diamonds) and modelled (line) S-parameters from 5 to 67 GHz for a 20-ohm TaN TFR.

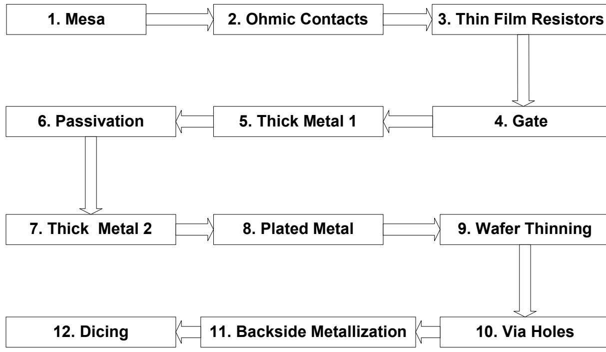

Fig. 7. Flow chart of the MMIC process.

The bottom plates of the capacitors were deposited directly on the InAlAs buffer layer exposed after mesa isolation, whereas the top plates were deposited on the dielectric right after device passivation, i.e. step 7 in Fig. 7. The capacitor top plates were connected to the transmission lines using electroplated air bridges. In the same step, gold was grown on the transmission lines and pads. The substrate was thinned down to 75 µm and via holes were wet etched from the backside. Finally, a 3-µm thick metal layer of gold was electroplated on the backside.

IV. RESULTS

To demonstrate the integration of the components into the MMIC process, a broadband, single-stage, resistive feedback amplifier was designed and manufactured (Fig. 8). The amplifier was designed around a 2x50 µm 50 nm InP HEMT, whose small-signal model was determined through extraction from S-parameter measurements [6], Fig. 9 and Table 1. The amplifier utilized a 250-ohm TFR and a 1.2-pF MIM capacitor in the feedback loop. To improve stability, the drain was loaded with a 10-ohm resistor in series. The S-parameters of the amplifier were measured on-wafer using coplanar probes with a network analyser. The amplifier exhibited more than 8-dB gain over a 0-42 GHz band at a DC power of 19 mW (Fig. 10).

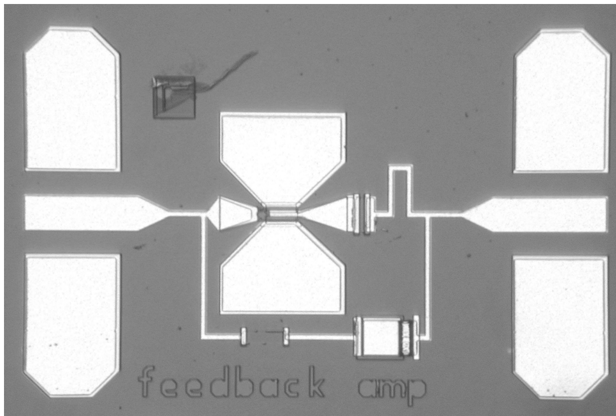

Fig. 8. Photograph of the InP HEMT MMIC feedback amplifier

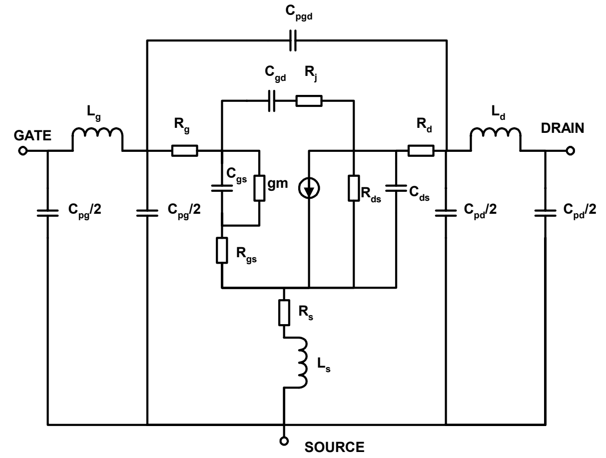

Fig. 9. Small-signal model of the InP HEMT.

Intrinsic	C_{gs}	59.9 fF	Parasitics	C_{pg}, C_{pd}	14.2 fF
	C_{ds}	43.1 fF		C_{pgd}	1.5 fF
	C_{gd}	9.5 fF		L_g	30.0 pH
	g_m	110 mS		L_s	1.0 pH
	R_i	1.0 Ω		L_d	36.0 pH
	R_j	44.2 Ω		R_g	3.0 Ω
	R_{ds}	159 Ω		R_s	5.6 Ω
				R_d	8.3 Ω

TABLE I
Extracted values for the small signal model used in the amplifier design. V_{ds} = 1.0 V, V_{gs} = -0.1 V, I_{ds} = 18.5 mA.

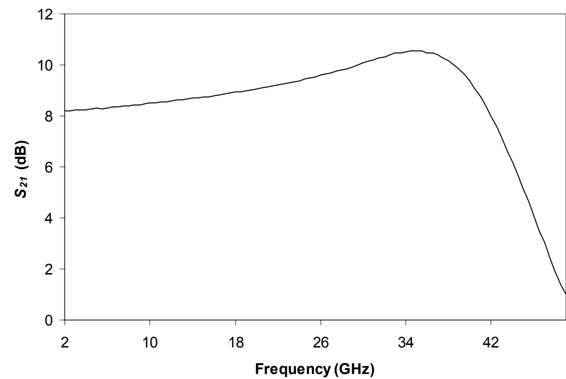

Fig. 10. S_{21} for the one-stage integrated feedback amplifier. V_{ds} = 1.0 V, V_{gs} = -0.2 V, and I_d = 19 mA.

V. CONCLUSION

Design and realization of pseudomorphic HEMTs, TFRs and MIM capacitors in a 50 nm InGaAs-InAlAs - InP HEMT process have been described. The components have been integrated in a MMIC process and demonstrated in a 0-42 GHz wideband amplifier.

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