

Robust GaN HEMT Low-Noise Amplifier MMICs for X-Band Applications

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Abstract—This work presents MMIC low-noise amplifiers based on AlGaIn/GaN HEMT technology on SiC substrate for robust receiver applications at X-band between 8 GHz and 11 GHz. Three versions of one-stage and two versions of two-stage amplifiers are presented with a noise figure of 1.81 dB at 10 GHz and 18 dB of small-signal gain for the two-stage device fully integrated in coplanar passive technology. The paper describes modeling and circuit design, bias dependence of the small-signal and noise circuit parameters of the MMICs realized, and high-power and intermodulation behavior.

I. INTRODUCTION

Significant progress has been achieved for III-N HEMT devices, especially for power devices and hybrid and integrated power amplifiers [1], [2]. However, there are so far relatively few reports on GaN HEMT based fully integrated MMICs in coplanar or microstrip passive technology due to the high requirements for a high-voltage passive technology on SiC substrates. The latter is e.g. due to the challenging substrate properties, such as micropipes and overall substrate quality, the challenge of homogenous epitaxial growth for high MMIC yield, and due to the challenge of homogenous processing.

Next to their outstanding power performance [2], GaN HEMTs are promising candidates for robust low-noise applications due to their low-noise performance, which is currently slightly inferior to GaAs PHEMT for the same gate-length [3], however provides enormous advantages in terms of linearity and robustness [4]. Recent MMIC examples can be found e.g. in [5], [6]. GaN HEMT devices in LNA front-ends are considered to reduce/to eliminate the need for additional RF limiting circuitry, which degrades noise performance and especially the dynamic range performance of the LNA in the system. This study presents several one- and two-stage low-noise MMIC amplifiers in coplanar technology operating between 8 GHz and 11 GHz with emphasis on low-noise and linearity evaluation.

II. GAN HEMT MMIC TECHNOLOGY

The AlGaIn/GaN HEMT technology is based on multi-wafer MOCVD III-N growth on two inch semi-insulating SiC wafers. Recent epitaxial development efforts concentrated on the reduction of the standard deviation of the sheet resistance below 2 % and improved device isolation.

For HEMT device processing, the device gate-length is 150 nm defined by electron beam lithography. Further details of the active GaN HEMT process are given in [7]. The devices in use show a current gain cut-off frequency f_T of 65 GHz at $V_{DS} = 7$ V and a maximum saturated drain current $I_D \geq 1100$ mA/mm.

The MMIC technology provides robust MIM capacitances with a breakdown voltage ≥ 150 V, inductances, and NiCr

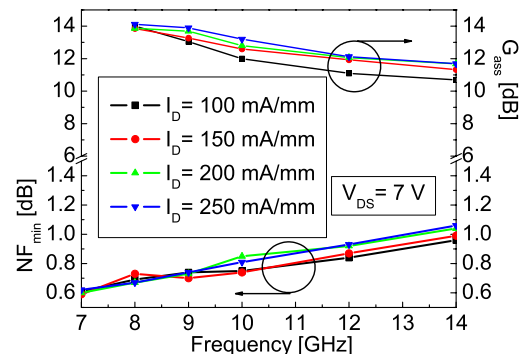


Fig. 1. Minimum noise figure NF_{min} and associated gain G_{ass} vs. frequency for an AlGaIn/GaN HEMT with $l_g = 150$ nm.

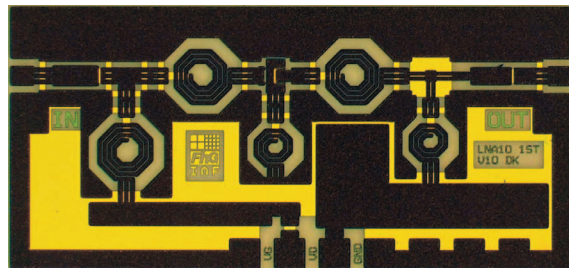


Fig. 2. Chip image of a one-stage GaN HEMT low-noise amplifier on SiC substrate, chip size 1 mm × 2 mm.

resistors. The passive circuit technology is coplanar and fabricated using thick galvanic gold. MMIC process yield was beyond 50 % for the proposed two-stage amplifiers on all wafers.

III. MODELING AND MEASUREMENTS

The coplanar passive components were modeled based on a purely passive run on semi-insulating SiC substrates with GaN epilayers [8]. A full coplanar library is extracted featuring 50 μm and 100 μm lines, T-junctions, MIM capacitances, and inductances.

For the active devices, high frequency noise measurements are performed up to 26 GHz using an Agilent 8975 noise figure meter and an ATN tuner system. Fig. 1 gives the measured minimum noise figure NF_{min} and the associated gain G_{ass} as a function of frequency for an AlGaIn/GaN HEMT on SiC with $l_g = 150$ nm and $W_g = 2 \times 60 \mu\text{m}$. At 10 GHz, a minimum noise figure of $NF_{min} = 0.7$ dB is measured at a drain current of $I_D = 150$ mA/mm. This result was reproduced in several process runs for the same device geometry and is consistent with the results obtained at other frequencies and bias points.

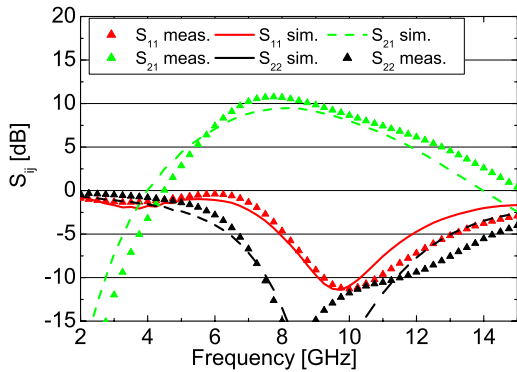


Fig. 3. Simulated and measured S-parameters as a function of frequency for a one-stage X-band LNA, $V_{DS} = 7$ V, version A.

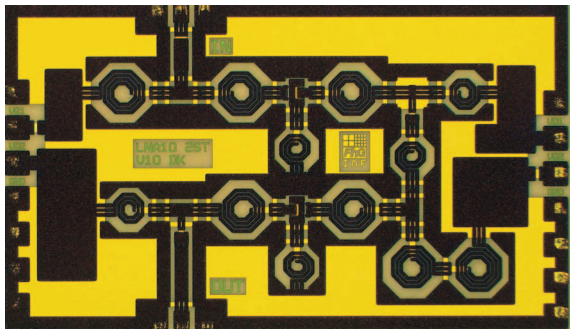


Fig. 4. Chip image of a two-stage GaN HEMT low-noise amplifier on SiC substrate, chip size $1.5 \text{ mm} \times 2.5 \text{ mm}$.

The selection of the device gate-width of $120 \mu\text{m}$ is based on the requirement for both minimum noise and support of a net input power of at least 23 dBm at appropriate bias. This requirement for regular operation exceeds a typical GaAs LNA destruction level without additional limiters [6]. Scaling of input gate width will then allow maximum input power levels of 30 dBm without limiters drastically increasing the dynamic range at the expense of a moderate increase in noise figure. For the $2 \times 60 \mu\text{m}$ device, the noise optimum generator impedance at $V_{DS} = 7$ V amounts to $\Gamma_{opt} = 0.68$ and 26° at 10 GHz derived from the measurements. The associated gain at $V_{DS} = 7$ V and $I_D = 150 \text{ mA/mm}$ amounts to $\geq 11.5 \text{ dB}$, as seen in Fig. 1.

The active devices were modeled based on small-signal S-parameters. A small-signal model is extracted and a Pospieszalski noise model derived from the noise measurements. Within this model, a maximum drain noise temperature of $T_{Drain} = 1820 \text{ K}$ and a gate temperature of $T_{Gate} = 300 \text{ K}$ are extracted at $V_{DS} = 7$ V and at drain current of $I_D = 150 \text{ mA/mm}$. Between 8 GHz and 14 GHz , the maximum deviation of the simulated and measured minimum noise figure NF_{min} of the $2 \times 60 \mu\text{m}$ device was $\leq 0.15 \text{ dB}$.

IV. MMIC CIRCUIT DESIGN

Based on the modeling of the active and passive components, three versions were designed of the one-stage and two versions for the two-stage amplifier. For both the one- and two-stage amplifier, version A is designed to be the most relaxed, version C is designed to be the most risky in terms of circuit stability. Fig. 2 depicts the chip image of the one-stage amplifier, version A. Chip size is $1 \text{ mm} \times 2 \text{ mm}$. The

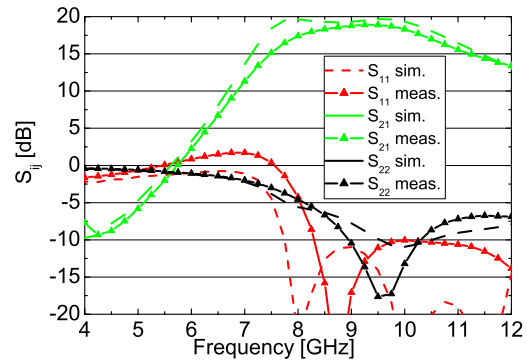


Fig. 5. Simulated and measured S-parameters as a function of frequency for the two-stage X-band LNA, $V_{DS} = 7$ V, version A.

gate-width amounts to $120 \mu\text{m}$. Fig. 3 gives the comparison of the simulated and measured S-parameters at $V_{DS} = 7$ V and $I_D = 150 \text{ mA/mm}$ drain current for the one-stage amplifier. The input and output match is better than 10 dB at 10 GHz and a maximum S_{21} of 10 dB is measured at 8 GHz . Measured reverse isolation S_{12} is better than -14 dB for the full frequency band. Fig. 4 gives the chip image of the two-stage design, version A. For the second stage, again a gate width of $120 \mu\text{m}$ is chosen. The chip size amounts to $2.5 \text{ mm} \times 1.5 \text{ mm}$. For both the one- and the two-stage design, the passive components consume most of the chip area leaving room for area reduction in future design iterations. Fig. 5 gives the comparison of the simulated and measured S-parameters of the two-stage amplifier at $V_{DS} = 7$ V for a drain current of $I_D = 150 \text{ mA/mm}$. At 10 GHz , we observe a measured $S_{21} \geq 18 \text{ dB}$, and a measured input and output match of better than 10 dB . Measured reverse isolation S_{12} is better than -28 dB .

Contrary to the one-stage design, both two-stage amplifiers are not unconditionally stable. The deviations of S_{ij} between measurement and simulations can be explained by improvements of the active device technology relative to the model extracted for LNA design. These include reductions of the intrinsic capacitances C_{gs} and an improvement of the source resistance R_S .

Summarizing the small-signal results from the different versions of each MMIC device, the following findings are made: For the three versions the measured S_{21} varied from 8 dB to 10 dB at $V_{DS} = 7$ V in the single stage design at 9 GHz . The input match S_{11} varied from -7 dB to -10 dB at 9 GHz . For the two-stage device, S_{21} varied from 17 dB to 18 dB at 9 GHz , while S_{11} varied from -10 dB to -15 dB at the same frequency.

V. NOISE CHARACTERIZATION

Low-noise characterization of the MMICs was performed on the same measurement system as for the active devices. Both source tuned and 50Ω source impedance measurements were performed. For the one-stage MMIC, Fig. 6 and Fig. 7 compare the noise figure NF and the minimum noise figure for MMIC version A between 7 GHz and 14 GHz at $V_{DS} = 7$ V for various drain currents. For 50Ω source impedance, the noise figure NF is minimized at a current of 150 mA/mm to 1.5 dB at 11 GHz . With appropriate tuning, the measurement yields a minimum noise figure of $NF_{min} = 1.35 \text{ dB}$ at the same bias at 11 GHz , and 1.2 dB at 9 GHz .

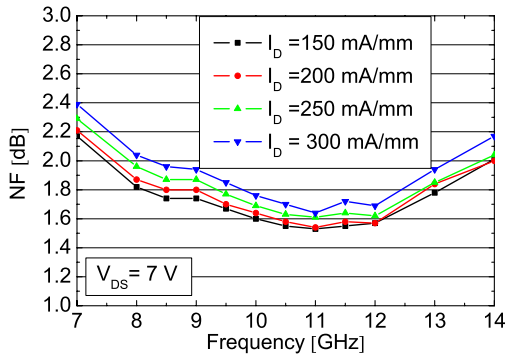


Fig. 6. Measured noise figure NF as a function of frequency for the one-stage X-band LNA for various drain currents I_D at $V_{DS} = 7$ V, version A.

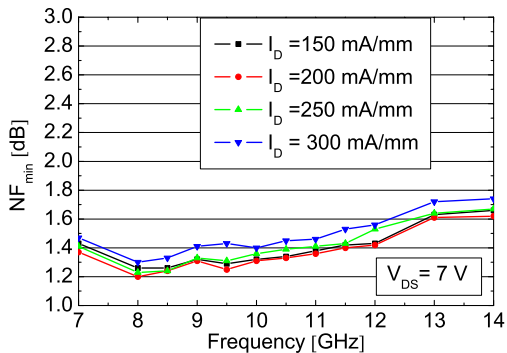


Fig. 7. Measured minimum noise figure NF_{min} as a function of frequency for the one-stage X-band LNA for various drain currents I_D at $V_{DS} = 7$ V, version A.

Fig. 8 gives the measured noise figure NF as a function of frequency for the two-stage LNA, version A, with the drain current as a parameter. A noise figure NF of 1.81 dB is observed for a drain current of $I_D = 150$ mA/mm at 10 GHz. At tuned input load and 10 GHz, the same two-stage device yields a noise figure of 1.5 dB at $V_{DS} = 7$ V. Thus, the second amplifier stage yields a contribution of less than 0.3 dB to the overall noise figure at 50 Ω source impedance and 10 GHz in comparison to Fig. 6.

Fig. 9 gives the measured noise figure NF vs. V_{DS} voltage and drain current I_D for the two-stage device. At a drain current of $I_D = 100$ mA/mm, the device did not provide a gain of ≥ 16 dB for all V_{DS} bias. It can be clearly seen that even at $V_{DS} = 20$ V, the noise figure amounts to ≈ 2 dB for a drain current of $I_D = 150$ mA/mm. Considering the different versions of the one-stage device, the noise figure NF of the one-stage MMICs at 9 GHz varied from 1.5 dB to 1.7 dB. For the two-stage MMIC, the noise figure NF at 9 GHz varied from 1.9 dB to 2.0 dB at $V_{DS} = 7$ V.

VI. LARGE-SIGNAL AND INTERMODULATION CHARACTERIZATION

For single frequency output power characterization, Fig. 10 shows the continuous wave (cw) output power measurement of the one-stage LNA, version B, for $V_{DS} = 25$ V and 50 Ω output match at 10 GHz. A net linear gain of 10 dB and a maximum cw power added efficiency (PAE) of 24 % are found. $P_{-1\text{ dB}}$ amounts to 22 dBm. A maximum saturated output power of

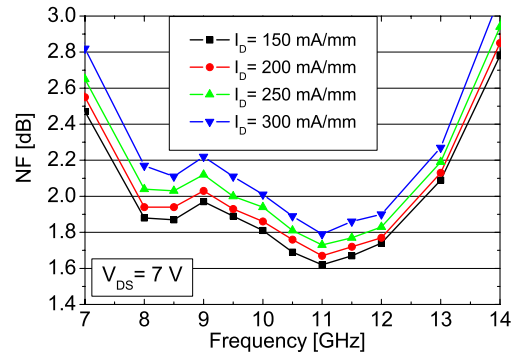


Fig. 8. Measured noise figure NF as a function of frequency for the two-stage X-band LNA for various drain currents I_D at $V_{DS} = 7$ V, version A.

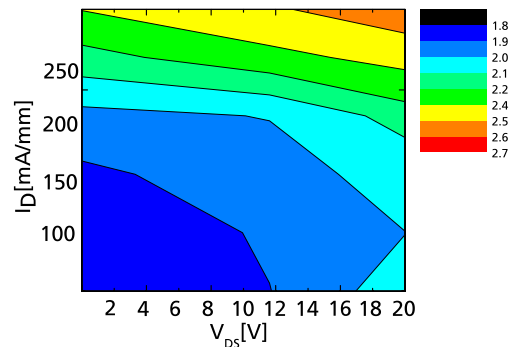


Fig. 9. Measured noise figure NF in dB as a function of drain current and V_{DS} voltages at 10 GHz for the two-stage X-band LNA, version A.

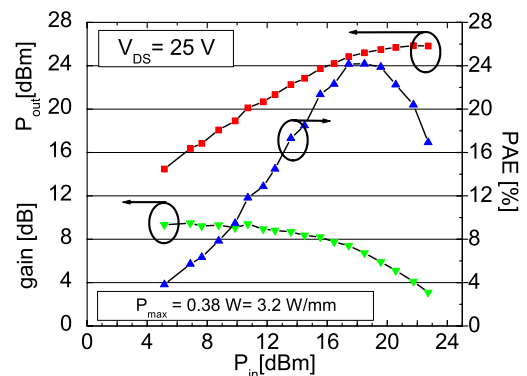


Fig. 10. Measured output power, gain, and power added efficiency for the one-stage X-band LNA, version B, for $V_{DS} = 25$ V at 10 GHz.

26 dBm is measured, which corresponds to a power density of 3.2 W/mm at 10 GHz. The maximum net input power amounts to 23 dBm or 1.7 W/mm at a compression level of $P_{-7\text{ dB}}$. Both the output power and the high compression level demonstrate the robustness of the GaN LNAs. Measurements to this compression level were repeated several times without indication of short term degradation. For low-noise bias at $V_{DS} = 7$ V, a maximum output power of 20 dBm, a PAE of 20 % with a linear gain of 9 dB, and a $P_{-1\text{ dB}} = 18.5$ dBm are reached. Maximum compression level was $P_{-5\text{ dB}}$ at an input power of 15 dBm.

The measured third order intermodulation (IMD_3) and cor-

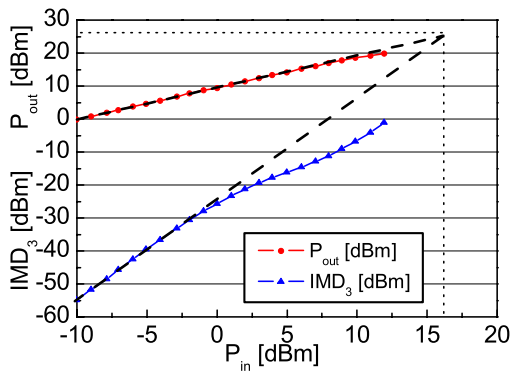


Fig. 11. Measured IMD_3 and output power as a function of input power for the one-stage X-band LNA at $V_{DS}=20$ V, $I_D=150$ mA/mm.

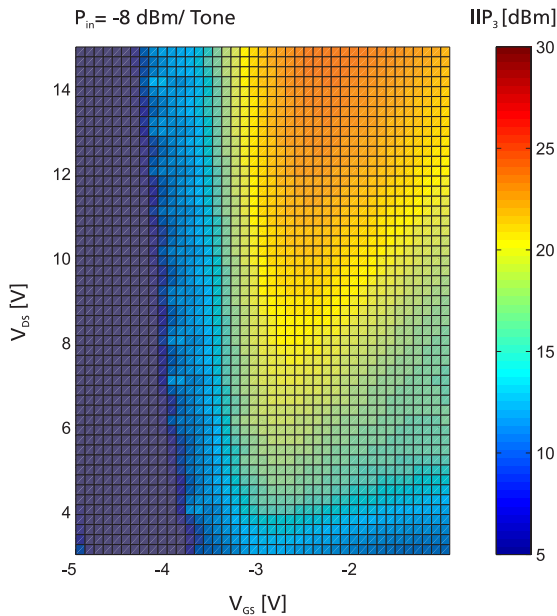


Fig. 12. Measurement of the input intercept point (IIP_3) as a function of V_{GS} and V_{DS} .

stages	version	S_{21} @ 10 GHz	NF@ 10 GHz
1	A	9 dB	1.6 dB
1	B	8 dB	1.49 dB
1	C	7 dB	1.51 dB
2	A	18 dB	1.81 dB
2	B	16 dB	1.71 dB

Fig. 13. Summary of the different versions of the one- and two-stage MMICs at $V_{DS}=7$ V and $I_D=150$ mA/mm.

responding two-tone output power measurements are given for the one-stage LNA in Fig. 11. At 10 GHz and 50 Ω load, a 1 MHz two-tone separation is used in an intermodulation measurement system based on spectrum analyzer and microwave transition analyzer. From the extrapolation shown in Fig. 11, an output side intercept point of $OIP_3 \geq 26$ dBm is found for an input power level of 16 dBm at $V_{DS}=20$ V assuming a 3rd order linearity model. In order to improve the accuracy of the OIP_3 extrapolation, for both input and output side of the MMIC, the intercept points were measured as function of input power. It was found that for an input power level P_{in} up to 2 dBm, both OIP_3 and IIP_3 are well defined. Based on this measurement, a bias dependent measurement of the input side intercept point is performed at $P_{in}=-8$ dBm/Tone as a

function of both V_{GS} and V_{DS} . Fig. 12 shows the V_{GS}/V_{DS} plane of the input side intercept point IIP_3 . This graph suggests increased linearity especially for high V_{DS} voltages ≥ 13 V at $V_{GS} \approx -2$ V or $I_D=300$ mA/mm. The use of GaN LNA MMICs will thus be a trade-off of low-noise performance at V_{DS} close to the knee voltage $V_{knee} \approx 5$ V, and high linearity, very robust power operation at $V_{DS} \gg V_{knee}$, in this case up to $V_{DS}=25$ V for a this HEMT process.

CONCLUSIONS

This work presents a comprehensive study of coplanar fully integrated MMIC low-noise amplifiers based on 150 nm GaN HEMT technology on SiC substrate for robust receiver applications at X-band. Three one-stage and two two-stage devices yield matched gain levels of as high as ≥ 9 dB per stage with a noise figure $NF=1.81$ dB at 10 GHz at 150 mA/mm. Some figures-of-merit are summarized in Fig.13. A maximum net input power level of 23 dBm is reached at a compression level of P_{-7dB} without any sign of short term degradation. The input side third order intermodulation intercept point (IIP_3) is measured and verified to be ≥ 27 dBm at 10 GHz for the one-stage MMIC. Operable V_{DS} voltage levels range from 5 V to 25 V at optimized drain currents of ≈ 150 mA/mm. The maximum output power density amounts to 3.2 W/mm at 10 GHz and $V_{DS}=25$ V. These comprehensive numbers achieved suggest the overall suitability of GaN/AlGaN HEMTs on SiC for highly-linear high dynamic range robust receiver applications.

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