The Fabrication and Characterization of High-Performance InP DHBTs (Invited)

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***Abstract* — We review the salient factors in the development of high-speed type-II NpN InP/GaAsSb/InP DHBTs. This new technology has swiftly transitioned from its 1997 launch in the university laboratory, to industrial production in 2004: the short incubation period can be read as clear evidence that InP/GaAsSb/InP DHBTs afford real world strategic advantages for the organizations that were first to reach market with it. The present article surveys the various approaches taken in the development 300 GHz f_T/f_{MAX} DHBTs for telecom and test applications: we present both the advantages and shortcomings associated with InP/GaAsSb/InP DHBTs. The current performance limiting factors are described and tentative projections are made for the future.**

I. Introduction: DHBTs in the 1990's

The interest of bipolar transistors for high-speed digital circuit applications have long been recognized. Our interest in the use of GaAsSb as a base layer material for InP DHBTs has its roots with the challenges associated with the realization of GaInAs –based DHBTs in 1996: although good power transistor characteristics were achievable at the time, reports indicated that transistor performance could be severely affected by the details of the grading scheme used at the B/C interface to overcome the blocking potential between the GaInAs base layer and the InP collector (see Fig. 1a). For example, the so-called "chirp" superlattice collector DHBTs could be prone to severe negative differential resistance phenomena if the grading superlattice period was longer than 1.5 nm [1] —effectively, this constrained growers to superlattice periods of < 3 monolayers. Although such superlattices could certainly be produced by modern epitaxial growth techniques, their implementation would involve a number of yield issues associated with growth uniformity on larger substrates as well as processing challenges associated with etching of quaternary (Al,Ga,In)As layers.

Around the same time period, impressive device performances were reported for step-graded launcher type structures which use a narrow-gap GaInAs layer to accelerate electrons over the band discontinuity between GaInAs and InP (Fig. 1b) [2]. The step-graded launcher collector appeared like a simple and effective solution to overcome collector blocking phenomena, it offered the possibility of achieving InP/GaInAs SHBT bandwidths with DHBT breakdown voltages at no extra cost. In practice, academic and industrial laboratories alike the found that attempts to implement the most interesting and promising published DHBT designs were often met with disappointing results, both with internally and vendor grown epilayers. These difficulties and their unclear causes have thus delayed the commercialization of GaInAs-based DHBTs.

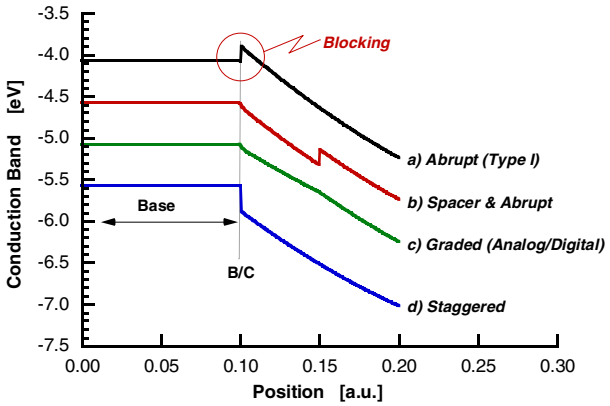

Fig. 1. Conduction band edge profile at the base/collector interface for various DHBT implementation strategies.

Such was thus the situation for compound semiconductor DHBTs in the mid-1990's. Our group's perspective by 1996 was that a successfully manufacturable technology should distinguish itself from other alternatives by its simplicity and ease of implementation on a large scale: clearly, if a new technology should be usable for the realization of chip sets with reasonably high transistor counts (perhaps as many as 1-10 K devices), one would need to develop robust materials structures and process architectures that could be produced with a high yield. Whereas this statement may be obvious to production engineers, it is not necessarily so apparent to academics. Simply put, we deemed it advantageous to work *with nature* rather than to try to *overwhelm it by design*.

GaAsSb bases seemed to provide an elegant avenue for the practical realization of high-speed InP DHBTs: we speculated, and later verified [5], that GaAsSb p-type base regions should show a staggered (or "type-II") lineup with respect to InP, thereby allowing electrons to be injected into the InP collector conduction band across an *abrupt* heterojunction (Fig. 1d). The rest of the DHBT structure seemed simple enough, consisting only of conventional GaInAs and InP layers (Fig. 2). Right

around the same time, independent reports from *Bellcore* and *Rockwell* demonstrated the first MOCVD-grown InP/GaAsSb DHBTs [3, 4]. These publications showed others were following similar thought processes. Both the *Bellcore* and *Rockwell* teams discontinued their GaAsSb DHBT development thereafter, presumably because early device results did not appear to offer a clear performance advantage over GaInAs SHBTs of the time. Fortunately, these early GaAsSb contributions already established the key fact that C- doping of GaAsSb was apparently very efficient and not prone to H- passivation effects in contrast to GaInAs –based devices. This later proved to have an enabling role in the realization of high-speed InP/GaAsSb/InP DHBTs at SFU.

II. Development of InP/GaAsSb/InP DHBTs

A. Principal Materials Characteristics & Phenomena

Fig. 2 shows the equilibrium band diagram of a representative NpN InP/GaAsSb/InP DHBT. At the outset, it should be noted that the InP emitter can easily be replaced with an (Al,Ga,In)As emitter should a type-I emitter structure prove desirable. The band diagram shows that a lattice-matched $GaAs_{0.51}Sb_{0.49}$ base provides a $\Delta E_C = -(0.10\text{-}0.15)$ eV with respect to the InP conduction band edge [5, 6]: because the GaAsSb energy gap is equal to ~0.72 eV, this results in a large valence band discontinuity between GaAsSb and InP that suppresses electron back-injection into the emitter. As well, this massive ΔE_V limits hole injection into the collector when the transistor is driven into saturation. This is an important advantage because some digital logic circuits nearly forward bias the base/collector junction, and a device that maintains good dynamic characteristics across large voltage swings should perform quite well.

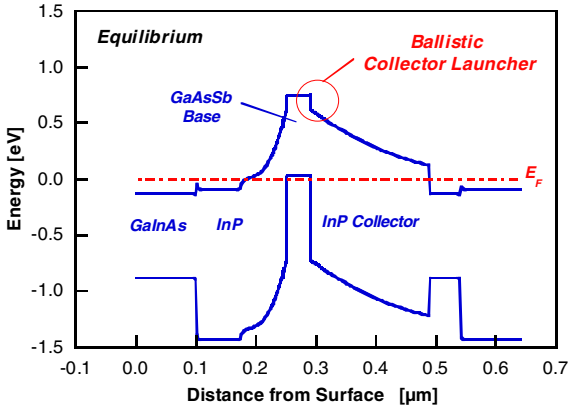

Fig. 2. Equilibrium band diagram for a staggered ("type-II") InP/GaAsSb/InP DHBT. Note this type of E/B junction results in thermal injection from the emitter into the base. Type-I AlInAs emitters have also been developed.

The use of an abrupt InP emitter structure is interesting from a number of perspectives: InP has a higher conductivity than AlInAs and it can be etched selectively with respect to GaAsSb. InP also offers a larger valence band discontinuity with respect to to GaAsSb. Because the surface Fermi level usually pins closer to the conduction band edge, InP shows a smaller surface depletion than found in AlInAs, which should help reduce emitter size effects and hopefully allow device models to scale with emitter size. Additionally, the higher thermal conductivity associated with InP emitters and collectors directly adjoining the base layer should help heatsink the devices under high power dissipation conditions. These attributes all suggest the InP/GaAsSb system offers key advantages for the fabrication of aggressively scaled HBT structures. Gummel characteristics from InP emitter devices show a collector current ideality of $n_C = 1.0$ indicative of *thermal* injection into the base: this helps maintain a lower base/emitter turn-on voltage that is helpful in limiting power dissipation in various applications such as digital circuits and long talk-time wireless circuits. One drawback associated with thermal injection is that base transport proceeds by diffusion only, without the assistance of hot electron transport as in the case of InP emitters on GaInAs bases [7].

The GaAsSb alloy turns out to be a very interesting material for base layers: its low energy gap results in low turn-on voltages. Another one of its key features is that GaAsSb shows a very high affinity for C- doping in MOCVD grown material: doping concentrations as high as 2.5×10^{20} /cm^3 have been demonstrated with minimal H- passivation effects since the SIMS H- concentration may be < 4% of the C- doping level [8, 9]. This greatly simplifies the fabrication of DHBTs because it eliminates the need for high-temperature annealing cycles to drive out passivating hydrogen incorporated into the device layers. GaAsSb is different from GaAs, as it seems that the majority of C atoms incorporate substitutionally in the lattice: this may explain why C- clustering has not yet been detected in GaAsSb DHBTs even after high-current high-temperature stressing. GaAsSb however does suffer one major disadvantage with respect to GaInAs from a transport point of view: it features a somewhat lower electron mobility that tends to lengthen the base transit time compared to diffusion across a GaInAs base of the same thickness. This result is not so puzzling once one considers the fact that whereas InAs has a 300 K peak mobility of some 30,000 cm^2/Vs, the electron mobility in GaSb is < 3,000 cm^2/Vs, and alloying with GaAs can only be expected to reduce the mobility with respect to that of pure GaAs.

Another inherent advantage associated with the use of GaAsSb base layers is the relative insensitivity of device performance to the exact composition of the alloy. This is to be contrasted to the exquisitely precise thickness, composition and doping control required in interface grading for GaInAs DHBTs, as mentioned in the Introduction. The reason for this is that GaAsSb is expected to make a transition to a type-I lineup for $x_{Sb} = 0.27$ [6]. Small excursions in the base mole fraction, say ± 5%, in fact have little discernible first order impact on the gross transistor properties, presumably because

the GaAsSb alloy energy gap shifts very little with composition as a result of significant bowing. It must be noted that GaAsSb is truly very well-suited to the fabrication of ultrathin base DHBTs: extremely heavy p-type doping can be achieved, and the resulting reduction of the lattice constant with high C- doping levels can be compensated by adjusting the As/Sb solid solution ratio. This possibility does not appear to exist for GaInAs base layers since C- tends to incorporate as a donor in InAs.

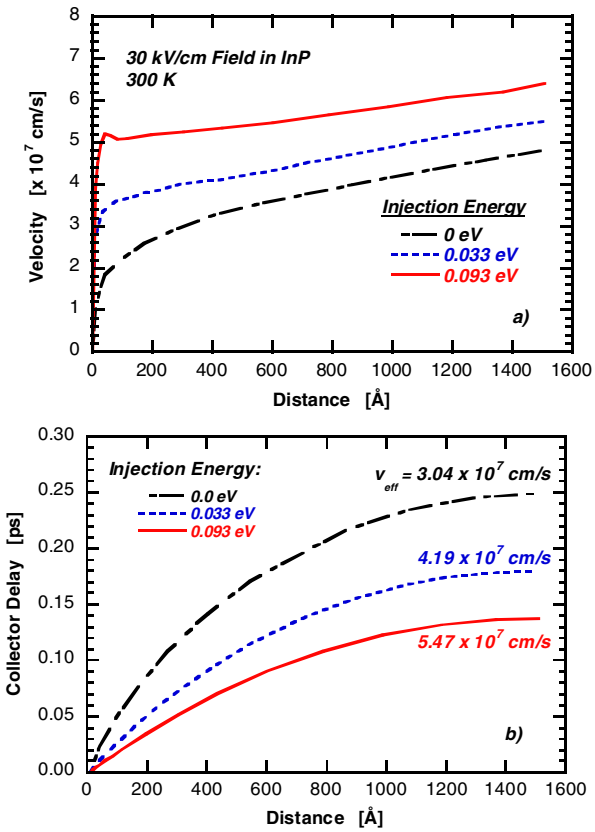

Fig. 3. a) Monte Carlo average electron velocity in a 30 kV/cm field with the launching energy as a parameter [10]; b) corresponding collector signal delay across a 1500 Å collector, showing the average collector velocity $v_{\text{eff}} = \tau_C/2W_C$. Clearly, a small launching energy is greatly beneficial.

Finally, the ability to form an abrupt base/collector heterojunction confers a number of advantages to the GaAsSb –based DHBT. Perhaps one of the most interesting advantages is that electrons are launched in the collector with a ballistic collector velocity corresponding to the ΔE_C at the base/collector junction. This results in a high initial electron velocity in the collector near the base layer, and it has been shown by Laux and Lee [11] and Ishibashi [12] that the initial collector velocity has a strong impact on the overall collector signal delay τ_C. We can evaluate the potential impact of the type-II B/C launcher by calculating the collector signal delay from the Monte Carlo results of Brennan and Hess [10] who considered the effect of injection energy on the velocity profile for electrons injected in a 1500 Å InP layer supporting a 30 kV/cm field.[1] Clearly the figure shows that ballistic injection results in a significantly higher initial collector velocity compared to the case where electrons experience acceleration solely due to the electric field alone. For example, increasing the injection energy from zero to 93 meV nearly halves the collector delay and increases the average collector velocity from 3.0 to 5.5×10^7 cm/s across a 1500 Å InP collector.

B. Current Limitations to Device Bandwidth

The drive to wider bandwidths has recently led us to perform a careful analysis of transistor delays in InP/GaAsSb/InP DHBTs in order to quantitatively understand which aspects of the devices is in most urgent need of improvement: the GaAsSb –based DHBT was the first bipolar transistor to break the 300 GHz milestone, [13] once thought to be the exclusive domain of nanogate InP HEMTs, but a number of bipolar technologies have followed suit with = 300 GHz cutoff frequencies in both SiGe and GaInAs.

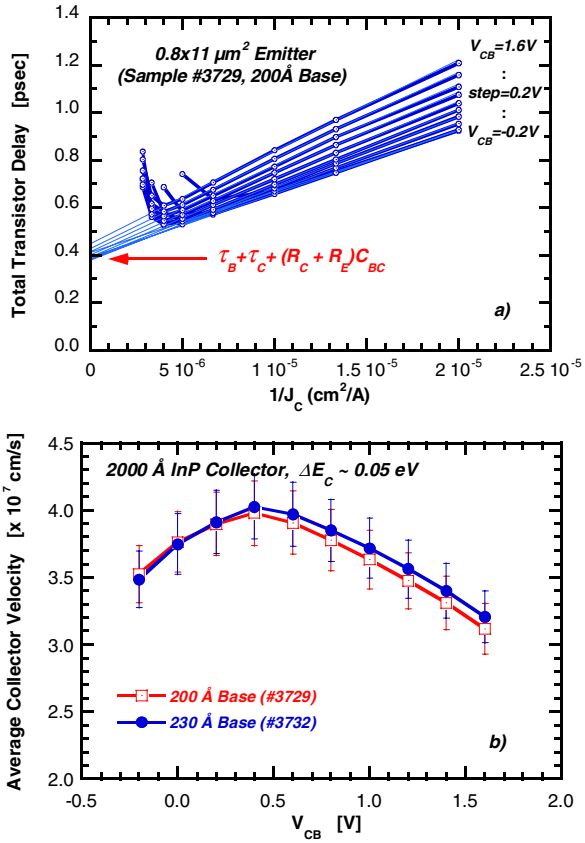

Fig. 4. a) Total delay *vs.* inverse current density and extrapolation to infinite current to strip dynamic emitter resistance delay contribution; b) extracted average collector velocity for two base thicknesses.

The main results of our delay analysis are summarized in what follows. Fig. 4a) shows plots of delay versus $1/J_C$ used to extract the residual $\tau_B + \tau_C + C_{BC}(R_E + R_C)$ delay time. The $C_{BC}(R_E + R_C)$ charging time was then stripped from the data by a combination of "flyback" and open collector *S*-parameter measurements, and bias-dependent

[1] The conditions do not exactly match existing DHBTs but are nevertheless useful in order to gain insight into device operation. Current transistor performance peaks for an average field of 50 kV/cm in a 2000 Å collector.

extraction of C_{BC}. The base transit time τ_B was evaluated by performing a delay analysis on two samples differing only their base layer thickness (200 *vs.* 230 Å) to extract the effective electron diffusivity through the base layer. For these samples with $x_{Sb} = 0.38$, $D_n = 43$ cm^2/s.

The above extraction procedure reveals that around peak f_T current the emitter dynamic resistance contributes ~0.10-0.15 ps to the total transistor delay, τ_B amounts to ~0.12 ps for a 200 Å base layer, while the collector signal delay amounts to $\tau_C \sim 0.25$ ps, while $C_{BC}(R_E + R_C)$~0.05 ps only.

III. Developments Prospects and Possibilities

It would appear reasonable to expect that the first three delay components could potentially be halved by appropriate scaling and the application of graded base techniques to InP/GaAsSb/InP DHBTs, and designing the devices to operate at higher current densities (with a thinner collector layer to delay the onset of Kirk like effects). Simple estimates would suggest that total transistor delays < 0.2 ps could be achieved, corresponding to cutoff frequencies $f_T \sim 800$ GHz.

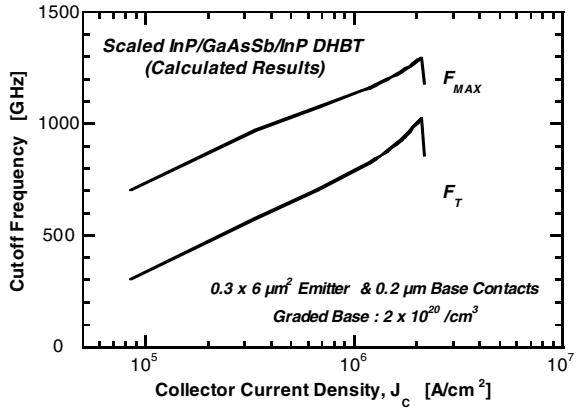

Fig. 5. Calculated performance for optimized scaled InP/GaAsSb/InP DHBTs.

To further test this idea, we have run more detailed estimates of possible device performance using our most current understanding of the operation for InP/GaAsSb/InP DHBTs. Fig. 5 shows the results of one such "*what if*" computer calculations: devices with simultaneous f_T and f_{MAX} cutoff frequencies exceeding 1 THz could be achieved with appropriately scaled InP/GaAsSb DHBTs: our group is taking some of the steps in that direction, and these will be discussed at the Conference. It is not clear whether or not we will succeed, but the most important fact to take away from the present discussion is that *all* the assumptions going into Fig. 5 are quite reasonable based on our current understanding of GaAsSb technology: the degree of success achievable in this process/device optimization exercise will determine how closely real device performance will approach Fig. 5. One thing is however quite clear from these considerations: much room for improvement remains for type-II InP DHBTs.

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