Application of SiGe:C BiCMOS to Wireless and Radar

Wolfgang Winkler, Bernd Heinemann, Dieter Knoll

IHP, Im Technologiepark 25, D-15236 Frankfurt (Oder), Germany, Phone: +49-(0)-335-5625-150

Abstract — Heterojunction bipolar transistors with carbon-doped SiGe base layer (SiGe:C HBTs) showing f_T and f_{max} values as high as 200 GHz have been developed and integrated into a 0.25µm CMOS platform. The combination of these high-performance HBTs with a modern CMOS backbone and a full menu of passive elements enables the fabrication of advanced wireless communication and radar systems. In this paper, we address the application of IHP's 200GHz SiGe:C BiCMOS process in two fields, the wireless communication in the 60GHz ISM band and radar applications at 24GHz, 77GHz and at frequencies above 94GHz.

I. INTRODUCTION

BiCMOS RF performance has strongly been improved during the last years through the integration of heterojunction bipolar transistors with carbon-doped SiGe base layer (SiGe:C HBTs) which reach meanwhile transit and maximum oscillation frequencies (f_T , f_{max}) of 200GHz and beyond [1-4]. The combination of these high-performance HBTs with a modern CMOS core and a complete menu of passive elements enables new product application areas. In this paper, we address the application of IHP's 200GHz SiGe:C BiCMOS process (SGC25C) in two fields, the wireless communication in the 60GHz ISM band and radar applications for automotive at 24GHz and 77GHz and other sensor applications above 94GHz.

In chapter II, we will first describe the SGC25C BiCMOS process and the device menu offered. Then, chapter III will deal with the circuit applications of this technology, focusing on some examples of the wide spectrum of fabricated components such as frequency dividers, LNAs, ring oscillators, LC oscillators, mixers and clock and data recovery circuits.

II. TECHNOLOGY AND DEVICES

SGC25C is IHP's first BiCMOS process which offers bipolar transistors with 200GHz cut-off frequencies. Fig. 1 illustrates both the full SGC25C BiCMOS process flow and the detailed flow for the HBT module. The HBT uses a single-polysilicon construction and an implanted extrinsic base layer (Fig. 2). This layer is formed on isolator regions during the non-selective epiprocess applied to grow the intrinsic SiGe:C base layer and a Si cap. The implantation step for doping the extrinsic base layer is carried out self-aligned to the outer edge of the polysilicon emitter, but not self-aligned to the emitter window. Shallow trench etch and fill Deep n-well implantation (isolated NMOS) MOS well implantations Gate oxidation, Gate poly deposition Gate etch, Spacer formation

Deposition of CMOS protection layers Opening HBT regions High dose collector implant + RTA Oxide deposition Opening active collector regions Si / SiGe:C/ Si epitaxy Opening emitter windows + SIC As doped emitter deposition Structuring polysilicon emitters + External base implant External base structuring Removing protection layers by wet etch

S/D implantations, RTA Salblock, Co salicide formation LI, Contact, Met-1, Via-1, MIM, Met-2 Via-2, Met-3, Via-3, Met-4, Passivation

Fig. 1. SGC25C process flow.

The high f_T results primarily from a novel collector design, which substantially reduces base-collector charging and transit times [2]. The key new SGC25C device features are the formation of the whole HBT structure in one active area without STI stripe between emitter and collector contacts, the complete lateral enclosure of the highly doped collector wells in the STI sidewalls, and the self-alignment of the collector contact region to the base-poly edge (Fig. 2). This allows us to achieve collector resistances that are even lower than



Fig. 2. Schematic cross section of a SiGe:C HBT as used in SGC25C.

the emitter resistance. In addition, the new design reduces device dimensions and parasitic capacitances. The reduced collector area results in a 50% reduction in the collector-substrate capacitance compared to the HBTs of the previous BiCMOS generation (SGC25B). Furthermore, since the collector well fabrication is implemented after the critical thermal treatments, this device design allows us to produce extremely steep collector doping profiles and achieves better control of the width of the base-collector space charge regions. Finally, the absence of DTI improves the heat dissipation and reduces the thermal resistance. In addition to the introduction of a new collector design we also optimized the base-collector as well as the emitter-base depletion widths by adjusting the buffer and cap thicknesses of the epi layer stack in order to maximize f_T. Fig. 3 compares the $f_{T}\xspace$ vs. $I_{C}\xspace$ curves of SGC25B and SGC25C HBTs and illustrates, by a comparison of transit time components, from what the SGC25C performance gain results in detail.



Fig. 3. Transit frequency vs. collector current for SGC25B and SGC25C HBTs, and comparison of the transit time components of these transistors.

Table 1 summarizes the SGC25C HBT parameters, while MOS parameters and passive elements are listed in Table 2. For the circuits discussed in following, most of these active and passive devices were used.

Parameter	Value	Unit	Remark	
Emitter dimens.	0.21x0.84	μm ²	Drawn dim.	
Current gain	300		$@V_{BE} = 0.7V$	
Peak f _T	200	GHz	$\bigcirc V = 1.5V$	
Peak f _{max}	200	GHz	$(\underline{w}) \mathbf{v}_{CE} = 1.5 \mathbf{v}$	
BV _{EBO}	>1.5	V	@ I _{EB} = 1µA	
BV _{CEO}	>1.85	V	Extrapolated	
BV _{CBO}	4.5	V	@ $I_{CB} = 0.1 \mu A$	
Early voltage	>40	V	$I_B = const.$	
B-E capacitance	3.8	fF	$@V_{EB}=0V$	
B-C capacitance	3.3	fF	$@V_{CB}=0V$	
C-S capacitance	3.0	fF	$@V_{CS} = 0V$	
Emitter resist.	19	Ω		
Collector resist.	16	Ω		
Base resistance	110	Ω	Circle fit of s_{11} @ $V_{BE} = 0.9V$	

TABLE 1: SGC25C HBT PARAMETERS.

Device	Param.	Value	Unit	Remark	
NMOS	I _{ON}	540	μA/μm	$@V_{DS}=2.5V$	
and	I _{OFF}	0.4	pA/µm		
Isolated	V _T	0.60	V		
NMOS	L _{EFF}	0.24	μm		
PMOS	I _{ON}	230	μA/μm	$@V_{DS}=2.5V$	
	I _{OFF}	0.5	pA/µm		
	V _T	-0.56	V		
	L _{EFF}	0.245	μm		
MOS Varactor	Tuning	1:3.4		-2.5V <v<2.5v< td=""></v<2.5v<>	
	O factor	120/30		for low/high	
, araovor	V Incioi	120/50		C @ 5GHz	
Salicide	R _S	6.6	Ω/sq	Silicided gate	
Resistor	TCR	2900	ppm/°C	poly	
Poly-Si	R _S	95	Ω/sq	Gate poly (n ⁺)	
Resistor	TCR	450	ppm/°C		
Poly-Si	R _S	350	Ωsq	HBT base poly	
Resistor	TCR	50	ppm/°C		
MIM- Capa- citor	C/A	1	fF/µm ²		
	VCC1	11	ppm/V	-	
	VCC2	1.6	ppm/V ²	$5V < V_{MIM} < 5V$	
	TCC	<10	ppm/°C	-40°C - 125°C	
	BV	>30	V	(a) $1 \text{pA}/\mu\text{m}^2$	
Predef.	Q factor	4		23.8nH, 1GHz	
Inductors	(examp.)	16		0.94nH, 10GHz	

TABLE 2: PARAMETERS OF SGC25C MOS TRANSISTORS AND PASSIVE ELEMENTS.

III. CIRCUIT APPLICATIONS

The IHP high-speed technologies with transit and maximum oscillation frequencies (f_T , f_{max}) up to 200 GHz enable new product application areas. For demonstration, a series of benchmarking circuits were designed and tested successfully. The main results are summarized in TABLE III. Intended applications are very high data rate wireless links in the 60 GHz ISM band and automotive radar at 77 GHz and beyond.

Circuit	Parameter	Value	Ref.
Static freq. divider, 1:2	Maximum	62 GHz	[5]
Dynamic divider, 1:2	frequency	72 GHz	[5]
Low power divider, 1:64,	Max. input frequency	2.4 GHz	[5]
$V_{CC} = 1$ Volt	Sup. current	0.6 mA	
60 GHz LNA	Gain @ 61 GHz	9.6 dB	[6]
LC oscillators	cillators Oscillation 60 GHz frequency 97 GHz 117GHz		[8]
Ring oscillators	Gate delay	3.6 ps	[3]

TABLE III Summary of Benchmarking Circuits

A. GHz Transceiver Circuits

For demonstration of new wireless transmission systems with data rates > 150 Mb/s key circuit blocks for a 60 GHz transceiver system were designed and fabricated [5], [6].

Fig. 3 shows the block diagram of the proposed transceiver. It is based on amplitude shift keying modulation principle (ASK). The reasons for the selection of this modulation technique are: its simplicity, the wide bandwidth of the 61 GHz ISM band and there is no need for high-performance A/D converter.

The transmit path of the transceiver consists of a 61.25 GHz fundamental mode oscillator, a switch and a power amplifier. Between the modulator and the power amplifier a filter is inserted to reduce spurs. The receiver path consists of a low noise amplifier (LNA), a mixer, a 56 GHz oscillator, a variable gain amplifier and an ASK demodulator.



Fig. 3. Transceiver block diagram

The three-stage LNA circuit of the transceiver is shown in Fig. 4 and Fig. 5. One task of the LNA design was to get unconditional stability for both on-wafer measurements and for the use of the amplifier in test board modules together with the other receiver components. Especially the use of bond wires for the connection of the ground potential (and the associated inductance) causes serious stability problems if a singleended configuration is used. That's why all the stages are designed in differential configuration. The input and output are trafo-coupled. The transformer coupling is useful in two ways. First, it acts as a balun for connection to a single-ended antenna. Second, the primary and secondary windings of the transformer are tuned to gat a bandpass characteristic. With this, an additional input filter in the RX path can be omitted and this function is integrated in the LNA.

The circuit of one single stage of the LNA is shown in Fig. 5. It is a differential stage with inductive load and with matching network at the output.







B. VCOs for Radar Applications

High-frequency oscillators are key components in modern low-cost radar systems for automotive and other sensor applications. Most of today's automotive radar systems utilize the frequency bands at 24 and 77 GHz. For future developments, also higher frequency bands at 94 and 140 GHz are under discussion. Also other applications such as millimeter-wave holography with high resolution require oscillators at very high frequency [7]. Reasons for the use of higher frequency bands are the further miniaturization of the radar systems and the better beam forming prospects due to the shorter wavelength.

Several LC oscillators for the different frequency ranges were designed and tested [8], [9].

The circuit diagram of the LC oscillators is shown in Fig. 7. The circuit is a common collector Colpitts oscillator in fully differential implementation. With the symmetric circuit, two advantages are reached: First, it gives reduced signal interference via the silicon substrate and, second, the coupling of the high-frequency energy to subsequent building blocks such as integrated amplifiers or mixers is more effective.



Fig. 7. Circuit diagram of the high frequency oscillator.

The diodes and resistors in the circuit are used to define the operating point of the transistors. The tank is a symmetric circuit of two Inductors L1 and L1' and the MIM capacitors C_1 , C_2 , C_1 ' and C_2 '. In parallel to the MIM capacitors C_1 and C_1 ' act the base-emitter capacitors C_{BE} of the bipolar transistors. For explanation, the tank can be divided into two half circuits separated by the symmetry line shown in Fig. 7. In operation, the oscillator-halves are working in the odd mode, such that the outputs are 180° out of phase. The nodes of the tank indicated by the symmetry line are fixed at virtual ground for the fundamental tone. With this circuit principle, LCoscillators for different applications (mainly for automotive radar) were designed and tested. The highest frequency reached was 117GHz [9].

Fig. 8 shows the measured output spectrum of the oscillator. The output power is -12.24 dBm per output channel. The frequency of oscillation can be tuned by applying a tuning voltage at the V_{Ctrl} input thereby changing the current flowing through the oscillator core. With increasing current level the frequency is reduced. The tuning range is from 117.2 GHz to 113.7 GHz for the control voltage changing from -2.5 V to 0 V. The overall current consumption varies from 10 mA for the highest frequency to 28 mA for the lowest frequency. The maximum output power is -11.2 dBm at 113.7 GHz.

VI. CONCLUSIONS

We have described IHP's modular SiGe:C RF BiCMOS technology providing SiGe:C HBTs combined with a $0.25\mu m$ CMOS core and state-of-the art passive elements. This process menu ideally fulfills the technological requirements for the fabrication of modern wireless communication and radar systems. Circuit examples are 60GHz transceiver and radar circuits.



Fig. 8. Output spectrum of the 117 GHz oscillator.

ACKNOWLEDGEMENT

The authors acknowledge the IHP technology team for chip fabrication and J. Borngräber for measurements.

REFERENCES

- [1] B.A. Orner et al., "A 0.13μ m BiCMOS technology featuring a 200/280GHZ (f_T/f_{max}) SiGe HBT", Proc. of the 2003 BCTM, p. 203.
- [2] B. Heinemann et al., "Novel collector design for high-speed SiGe:C HBTs", IEDM 2002 Tech. Dig., p. 775.
- [3] H. Rücker et al., "SiGe:C BiCMOS technology with 3.6ps gate delay", IEDM 2003 Tech. Dig., p. 121.
- [4] T. Hashimoto et al., "Direction to improve SiGe BiCMOS technology featuring 200-GHz HBT and 80nm gate CMOS, IEDM 2003 Tech. Dig., p. 129.
- [5] W. Winkler, et al., "High-performance and lowvoltage divider circuits fabricated in SiGe:C HBT technology," ESSCIRC Digest of Technical Papers, Sept. 2002, pp. 827-830.
- [6] W. Winkler et al., "60 GHz Transceiver Circuits in SiGe:C BiCMOS Technology", ESSCIRC Leuven, September 2004, accepted for publication.
- [7] D. M. Sheen, D. L. McMacin, T. E. Hall, "Threedimensional millimeter-wave imaging for concealed weapon detection", *IEEE Transactions on microwave theory and techniques*, vol. 49, no. 9, pp. 1581-1591, September 2001.
- [8] W. Winkler et al., "60 GHz and 76 GHz oscillators in 0.25 μm SiGe:C BiCMOS", IEEE Int. Solid-State Circuits Conf., February 2003, pp. 454-455.
- [9] W. Winkler et al., "LC-Oscillators above 100 GHz in Silicon-Based Technology", ESSCIRC Leuven, September 2004, accepted for publication.
- [10] http://www.ihp-ffo.de/ihpoffer/Deliverables%20and %20Services2004.htm.