A GaAsSb/InP HBT circuit technology

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***Abstract* — A InP/GaAsSb/InP double-heterojunction bipolar transistor (DHBT) structure has been defined, realized by MBE epitaxy, and optimized, thanks to simulation based on in-depth physical characterizations. A circuit-oriented technology has been developed, which has been validated by the design and fabrication of a full-rate (40 GHz clock) 40 Gbit/s D-FF.**

I. Introduction

InP/GaAsSb material has been for long identified as having a great potential for high performance HBTs [1]. InP/GaAsSb transistors have been developed and cut-off frequencies beyond 300 GHz have been achieved [2]. In this paper, we report on the fabrication of a GaAsSb/InP DHBT structure, its optimization thanks to physical simulations based on physical characterization, and the development of an associated circuit-oriented process. This process has been validated by the fabrication and characterization of a full-rate 40 Gbit/s D-FF. Epitaxial growth is presented in section II, material characterization in section III, simulation-based optimization in section IV, DHBT circuit technology in section V; the design, fabrication and characterization of the validation circuit is reported in section VI.

II. GaAsSb/InP epitaxy and characterization

A VG 100 multi 4"wafers MBE system equipped with standard Veeco effusion cells for Group III and Group V elements was used for the elaboration of the structure. Regular solid Si and CBr_4 gaz sources were used as n- and p-type dopants respectively. Growth temperature was monitored by Ircon pyrometer. DHBT InP/GaAsSb/InP growth was conducted on nominally exact (001) InPact InP:Fe substrates. Devices structures consist in a heavily doped InP/GaInAs lattice matched subcollector, a 250 nm InP low doped collector (few 10^{16} cm^{-3}), a 50 nm GaAsSb heavily doped base (C: 8 10^{19} cm^{-3}), a 70 nm doped InP emitter and a heavily doped InP/GaInAs emitter cap. The typical base sheet resistance value determined by TLM measurements is ρ_B = 760 Ω/sq. Optimal growth conditions were obtained by a fine tuning of the growth temperature, total group V to III ratio with a particular attention to the GaAsSb base material. A preliminary work [3] has shown that the p-type carriers mobility can be maintained at 28 cm^{-2}/V/sec with corresponding doping as high as 2.5 10^{20} cm^{-3} (Fig. 1).

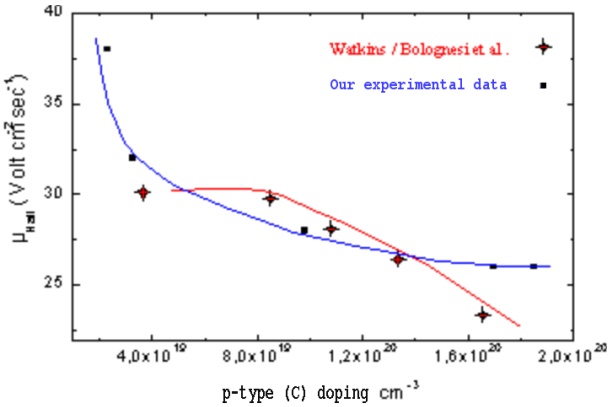


Fig. 1: GaAsSb hole mobility

X ray diffraction peak relative to the GaAsSb base material intentionally off matched regarding InP lattice parameter indicates very high crystalline quality (Fig. 2). The presence of fringes are corresponding to the GaAsSb epilayer grown onto lattice-matched InP/GaInAs underlying layers.

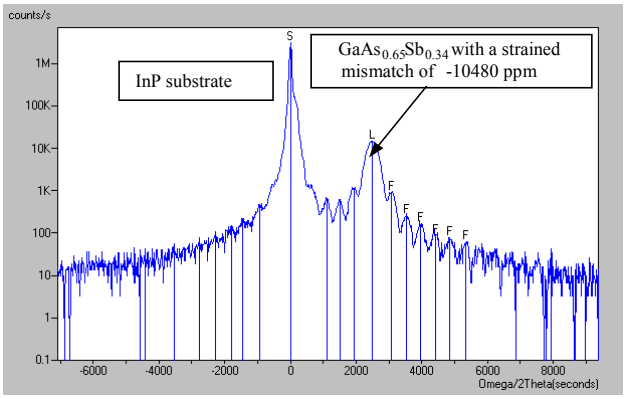


Fig. 2: X ray diffraction spectrum

III. Physical characterization

From extensive photoluminescence (PL) and photoreflectance (PR) spectroscopy, we evidenced the type-II nature of the InP/GaAsSb interface which impacts both the emitter-base injection efficiency, and the collector electron average velocity, leading to high speed

transistors [4]. The conduction band offset ΔE_c was found to be ~95 meV for Sb fraction X_{Sb} = 45.7% [5]. The Fermi level pinning at the GaAsSb surface (which impacts on the base sheet resistance) is found to be pinned at 220 meV above the valence band. Finally, PL and PR analysis led us to conclude to rather strong localization effects, related to potential fluctuations probably induced by alloy disorder in antimonide alloys [6].

IV. GaAsSb DHBT structure optimization

A. Physical simulations

Accurate physical simulations were performed to save expensive technological effort and confirm significant direction of improvements of the device performances. A two dimensional device simulation software is used to calculate the DC characteristics of the DHBT. The carrier transport mechanisms are described by a hydrodynamic model derived from Stratton energy balance equations, which is extended to the case of degenerate semiconductors. The numerical solution is achieved using self-consistent solution of Stratton partial differential equations coupled with Poisson and carrier continuity equations. Due to type-II conduction band alignment at the InP/GaAsSb interface, electron injection through the heterojunction is described by thermo-ionic field emission. To save computer time, the simulation domain is limited to half a device with an emitter area of 2×30 µm².

As experimental features of the heavily carbon-doped $GaAs_{0.51}Sb_{0.49}$ base is one of the key points to implement realistic simulation, the influence of unknown sensitive GaAsSb parameters were studied [7]. Indeed, fitting the Gummel I-V characteristics of real transistors has allowed to precise:

- the bandgap narrowing and its sharing between the valence and conduction band discontinuities of the heterojunction,
- mechanisms of electron-hole recombination in the base,
- a typical value of carrier minority lifetime.

Finally, the physics of DC current gain drop at high collector density current was studied.

As the DHBT DC current gain strongly depends on the conduction band alignment at the InP/GaAsSb interface, the effective band gap energy of the GaAsSb is implemented as an adjustable parameter. The theoretical value E_{Gth} of 0.72 eV for $GaAs_{0.49}Sb_{0.51}$ energy band gap at 300K was found to have to be reduced by 70 meV.

B. Transport analysis and optimization

The preeminent influence of SRH bulk recombination into the p-GaAsSb base on the current gain was confirmed [8]. To estimate the associated minority carrier life time, τ_n, forward Gummel characteristics were simulated for different τ_n values and compared to the measured ones with GaAsSb recombination centers located at mid gap. As shown in figure 3, the simulated forward Gummel plots are in good agreement with the measured values for $\tau_n \approx 0.5$ ns.

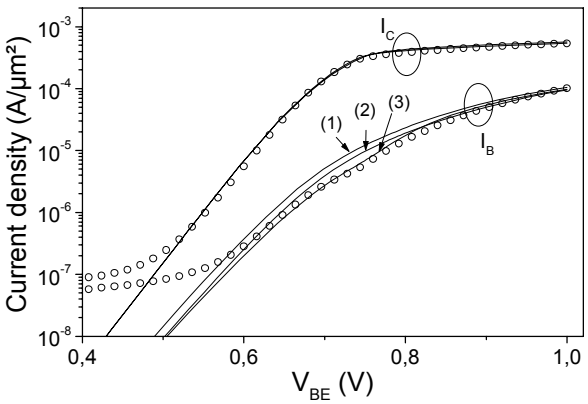
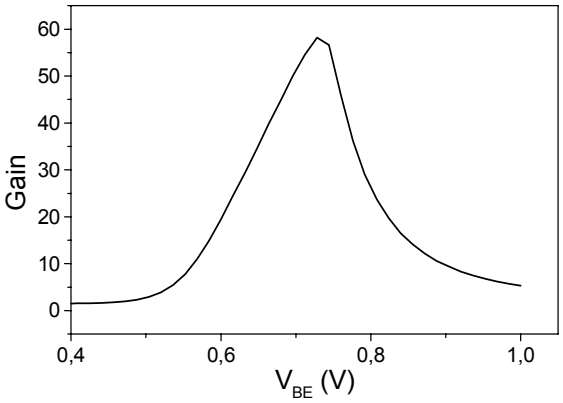


Fig. 3: Measured (o) and simulated (solid lines) base and collector current densities versus V_{BE} for V_{CB} = 0V and for different values of electron life-time in the base: τ_n = 0.05 ns (1), τ_n = 0.25 ns (2) and τ_n = 0.5 ns (3)

The evolution of DHBT current gain, β, with respect to biasing is shown in figure 4. A sharp drop of β is observed for V_{BE} >0.73 V and collector current density about 30 kA/cm². Indeed, at high injection level, for J_C > 30 kA/cm², the large valence band discontinuity at the base-collector interface, i.e. ΔE_V in the range of 0.85-0.92 eV, prevents the injection of holes from the base into the collector. Hence, instead of the classical base push-out effect, a parasitic barrier builds up at the base-collector interface inducing two major effects [7]:

- Electrons injected in the collector are partly reflected back to the base, leading to the quasi-saturation of J_C .
- The base majority carrier concentration increases to maintain the quasi-neutrality, leading to the increase of the base recombination rate and hence the rise of the base current, J_B.



(b)

Fig. 4: Evolution of current gain versus V_{BE}

Finally, the results presented in [9] have shown the enhancement of the DHBT operation at high current density requires not only the optimization of intrinsic collector parameters but also the quality of the collector ohmic contact.

V. GaAsSb/InP Technology

Alcatel R&I self-aligned triple-mesa InGaAs/InP DHBT technology has already been described [10]. It has been slightly adapted to suit GaAsSb/InP DHBT structure: due

to its favorable type-II lineup, antimonide-based HBTs do not need the quaternary compounds currently used in InGaAs-based HBTs to suppress the conduction band spike at the base-collector junction; the associated two etching steps are no longer necessary, leading to a simpler and more reproducible process. Due to the associated dimensional control, the scaling needed to achieve still higher performances will be more easily achieved.

A. Large size transistor characterization

Large size transistors were fabricated for various characterization; in particular, static gain >30 and base sheet resistance ~800 Ω/sq were measured.

Micro-photoreflectance measurements (fig. 5) were successfully performed on a 1µm diameter spot on a large size HBT (50µm x 50µm emitter size).

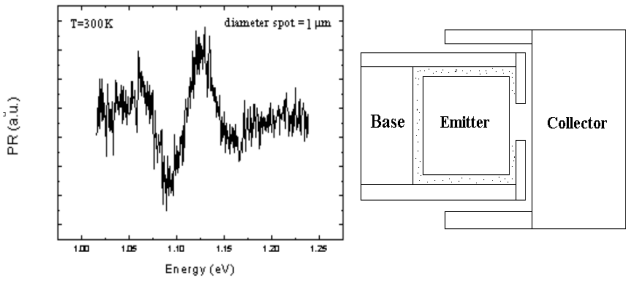


Fig. 5: Micro-PR spectrum recorded on a 1µm spot in the E-B spacing of a 50µmx50µm size emitter TBH

This allowed to optically determine the internal electric field at the emitter-base junction (about 75 kV/cm) [11].

Localized optical characterization has been done on HBT under biasing [12]; figure 6 presents micro-PR spectra for two biasing conditions.

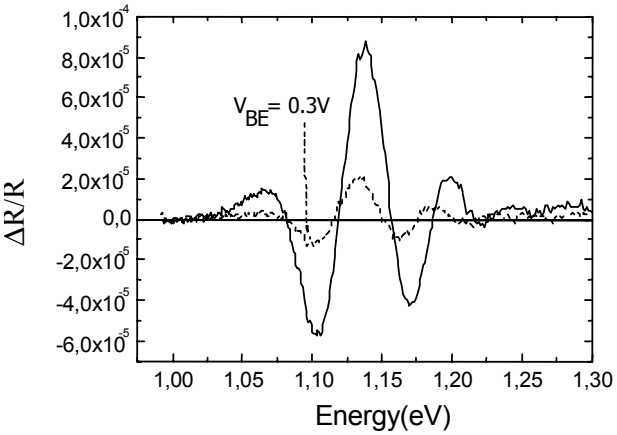


Fig. 6: Micro-PR spectra for V_{BE}=0 V (solid) and 0.3 V (dashed) biasing

This kind of characterization opens the way to E/B junction optimization w.r.t. base composition.

B. Low resistivity base contact

Pt-based ohmic contact has been intensively studied for reliable, low resistive and non-diffusive base contacts. Pt/Ti/Pt/Au (15/20/30/50 nm) contacts show extremely low resistivity on p-doped GaAsSb layers ($\rho_c < 10^{-6}$ Ω.cm^2) for which conventional TLM measurements lead to large uncertainties. An alternative method, called Floating Contacts Transmission Line Modeling (FCTLM) has been developed [13]. Using this method, reliable parameters have been extracted from Pt-based ohmic contacts on p-doped GaAsSb (N_A=3.6x10^{19} cm^{-3}). In agreement with the favorable Fermi level pinning reported above, the contact resistivity has been found as low as ρ_c = 8.2x10^{-7} Ω.cm^2, corresponding to a transfer length L_T = (330 ± 10) nm.

C. Micronic device fabrication and characterization

The self-aligned triple mesa technology allows to fabricate devices with 2-µm-width emitters (Fig. 7).

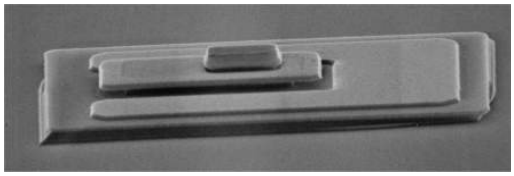


Fig. 7: 2 x 3 µm² GaAsSb DHBT microphotograph

Figure 8 shows the frequency characteristics for various emitter lengths. F_T and F_{MAX} reach 160 and 200 GHz respectively.

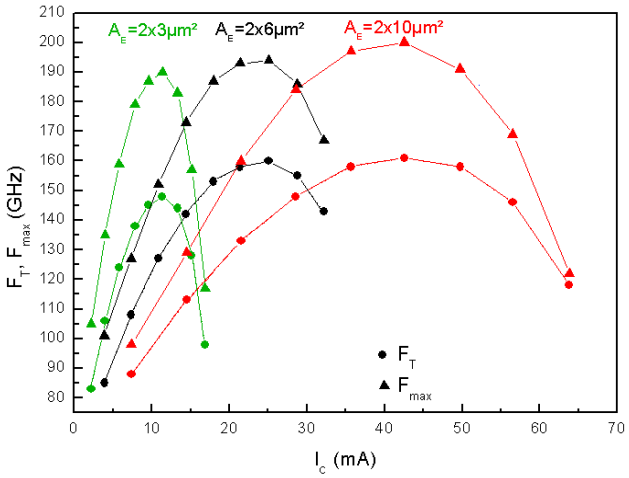


Fig. 8: Dynamic characteristics of 2 µm-width GaAsSb/InP DHBTs

VI. Circuit Design, Fabrication & Characterization

A circuit-oriented InP/InGaAs technology has been developed for very high bit-rate ICs fabrication [14] using HBTs with 2-µm emitter width, and including three Ti/Au interconnection levels, TaN resistors, MIM capacitors and spiral inductors.

This technology has been used, the only modifications in the process being those presented in section V.

In order to validate the suitability of this GaAsSb/InP HBT technology to address very-high-speed mixed-signal applications, we have chosen to use a Master-Slave D-Flip-Flop (MS-DFF), rather than more common but less relevant ring oscillator or static divider, as it operates at full-rate, on very wide band input.

The design of this DFF [15] is based on an ECL architecture, in order to operate at 40 Gbit/s with 40 GHz clock. It includes a sensitive buffer, two (master and slave) clocked latches and an output buffer. Compact and symmetric layout is a key to achieve high quality output signal.

Figure 9 shows the microphotograph of the circuit fabricated using this GaAsSb-based technology.

Measured fabrication yield is 77% on a two-inch wafer.

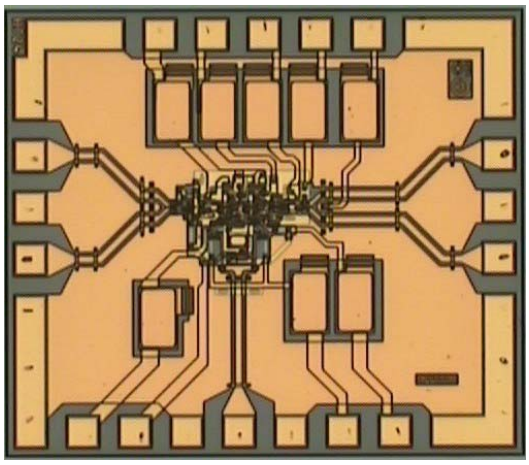


Fig. 9: 40 Gbit/s (40 GHz-clock)
GaAsSb DHBT D-FF microphotograph

Excellent functional characteristics have been achieved, as appears on figure 10. These include:

- S/N>19 (85% vertical eye opening)
- 500mV output swing and
- < 0.5 ps RMS jitter (88% horizontal eye opening).

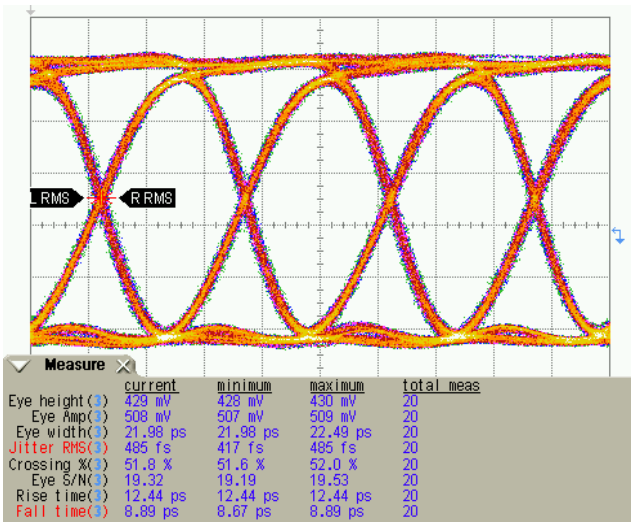


Fig. 10: 40 Gbit/s (40 GHz-clock) GaAsSb DHBT
D-FF eye diagram (100 mV/division)

VII. Conclusion

Based on an in-depth physical analysis of GaAsSb material and GaAsSb/InP heterojunctions, simulations have allowed to define and optimize a GaAsSb/InP DHBT device structure. All structures were realized using GSMBE epitaxy. The DHBT structure has been optimized for 40 Gbit/s digital IC fabrication. Using a triple-mesa self-aligned micronic HBT technology, 40 Gbit/s (40 GHz clock) D-Flip-Flops have been fabricated, validating the full process (from epitaxy to circuit). As using antimonide-based HBTs leads to a more robust technology, this approach has great potential for future scaled (submicron) HBT technology suitable for very high performance circuit fabrication.

Acknowledgement

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