Design and Fabrication of Short Gate-Length Heterostructure Charge Coupled Devices for Transversal Filter Applications

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***Abstract* — This paper presents the first reported quarter-micron double delta doped AlGaAs/ InGaAs charge coupled device for microwave filter applications. The design and fabrication of conventional and multi tapped delay line MMICs for RF filter applications are also discussed. Schrödinger and Poisson's equations are self consistently solved with current continuity equations to show the variation in channel charge concentration as the gate voltages are varied. The device is implemented as a recessed capacitive gate structure which is fabricated using established GaAs heterostructure MMIC technology to ensure good repeatability.**

I. Introduction

Since the advent of the charge coupled device (CCD) back in the 1970s, their application in various fields has increased tremendously. AlGaAs/InGaAs based CCD heterostructures, with 0.5×100μm fingers, have been demonstrated [1] to have many advantages over earlier silicon and GaAs structures because of their higher low-field mobility and saturation velocity. The upper limit frequency operation of a modulation doped CCD was found to be limited by the electron saturation velocity [2]. CCDs based on this technology could be used as electro-optic detectors or as microwave frequency filters. Such devices play an important role in the miniaturization of future handheld devices due to the ease of their integration with current MMIC GaAs technology. This paper presents an AlGaAs/InGaAs/GaAs CCD device with quarter-micron finger lengths, offering superior performance and high operating frequencies comparable with previously reported devices.

CCD device structures can be divided into two categories; resistive gate CCDs and capacitive gate CCDs. Capacitive gate CCDs with inter-electrode recesses which are described in this paper eliminate the need for having submicron (<0.5μm) inter-electrode gaps [3]. These inter-electrode recesses reduce the parasitic potential trough problem which occurs between gate electrodes, thus effectively increasing the charge transfer efficiency (CTE) of the device.

Split electrode structures were originally proposed in the late 1970s [4]. These structures were found to be an effective way to represent tap weight concepts used in digital filter theory. By varying the width of each split electrode, the value of the 'tap-weight' can be controlled. Various CCD transversal filters [5] based on MOS [6] and GaAs [7] technology have been investigated. Integrated microwave frequency transversal filters with input bandwidths of approximately 20 GHz [8] could be accomplished by the CCDs described in this paper.

II. Device Structure And Operation

The double delta doped CCD shown in Fig. 1 is a buried channel device which is an advancement of the structure in [1]. The band diagram of the device with no signal charge present and zero applied voltage is shown in Fig. 2.

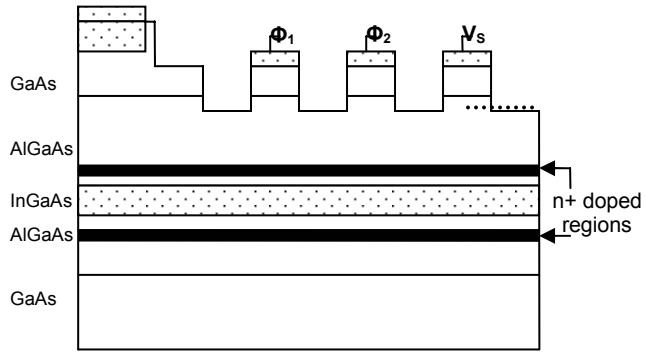

Fig 1. The side schematic of the charge coupled device. The transport channel is an undoped InGaAs (pseudomorphic) layer.

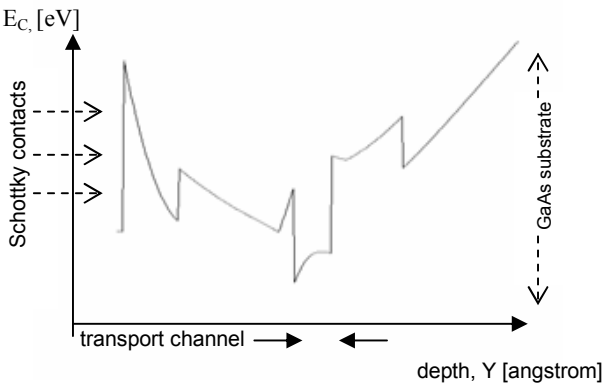

Fig 2. Conduction band diagram of the structure in Fig 1.

The length of the gate electrode is 0.25µm and its chosen width is 100µm. The length of the inter-electrode gate gap is 1.75µm. The quarter micron gates described in this paper are ideal for rapid charge transfer (by large fringing fields and thermal diffusion) making them optimum for high frequency operations. If the gate length is too large, the charge transfer time will be severely limited by thermal diffusion thus causing the maximum clock frequency to be reduced.

The InGaAs transport layer is sandwiched between two AlGaAs spacer layers for increased mobility of the carriers. The first n-type doped (~>10^{18} cm^{-3}) AlGaAs region is located above the first spacer layer and the second doped layer is buried below the second spacer region. The device is completed with ohmic contacts at the beginning and at the end of the doped areas. Charge confinement in the transport layer is important to ensure high charge transfer efficiency in the device.

Neglecting channel quantization and setting signal charge density as Q, an approximation for the channel potential is derived as:

$$V_{CH} = \frac{q(N_{d2}d_7 + Qd_5)(d_1 + d_2 + d_3 + d_4)}{\varepsilon} + \frac{qN_{dd}d_1^2}{2\varepsilon} + \frac{qN_{d1}d_3}{\varepsilon}\left(\frac{d_3}{2} + d_1 + d_2\right) + V_G - \phi_B + \Delta E_C \quad \textbf{(1)}$$

where d_1 is the thickness of the doped GaAs layer, d_2 is the thickness of the undoped AlGaAs layer, d_3 is the thickness of the first doped AlGaAs layer, d_4 is the thickness of the spacer layer, d_5 is the thickness of the transport layer, d_7 is the thickness of the buried doped AlGaAs layer, Φ_B is the Schottky barrier height and ΔE_C is the conduction band discontinuity. From equation (1), it is shown how the channel potential is dependent on the applied gate voltage and doping levels.

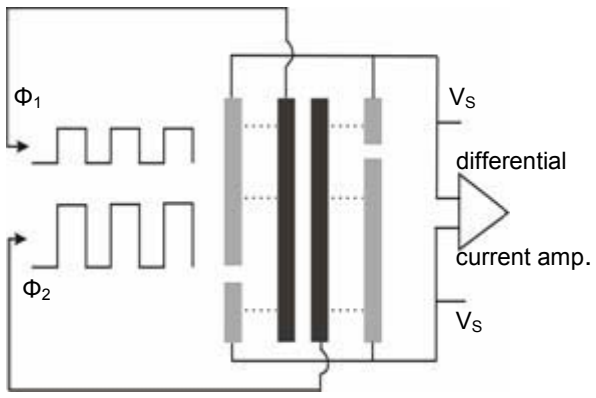

Fig. 3. Sample schematic drawing of the split electrode CCD structure with applied clocking signals.

Charge packets are transferred along the CCD described in Fig. 3 by applying clock signals to the gates denoted by Φ_1, Φ_2, and V_S. The split electrodes (tap weights) are held at fixed dc bias, V_S. Φ_1 and Φ_2 are clocked in phase but a higher voltage is applied to the electrode of Φ_2 resulting in a bigger potential well beneath gate Φ_2. The charge packets would be transferred throughout the device by alternating the applied clock voltages. The transfer of the charge packets would be similar to that of a shift register. Each half of the split electrode would be connected to the negative and positive input of a differential current amplifier. Through the summation process in the differential current amplifier, charge packets are then non-destructively sensed as they pass through the CCD structure. This entire differential summing operation which would require multiple digital chips to perform would then be simplified into a single CCD clock cycle.

A charge transversal filter requires multiple delay stages which are multiplied with weighting coefficients. A single delay stage represents one clock cycle of the CCD. The applied signal is non-destructively sampled at each stage via the split electrode structure described above. Hence, a wide variety of filter responses can be realized by changing the CCD's metallization patterns.

III. Device Modelling

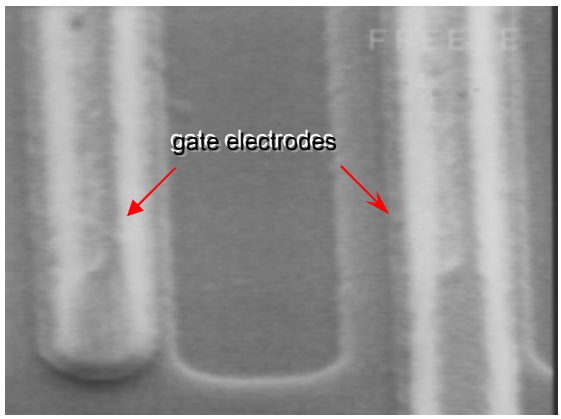

Fig. 4. SEM photomicrograph of two gate electrodes separated by a recessed gap.

The region of the physical structure shown in Fig. 4 was simulated using a modified version of the Leeds Physical Model (LPM) [9, 10]. The LPM is based on a quasi two dimensional pHEMT model. The input data includes information about the process, the delta doping levels in the structure, and the cross-sectional geometry. This model self consistently solves two dimensional Poisson-Schrödinger equations with energy conservation and current continuity equations for the active region shown above. As the model is based upon a fast, accurate and robust solution algorithm, the simulation time is extremely short and can be completed within minutes on a personal computer.

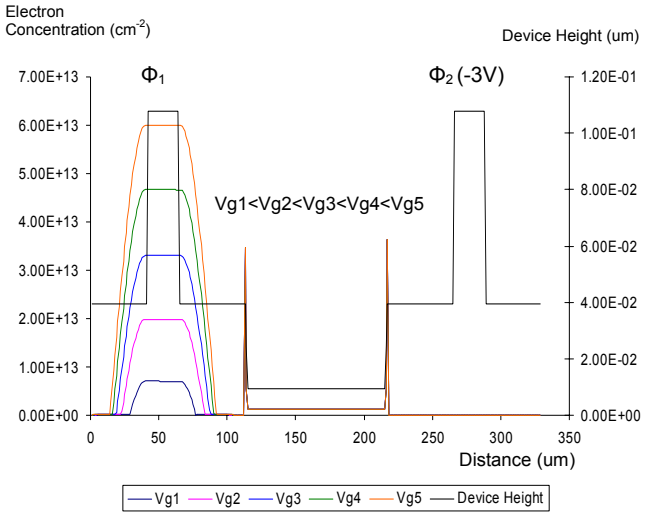

Fig. 5. LPM simulation of the signal charge in the channel of a dual-gate CCD with varying voltages at gate Φ_1. Gate Φ_2 is held at -3 [V]. Vg5 is the most positive voltage with Vg1 being most negative.

By modelling the CCD as a dual gate pHEMT and referring to the area of interest defined in Fig. 4, it can be seen how the electron concentration in the channel varies as different voltages are applied to gate Φ_1 (Fig. 5). No signal charge exists beneath gate Φ_2 because the voltage at that gate is held at a negative potential (-3V) beyond the pinch off voltage of the device. It can be seen from Fig. 5 how the signal charge is effectively isolated at gate Φ_1 from gate Φ_2 when a positive voltage is applied to the first gate. The increase in the signal charge concentration as the gate voltage increases clarifies the concept of charge transfer and how it is controlled by varying the applied gate voltages

IV. Device Fabrication

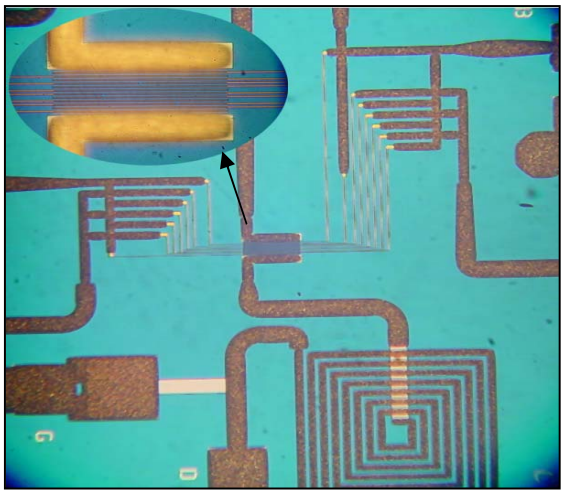

Fig. 6. Actual layout of the split electrode test array CCD MMIC with emphasis on the split electrode CCD structure.

Filtronic's 0.25µm pHEMT process was used to fabricate the two different MMICs. The process was modified to allow for multi gate structures with inter-electrode recesses and split electrodes. The size of the actual 'split electrode delay line', shown centrally in Fig. 6, is only 100µm x 50µm. The entire test layout is 1.6mm x 1.6mm**.** Bias pads are located at specific points in the MMIC to allow for ease of integration with periphery devices for testing purposes. Biasing circuitry (decoupling capacitors and inductors) are also included. The delay line response is being characterized using an automated temperature controlled probing station setup.

Fig. 7. SEM photomicrograph of the gap in the split electrode test structure. Gap size is approximately 1µm.

The final fabrication result is extremely accurate as seen in Fig. 7, where the specified gap size of 1µm is fabricated with just ~0.01µm error. Fig. 8 shows the ability of the 0.25µm process to produce a uniform multi gate structure over a large area. This is extremely important to ensure a reproducible and predictable filter operation.

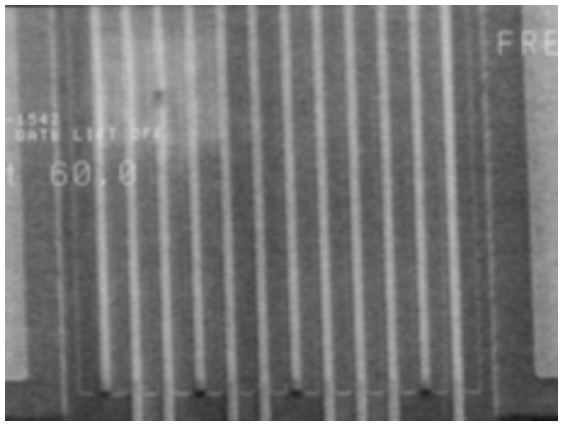

Fig. 8. SEM photomicrograph of the CCD array. Notice the uniformity of the gate gaps and electrodes due to the fabrication process.

V. Conclusion

Prototype pseudomorphic AlGaAs/InGaAs CCD delay lines and split electrode CCD structures have been fabricated. The devices presented here have the shortest gate length charge coupled device ever fabricated on such a modulation doped CCD structure. It is also shown that by using the LPM, a reasonable estimate of the pinch off voltage of the device as well the maximum capacity of

the potential wells beneath each storage gate may be obtained. The two different double delta doped CCD heterostructures presented in this paper will therefore be useful in the development of an integrated microwave frequency transversal filter.

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