High Gain 110-GHz Low Noise Amplifier MMICs using 120-nm Metamorphic HEMTs and Coplanar Waveguides

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***Abstract*—this paper presents the design and performance of 110-GHz low noise amplifier MMICs, based on coplanar technology, and utilizing 120-nm gate-length Metamorphic HEMTs. Thanks to a cascode device, a single-stage amplifier achieves 8-dB small signal gain, with less than 4-dB noise figure at 105 GHz, within a chip size of only 0.725 mm^2. The 2- and 3-stage LNAs exhibit small signal gains of more than 15- and 22-dB, respectively over the 100-115 GHz frequency range, with associated measured noise figures of 4.5 dB at 105 GHz; the chip area for these circuits are less than 2- and 3 mm^2. To the author's knowledge, these results are amongst the lowest noise figures reported to date for uniplanar amplifier MMICs operating at these frequencies.**

I. Introduction

Progress in Indium Phosphide-based (InP) high electron mobility transistors (HEMTs) have enabled the fabrication of millimeter-wave integrated circuits for passive and active imaging, and radar systems in the upper W-band (94 GHz and beyond). As in many others, these systems require low-noise amplifiers (LNA) MMICs with high gain, wide bandwidth and low power consumption. In order to address these applications, InP and Metamorphic HEMTs have been the subjects of constant developments over the last decade, due to their excellent transport properties, and superior performance, especially at millimeter-wave frequencies in comparison to GaAs PHEMTs (e.g. [1-2]). However, compared to InP substrates, metamorphic technology is less expensive [1-3], and thus found to be more and more considered by III-V semiconductor foundry manufacturers [3].

In this paper, we report on the performance of high gain 110-GHz low noise amplifier MMICs based on 120-nm Metamorphic HEMTs and coplanar technology. Despite of their rare use, coplanar waveguides (CPW) are very attractive at millimeter wave frequencies compared to microstrip technology due to:

- a simplified fabrication process, alleviating the necessity for wafer thinning, backside metallization and via-hole processing,
- the higher isolation between adjacent lines, and low dispersion characteristics,
- the compatibility of CPW MMICs with flip-chip assembly and packaging, among other advantages [4,5].

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II. MMIC process and technology

The W-band amplifier MMICs were fabricated with a fully passivated 120-nm T-gate Metamorphic HEMT technology developed by UMS in the frame of the ESA-ESTEC contract n° 15909. The epitaxial growth features an InAlAs/InGaAs/InAlAs structure with graded channel, which the Indium content varies from 53- to 70 %. Layers were grown by Molecular Beam Epitaxy on 4-inch GaAs substrates. This process exhibits typically the following DC and RF characteristics: an extrinsic transit frequency f_T of 200 GHz at 1.5-V drain bias, a maximum RF transconductance G_m in excess of 1000 mS/mm, a maximum drain current density I_{dmax} of 700 mA/mm, and 4.5-V gate-drain breakdown voltage at 1 mA/mm. The MMICs are designed on 635-µm thick substrates, with two gold metallization levels, 30 Ω/square TaN resistors, 330 pF/mm^2 SiN MIM capacitors, and airbridges.

III. Circuit design

In order to minimize design complexity and chip area for higher module integration, while providing maximum gain in the W-band, the MMICs are based on cascode devices. Indeed, cascode devices feature approximately twice the gain of conventional common source FETs for nearly the same amount of coplanar device area [4]. The basic gain block consists of two MHEMT devices arranged in the modified cascode configuration described by Tessmann in [1], and illustrated in Fig. 1.

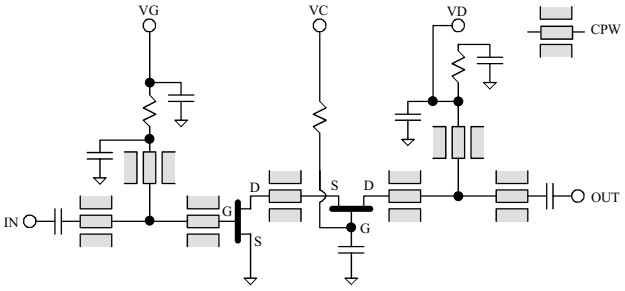

Fig. 1. Simplified schematic diagram of the single-stage coplanar W-band cascode amplifier block MMIC.

A. PHEMT device modeling and optimization

As active and passive element model description is critical at W-band frequencies, much effort was spent on devices modeling. At the time of development, no

accurate FET device models were available in coplanar environment: the common source FET device and noise parameter models were derived from the characterization of few *microstrip* transistor devices (i.e. with ground vias and different layouts) up to 50-GHz for S-parameters, and 18-GHz for noise measurements. From the evaluation of a scalable intrinsic model, the parasitic element shell for the coplanar MHEMT was estimated to predict the performance at W-band based on earlier work [4-6]; despite of more accurate models, the cascode configuration was represented in the simulation tool as a simple common source (CS) FET model (Fig. 2) connected to one common gate (CG) device model; the same model with swapped gate and source, being used for the common gate device.

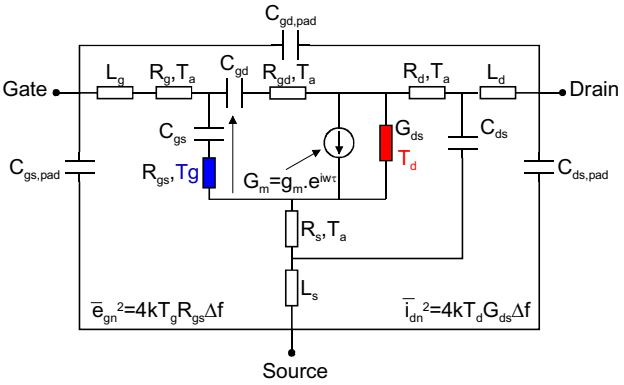

Fig. 2: The small signal equivalent common source FET model with noise sources used for the 120-nm MHEMT devices.

From the preliminary characterization of microstrip MHEMT devices, it could be estimated, that the best compromise between noise figure and gain can be obtained near 1-V drain voltage with approximately 350 mA/mm drain current. Thus, the single device gate width, and the number of gate fingers were optimized for minimum noise figure at the highest associated gain. This resulted in optimum device of 2×20 µm CS FET connected to a 2×20 µm CG one. The noise figure model is based on the temperature noise description of Pospiezalski [7]. This model compatible with the above small signal equivalent circuit, enables to represent the noise dependence through only two parameters T_g and T_d, being respectively the equivalent noise temperatures of the gate-source R_{gs} and drain-source R_{ds} resistances. All resistive elements have an equivalent noise temperature of T_a=298 K (room temperature), except the channel conductance G_{ds}, which has a higher equivalent noise temperature estimated to approximately T_d≈2000 K at 350-mA/mm drain current. Such estimates were later confirmed with W-band noise figure measurements up to 100 GHz, performed at Millilab – Finland: as shown in Fig. 3, for a 2×20 µm common source MHEMT biased at 1 Volt, a minimum noise figure of 3.1 dB is measured at 100 GHz and 175 mA/mm, whereas a bias of 375 mA/mm provide the highest associated gain with the lowest noise figure. For these biases, the extrapolated minimum noise figure for the single common device is around 4 dB and 4.5 dB at 110 GHz.

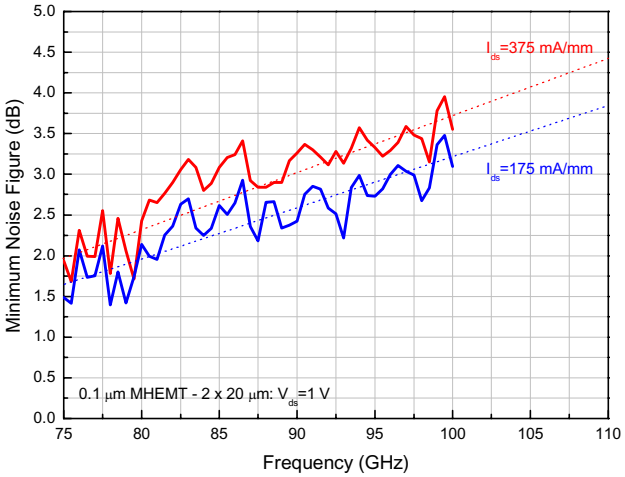

Fig. 3: Measured minimum noise figure (solid lines) for the common source 0.1×2×20 µm MHEMT device at V_{ds}=1 V, and I_{ds}=175..375 mA/mm. Simple extrapolation to 110 GHz is represented in dashed lines.

B. Coplanar line element and discontinuity models

Accurate passive element modeling is also essential at W-band frequencies. Although using conventional matching techniques, the passive circuitry simulation relies on an accurate coplanar element model library, derived from the characterization of passive test structures up to 120 GHz [6]. All CPW elements have a ground-to-ground spacing of 50 µm. These elements are an exhaustive suitable database for coplanar millimeter-wave integrated circuit design, enabling a wide impedance range of coplanar transmission lines (10-100 Ω) and associated discontinuities. The key in this coplanar device modeling approach is based on the combination of different sections of equivalent transmission lines [8]. For the CPW transmission lines with the cross sections depicted in Fig. 4, the electrical parameters such as characteristic impedance Z_c, effective relative dielectric constant ε_{re} and attenuation $\alpha=\alpha_{dc}+\alpha_{rf}f^n$, are accurately extracted from on-wafer measurements of different geometries and lengths.

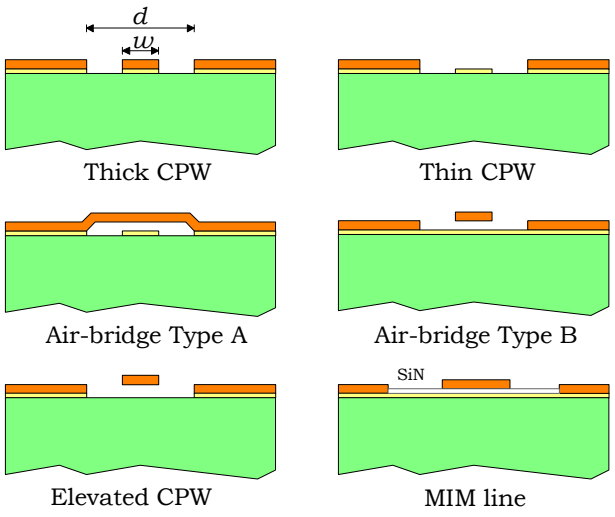

Fig. 4: Different possible configurations of coplanar waveguide transmission lines using two interconnect metallization levels.

Geometries and corresponding parameters for some conventional CPW lines using the stack of the two available metallization levels (i.e. Thick CPW in Fig. 1) and covering the useful range of characteristic impedances are summarized in Fig. 5 [6].

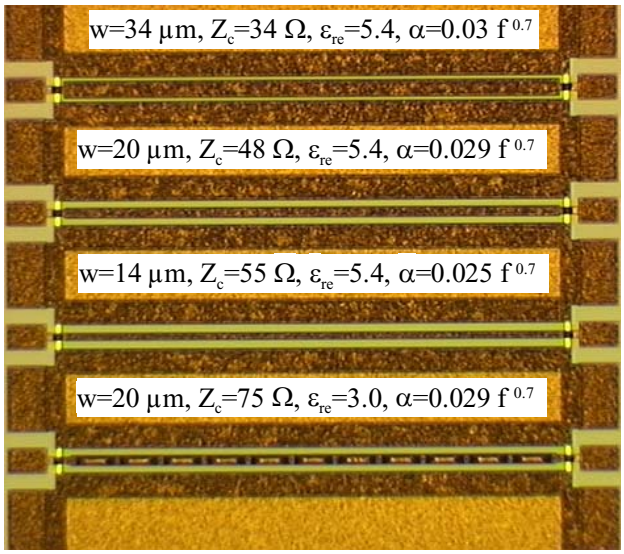

Fig. 5: Example of coplanar line test structures (thick CPW) with 50-µm ground-to-ground spacing and associated extracted models (high impedance elevated or "air-bridge" CPW line with posts at bottom).

A rigorous methodology was used for the design of the coplanar MMIC low noise amplifiers: Optimum noise source match and power transfer were considered in the optimization of gain, bandwidth, and noise figure. In order to achieve compact size, the bias networks were directly integrated into the T-matching networks, and the interstage was optimized for direct impedance transformation. Circuit stability was also of primary concern: source feedback on the first common source device was used to stabilize the LNA, in combination with large on-chip bypassing capacitors, and appropriate out-off band resistive loading for the best trade-off between noise figure and gain. This resulted in the unconditional stability of the amplifier over the entire frequency range.

The single-stage MMIC amplifier is shown in Fig. 6. It is based on the topology of Fig. 1. Although first and second gates can be individually adjusted for gain, noise figure and power control, in order to be operated from a single drain supply (self-bias), the circuit incorporates a resistive divider at the second-stage gate. This feature is done taking advantage that maximum transconductance for the MHEMT process occurs at a gate-source voltage near 0 Volt. The circuit was designed targeting small chip area so that it can be used as general buffer amplifier in W-band transmit/receive ICs. Most elements were folded as much as possible, resulting in total chip area of less than 0.73 mm^2. This remarkable small chip size can be even less if one only considers the functional area (approx. 0.5 mm^2). The 2- and 3-stage amplifier MMICs were designed by cascading similar individual gain cells, slightly differently optimized however for larger bandwidth (see further).

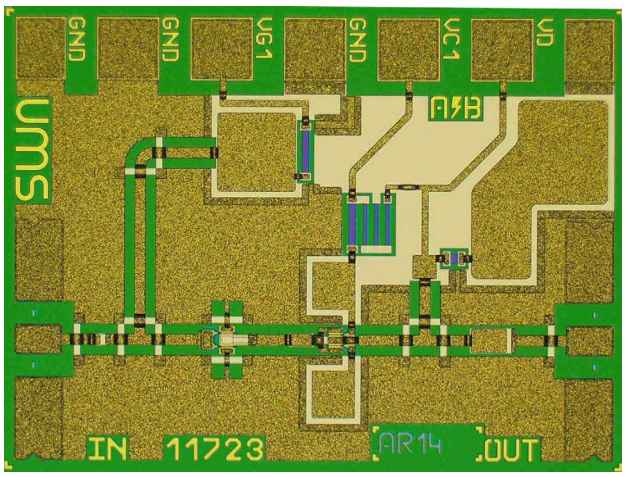

Fig. 6: Chip photograph of the single-stage coplanar low noise amplifier cascode MMIC (chip size is 0.99 × 0.73 mm^2).

IV. Measured Performance

A. Single-stage 100-120 GHz amplifier MMIC

Fig. 7 shows the typical on-wafer small signal S-parameters and measured noise figure for the single-stage LNA. At a nominal drain voltage of 2 V (cascode FET, let V_{d1}≈1V), and for a total current of 15 mA (375 mA/mm), the LNA demonstrates more than 7-dB gain (S_{21}) from 100- to 120 GHz, with a peak gain of 8 dB at 110 GHz. At this frequency, the input- (S_{11}) and output- (S_{22}) return loss are below -15 dB and -20 dB respectively. The reverse isolation (S_{12}) is better than -18 dB over the whole frequency range. Yet, at the same bias conditions, the noise figure could be measured up to 105 GHz with the millimeter noise-figure measurement system of the Fraunhofer IAF-Freiburg, with values of 4 dB at this frequency. These results are in excellent agreement with the expected noise figure for a single 2 × 20 µm 120-nm MHEMT shown in Fig. 3.

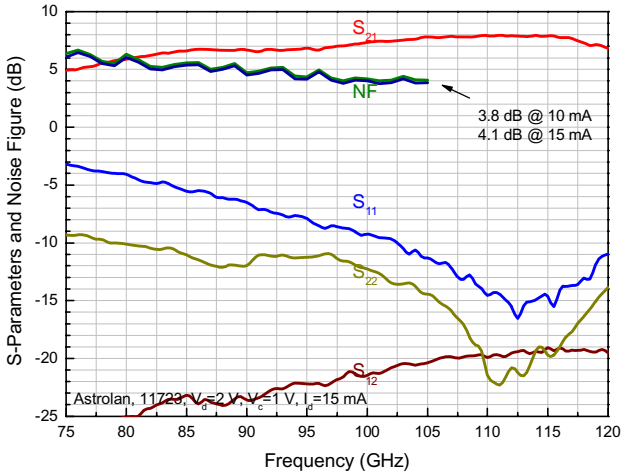

Fig. 7: On-wafer measured S-parameters and noise figure of the single-stage LNA MMIC at V_d=2 V, V_c=1 V, and I_d=15 mA.

B. Two-stage 100-120 GHz amplifier MMIC

A Chip photograph of the 2-stage MMIC is shown in Fig. 8. The Fig. 9 shows its small signal S-parameters and noise figure. The amplifier exhibits more than 15-dB gain over 100- to 115 GHz, and a noise figure of 4.4 dB at 105 GHz, with excellent input- and output return loss at this frequency, i.e. < -15 dB at 110 GHz.

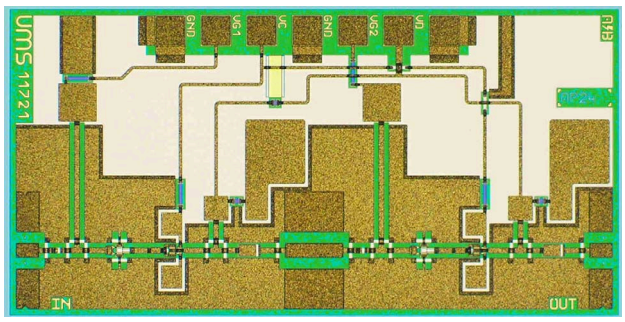

Fig. 8: Chip photograph of the 2-stage coplanar LNA (chip size is 2.0 × 1.0 mm^2).

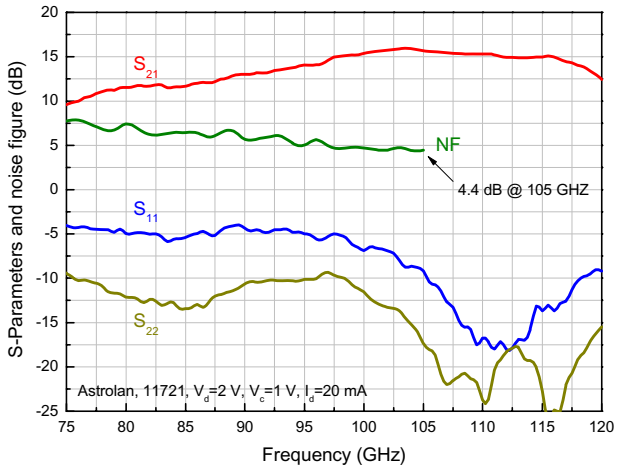

Fig. 9: On-wafer measured S-parameters and noise figure of the 2-stage LNA MMIC at V_d=2 V, V_c=1 V, and I_d=20 mA.

C. Three-stage 100-115 GHz amplifier MMIC

Fig. 10 shows a chip photograph of 3-stage LNAs, and Fig. 11 shows the measured S-parameters and noise figure. A small signal gain of more than 22 dB is measured in the 97.5-115 GHz range, with 24-dB peak gain and 4.5-dB noise figure at 105 GHz. Again, these measured data are in excellent agreement with the single-device noise figure measurements presented in Fig. 3, slightly increased by the contribution from other stages.

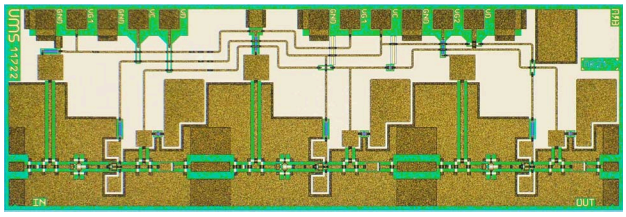

Fig. 10: Chip photograph of the 3-stage coplanar LNA (chip size is 3.0 × 1.0 mm^2).

Finally, it is worth mentioning that all measurements reported here were performed at typical simulated bias. Further improvement is possible with individual stage bias tuning: best results showed 0.5-dB additional gain per stage and 0.1-dB absolute reduction in noise figure. Recent published data for 100-nm gate MHEMT MMICs report an average noise figure of 3 dB and 10-dB associated gain in the lower 80- to 100 GHz frequency band [1]. The first pass 110 GHz designs and results presented in this paper show the high gain potential combined with the low noise performance of the 120-nm Metamorphic HEMT technology. Yet, better performance prediction is still possible with more accurate models for the coplanar active devices.

V. Conclusion

110-GHz low noise amplifier MMICs, based on coplanar technology, and 120-nm gate-length Metamorphic HEMTs were presented. By means of cascode devices, 8-dB small signal gain with less than 4-dB noise figure at 105 GHz was achieved on a single-stage amplifier for a chip area of only 0.73 mm^2. The 2- and 3-stage LNAs exhibit high small signal gains of more than 15-, and 22-dB, over the 100-115 GHz frequency range, with associated measured noise figures of 4.5 dB at 105 GHz; the chip area for these circuits are less than 2- and 3 mm^2.

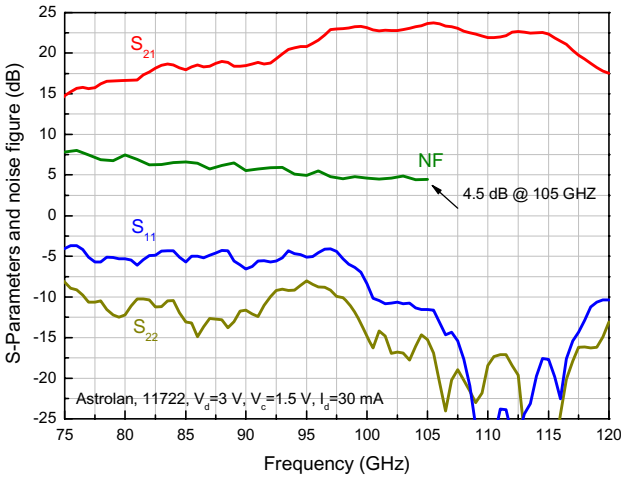

Fig. 11: On-wafer measured S-parameters and noise figure of the 3-stage LNA MMIC at V_d=3 V, and I_d=30 mA.

Acknowledgements

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