RLC Parasitic Extraction and Circuit Model Optimization for Cu/SiO_2-90nm Inductance Structures

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Abstract

An efficient interconnects modeling and optimization methodology is proposed for multi-GHz clock network design. High frequency effects, including inductance and proximity effects are captured. The results are validated through comparisons with electromagnetic simulations and measured data taken from a Cu/SiO_2 90nm process test chip.

1. Introduction

In today's multiple-layer interconnects design, clock distribution nets usually use thick top metal that is routed with large dimensions to reduce line resistance. Faster clock frequency and lower line resistance [1, 2] enhance interconnect inductive effects that now become a first order effect for global clock distribution design. The most accurate way of analyzing inductance effects in complex structures is to carry out wave/field equation analysis, which uses the measured S-parameters to get propagation constant, γ, and characteristic impedance, Z_c, of test structures. However, because of the dense inductance matrix involved for ever-complex structures, this method is computationally expensive and might also fail in some cases as in the case of on-chip spiral inductors. More efficient methodologies are preferred to enable fast optimization and physical design exploration in the design and simulation of complex networks. One major complication of inductance analysis is the difficulty in determining current return paths in advance. But in the case of clock nets, wires are highly optimized and usually have VDD/GND shields to provide close return paths and to limit signal line coupling. Also, wide lines are usually split into multiple fingers interspersed with VDD/GND shields in order to suppress inductive ringing, and reduce delay [3]. In these special cases, the current return loops are relatively well-defined or can be estimated with reasonable accuracy. Therefore, it is feasible to use a *loop-based* method, in which the entire signal and return loops of single or multi-line structures are modeled with equivalent loop resistances (*R-line*) and inductances (*L-line*).

In this paper, we propose new interconnect modeling approach based on equivalent circuit optimization methodology. This optimization is carried out using *OpSim* (Mentor Graphics optimization tool) on a very compact circuit model. The results are also obtained by solving wave/field equations applied on standard S-parameters measurement for comparison reasons. The proposed optimization model is also suitable for coupled lines characterization.

In section 2 a novel test structure is proposed for our study followed by wave equation methodology in section 3. The proposed optimization model is presented in section 4. Section 5 demonstrates measurement results and comparisons.

2. Novel interconnect test structure

More than 30 test structures have been dedicated for our study. These novel structures are designed to "mimic" interconnect configuration in modern IC-design. Ground plan is the dominant parameter in inductance characterization. Inductance value is highly affected by our choice of ground plans. In today's ASIC design, ground and supply lines are located on the very top metal layer for efficient design routing. In addition, top metal layers enjoy the lowest resistivity due to its relatively higher thickness than other metal layers.

With these observations in mind, top metal layer ground plane are used in our inductance test structure as shown in Fig. 1. Crossed horizontal and vertical lines form inductance ground plan grid. Different grid density (i.e. lines separation, S, or lines width, W) are implemented for technology characterization purposes. Also, different signal line widths should be investigated on various metal layers.

For test structure set completion, a standard surface structure is also considered as shown in Fig. 2.

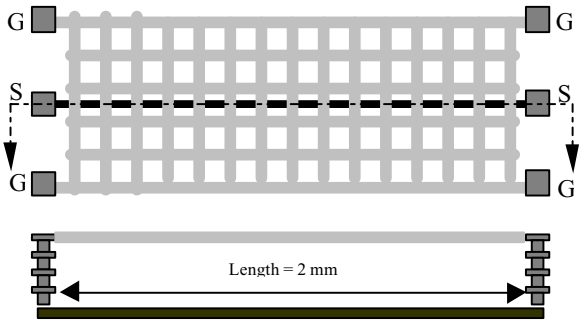

Figure 1. Interconnect structure under study, top view and cross-section.

Figure 2. Standard single line surface structure.

Ground-Signal-Ground, GSG, infinity probes along with Vector Network Analyzer and Thru-Reflect-Line (TRL) Calibration technique are used at frequencies from 45MHz to 20GHz.

An open-circuit structure is included for PAD parasitic de-embedding as shown in Fig. 3.

Figure 3. Open circuit test structure.

It is not necessarily that distance between the two probes is the same as the structure length (2mm), but it should be long enough for accurate PAD capacitance removal.

3. Wave equation extraction method

PAD parasitic de-embedding is considered to be an essential procedure in this method. The procedure relies on subtracting the Y-parameters of the open circuit structure from the Y-parameters of the test structure to get the Y-parameters of the device under test, *DUT* [4]. This step will need S to Y Matrix parameters conversion taking into account the probe matching impedance used in S-parameters measurement.

The second step is to convert the *DUT* Y-parameters into Transmission matrix, *T*, (*A*, *B*, *C* & *D* parameters). The entire Matrix conversion processes can be performed by hand calculation or using any mathematics software package. From the transmission parameters, propagation constant, γ, and the characteristic impendence, Z_c can be calculated as follows:

$$\gamma = \frac{\cosh^{-1}(T_{11})}{Len} \qquad (1)$$

$$Z_c = \frac{50 \times T_{12}}{\sinh(\gamma \times Len)} \qquad (2)$$

where *Len* is the structure length, T_{11} is the first row-first column element of the DUT transmission matrix; T_{12} is the first row-second column element of the *DUT* transmission matrix.

From γ and Z_c calculations, standard RLCG transmission line model can be implemented at each frequency as shown in Fig. 4.

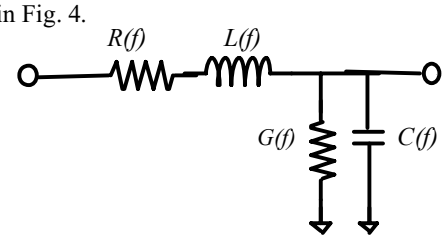

Figure 4. Standard *RLCG* transmission line representation.

From Eq. (1) & (2), we can calculate the *R, L, C* and *G* value at scanned frequencies as follows:

$$R = \mathrm{Re}(\gamma \times Z_c) \qquad (3)$$

$$L = \frac{\mathrm{Im}(\gamma \times Z_c)}{\omega} \qquad (4)$$

$$G = \mathrm{Re}\left(\frac{\gamma}{Z_c}\right) \qquad (5)$$

$$C = \frac{\mathrm{Im}\left(\frac{\gamma}{Z_c}\right)}{\omega} \qquad (6)$$

Calculations of *R*, *L*, *C* and *G* at all the frequency range available in our S-parameters measurement (from 45MHz to 20GHz) is shown in Fig. 5.

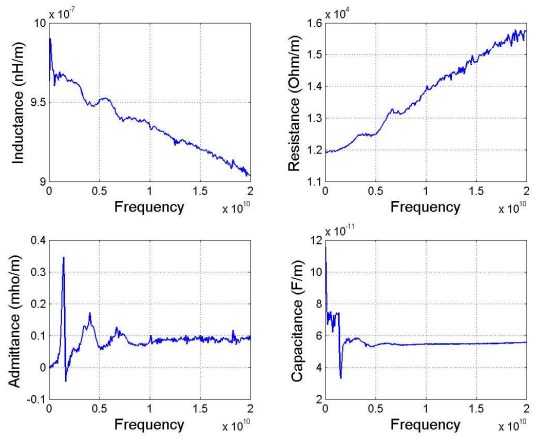

Figure 5. RLCG variation with frequency for sample test structure.

Low frequency capacitance and admittance result suffer from some high ripples due to the dominating resistive effect at low frequency. Meanwhile, high frequency values are stable and constant as the capacitive and inductive effect are the dominating effects. It should be noted that proximity effect is highly observed above 10 GHz regimes. This observation should be reflected on the circuit model discussed in the next section.

De-embedding and transmission line characterization procedures are shown in Fig. 6.

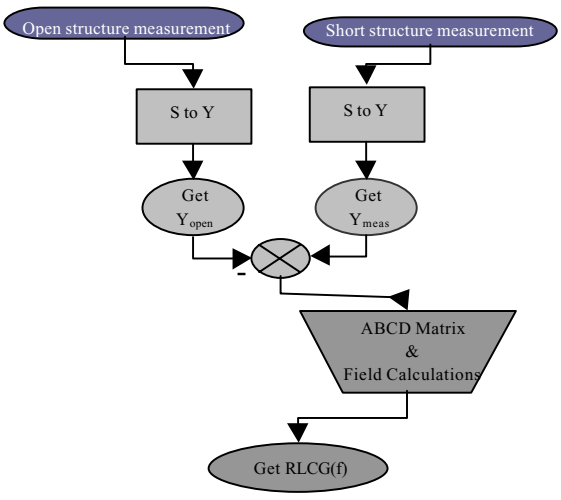

Figure 6. Wave equation method flow chart.

4. Circuit model optimization method

A physically-based circuit model can be developed to represent interconnect line under study. However, circuit element values should be carefully selected to truly characterize interconnects in modern simulators. Simple RLCG section can fit very well for a small frequency range. In practice, line resistance, *R*, and inductance, *L*, vary with frequency due to skin/proximity effects mentioned previously. Hence, the selected model should include frequency variation mechanism by element frequency coefficient or more complex circuit model. The model shown in Fig. 7 is adopted for its suitability to this study.

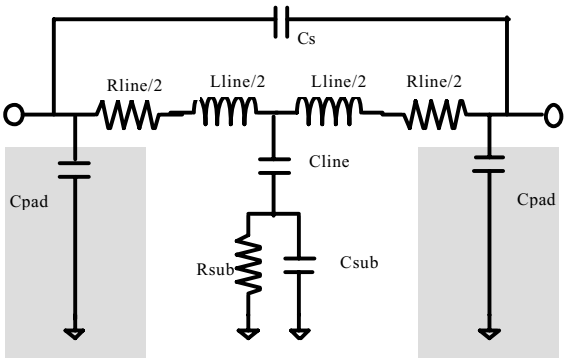

Figure 7. Circuit model for single interconnect line.

Here, Rsub and Csub represent the substrate losses, Cline is the line capacitance, Lline is the line inductance and Rline represents the line resistance. The shunt capacitance Cs is included in the model to account for frequency variation. The proposed model replaces the traditional transmission line RLCG model to suit the implemented structure.

Circuit model shown in Fig. 7 represents only the DUT portion of our test structure. However, Cpad should be added to the model (shown by shaded boxes in Fig. 7) at each end to represent PAD capacitance contribution. The optimization of Cpad will eliminate the need for the de-embedding procedure motioned in the wave equation technique.

Only seven parameters are included in our model, which enables almost any optimizer to obtain very good correlation with measured S-parameters of all structures under study. The optimized values fit all scanned frequency range from 45MHz to 20GHz. As an example, Fig. 8 shows S11 and S12 of both measured and optimized equivalent circuit drown on real/imaginary rectangular axis.

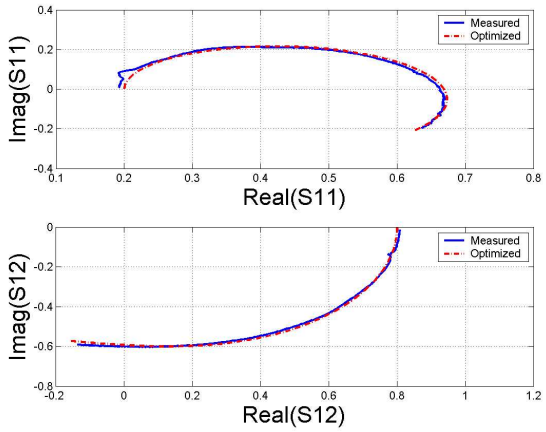

Figure 8. Rectangular plot of S11 and S12 for both measured and optimized circuit model.

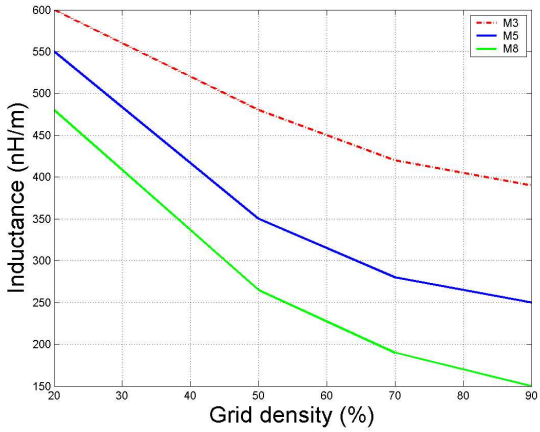

Figure 9. Inductance variation with different ground grid density.

As shown in Fig. 8, excellent correlation between the measured and optimized circuit S-parameters without the need for a de-embedding step for PAD parasitic removal. This is carried out by adding the C_{pad} element inside the proposed model. This correlation is repeated almost in all structures optimization in our study.

5. Results and Discussion

Our structures set included different ground lines grid density and also different signal metal layers. Table. 1 shows line inductance per unit meter for various structures obtained by wave equation method in comparison with optimization technique and Fast Henry results.

Table 1. Sample results of test structures compared to optimized circuit model and Fast Henry data.

Signal metal layer	Grid density	Inductance nH/m	Inductance Optimized nH/m	Fast Henry nH/m
M3	20%	600	608	613
M3	50%	480	477	467
M5	20%	605	590	603
M8	20%	480	502	572
M8	50%	265	272	328
M9	10%	900	915	900
M9	20%	760	779	772
M9	50%	520	529	537

Fig. 9 shows inductance variation on different grid density and metal layers.

As shown in Fig. 9, ground grid density has noticeable impact on inductance value of an identical dimension interconnect line. Grid density should be taken into account while used in recently developed inductance extraction tools.

6. Conclusion

A complete procedure to characterize and optimize Cu/SiO_2 90nm interconnect inductance test structure has been developed. Also, ground lines grid density impact on line inductance has n\been investigated. Coupled lines characterization can be realized following the same optimization technique taking into account partial inductance inside equivalent circuit model.

7. References

[1] T. N. Theis,"The future of interconnection technology", *IBM J.Rev, Develop. Vol. 44 No. 3 May 2000.*

[2] Ken Lee, "On-Chip interconnects- GegaHertz and Beyond", *Solid State Technology, No. 85-89, September 1998*

[3] Y. Massoud, S. Majors, T. Bustami, and J. White, "Layout techniques for minimizing on-chip interconnect self-inductance," *Proceedings 1998 Design and Automation Conference (DAC)*, pp.566-71.

[4] K. Beilonhoff, H. Klingbeil, W. Heinrich, H.L. Hartnagel; "Open and Short Circuits in Coplanar MMIC's." *IEEE-Trans. MTT. 41, 1993, pp. 1534-1537*