Extremely High Gate Turn-on Voltage of GaAs Double Camel-Like Gate Field-Effect Transistor

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Abstract — **Extremely high potential barrier height and gate turn-on voltage of a novel GaAs field-effect transistor with $n^+/p^+/n^+/p^+/n$ double camel-like gate structure are demonstrated. The maximum electric field and potential barrier height of the double camel-like gate are substantially enhanced by the addition of another n^+/p^+ layers in gate region, as compared with the conventional $n^+/p^+/n$ single camel-like gate. For a 1 x 100 μm^2 device, a potential barrier height up to 2.741 V is obtained. Experimentally, a high gate turn-on voltage up to + 4.9 V is achieved because two reverse-biased junctions of the double camel-like gate absorb part of positive gate voltage. In addition, the transistor action shows a maximum saturation current of 730 mA/mm and an extrinsic transconductance of 166 mS/mm.**

I. Introduction

GaAs-based field-effect transistors (FETs), such as metal-semiconductor FETs (MESFETs) [1, 2], doped-channel FETs (DCFETs) [3, 4], and modulation-doped FETs (MODFETs) [5, 6], etc., have been widely developed for digital circuit applications because of their simplicities and excellent device performances. However, the low gate turn-on voltage resulting from the low potential barrier height of Schottky gate severely affects the noise margin in inverter circuit applications [4, **7**]. On the contrary, high gate turn-on voltage can prevent the injection of channel carriers into the gate electrode and allow the drain output current to increase.

Over the past years, due to the pn depletion in gate region the $n^+/p^+/n$ camel-like gate FETs performing with high barrier heights were well investigated [8-11]. The camel-like gate also provides some advantages when compared with conventional Schottky gate, such as i) elimination of the metallurgical difficulties due to the ohmic contact, ii) relatively easy adjustment of the built-in voltage, and iii) the potential for improving reliability in adverse environments and under high power dissipation conditions [8]. Recently, we have fabricated and demonstrated n- and p-channel camel-like gate pseudomorphic MODFETs (pMODFETs) [10, 11]. A gate turn-on voltage larger than 1.7 V (2V) was achieved which can be attributed to the pn depleted junction and the presence of large conduction (valence) band discontinuity at InGaP/InGaAs heterostructure for the n-channel (p-channel) pMODFET.

In this article, a novel GaAs $n^+/p^+/n^+/p^+/n$ double camel-like gate FET exhibiting extremely high potential barrier height and gate turn-on voltage is fabricated and demonstrated. The high gate turn-on voltage increasing the forward gate operation voltage and input voltage swing is suitable for linear and signal amplifiers and inverter circuit applications [4, 10]. The electric-field distributions and energy-band diagrams of the single (conventional) and double (studied) camel-gate devices are investigated and compared. As compared to the conventional camel-gate devices, the potential barrier height and gate turn-on voltage are enhanced efficiently by the addition of another thin n^+/p^+ layers in middle region of the camel-like gate.

III. Decvice Structure and Experiments

The double camel-like FET was grown by low-pressure metal-organic chemical-vapor deposition (LP-MOCVD) on an (100)-oriented semi-insulating GaAs substrate. The layer structures consist of a 0.2 μm GaAs undoped buffer layer, a 0.1 μm n = 5 x 10^{17} cm^{-3} GaAs channel, a first 50 Å p^+ = 2 x 10^{19} cm^{-3} GaAs layer, a first 50 Å n^+ = 6 x 10^{18} cm^{-3} GaAs layer, and a second 50 Å p^+ = 2 x 10^{19} cm^{-3} GaAs layer. Finally, a 300Å n^+ = 6 x 10^{18} cm^{-3} GaAs cap layer was deposited. A mesa structure provided the required isolation. Drain and source ohmic contacts were formed by alloying evaporated AuGeNi metal at 400 ^{0}C for 30 sec. The ohmic gate electrode was fabricated by evaporating Au metal without the need for annealing. All the contacts were deposited on n^+-GaAs cap layer. After these contacts were formed, the sample was dipped in etching solution and the n^+-GaAs cap layer was partly recessed to avoid the gate-to drain (G-D) and gate-to-source (G-S) short. The schematic cross section of the device is revealed in Fig. 1.

III. Results and Discussion

Figure 2 shows the G-D current-voltage (I-V) characteristic of the studied FET. The gate reverse current was smaller than 0.1 mA at V_{GD} = -15.6 V. An extremely high turn-on voltage up to + 4.9 V at 0.1 mA is obtained. To our knowledge, the turn-on voltage is the largest value among of the GaAs-based FETs. In order to investigate the improvement of the double camel-like gate structure on the gate turn-on voltage, two devices denoted devices A (our double camel-like device) and B (conventional single camel-like device) are compared. Similar to the device A, only a 50 Å p^+ = 2 x 10^{19} cm^{-3} GaAs layer was added between n^+-GaAs cap layer and n-GaAs channel in the device B.

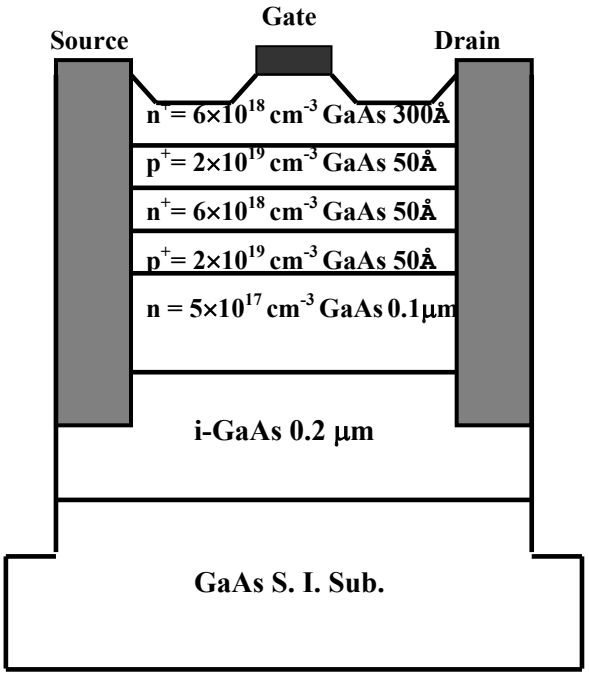

Fig.1. Schematic cross section of the experimental double camel-like gate FET. The gate dimension and the drain-to-source spacing were 1 x 100 μm^2 and 3 μm, respectively.

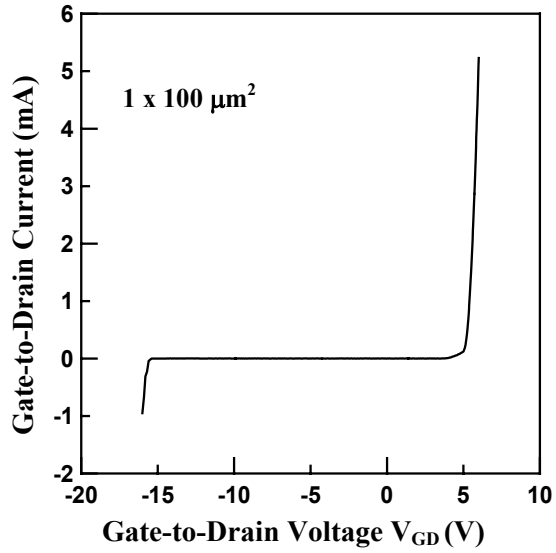

Fig.2. Experimental gate-to-drain current-voltage characteristic of the studied device with a gate dimension of 1 x 100 μm^2.

By solving Possion's equation, the electric-field distributions of the two devices are shown in Fig. 3. In the device A, the designed principle is that the thin $p^+/n^+/p^+$ GaAs triple layers must be completely depleted at equilibrium and under gate biases. Similarly, the thin p^+ GaAs layer of device B must be entirely depleted. With respect to the device A, four pn junctions are denoted as J1, J2, J3, and J4, respectively. It can be seen that the maximum positive electric field is substantially increased and another triangular-shaped positive electric-field distribution is formed by the addition of another n^+/p^+ layers in gate region as compared to the device B.

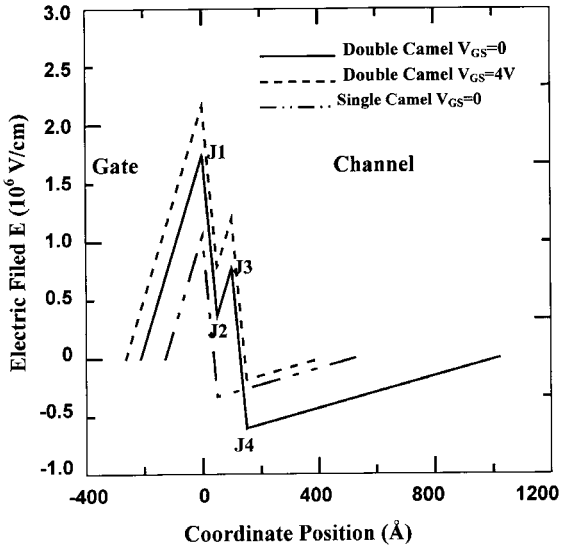

Fig.3. Electric-field distributions of the single and double camel-like gate FETs.

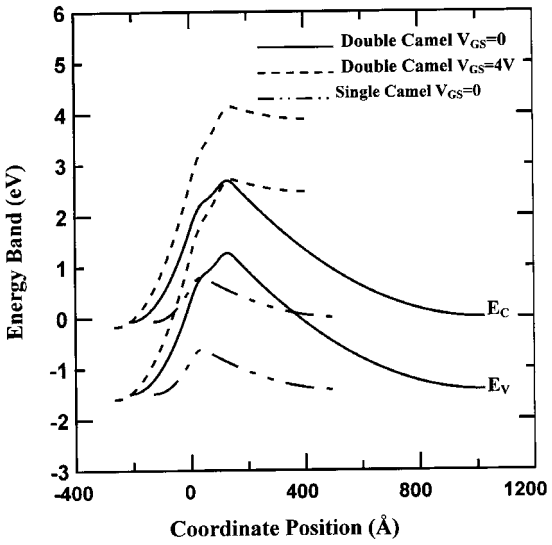

Fig.4. Corresponding energy-band diagrams of depletion region for the single and double camel-like gate FETs.

The energy band diagrams of depletion region for the devices A and B are illustrated in Fig. 4. Double camel-like gate is formed in the device A, while only a single camel-like gate is formed in the device B. At equilibrium, the potential barrier height up to 2.741 V is observed for the device A, while it is only 0.851 V for the device B. The second triangular-shaped positive electric-field distribution also helps to increase the potential barrier height, as seen in Figs. 3 and 4. It is worthy to note that the turn-on voltage (4.9 V) is larger by a factor of about 2 than the potential barrier height (2.7 V) at equilibrium. The detailed mechanism corresponding to the large gate turn-on voltage can be explained as follows.

As a positive gate voltage is applied, the J2 and J4 are forward-biased while the J1 and J3 are reverse-biased. Because the concentration of channel is lower than that of the $n^+/p^+/n^+/p^+$ heavy-doped camel-gate layers, the variety of depletion thickness mainly occurs at the

channel region. Significantly, it is true that the first p^+ layer is completely depleted by the n channel and the first n^+ layer. With the increase of positive gate voltage, the deplettion depth into the first p^+ layer by the contribution of depletion charge in channel layer is decreased and then the depletion depth into the first n^+ layer by the contribution of depletion charge in the first p^+ layer is increased (note that the $p^+/n^+/p^+$ layers are entirely depleted). Thus, the reverse-biased J3 will cause the substantial elevation of energy band in the first n^+ "heavy-doped" layer. Similar to the above condition, the energy band of the second n^+ "heavy-doped" layer (cap layer) is also elevated, as seen in Fig. 4. Thus, the reverse-biased J3 and J1 could absorb part of positive gate voltage and a relatively high gate turn-on voltage is expectable. The high turn-on voltage could enhance the drain output circuit and gate voltage swing. However, as to the device B, only a reverse-biased junction helps to absorb the forward gate voltage. Hence, the turn-on voltage of the conventional single camel-like gate is smaller than the studied device [8-10].

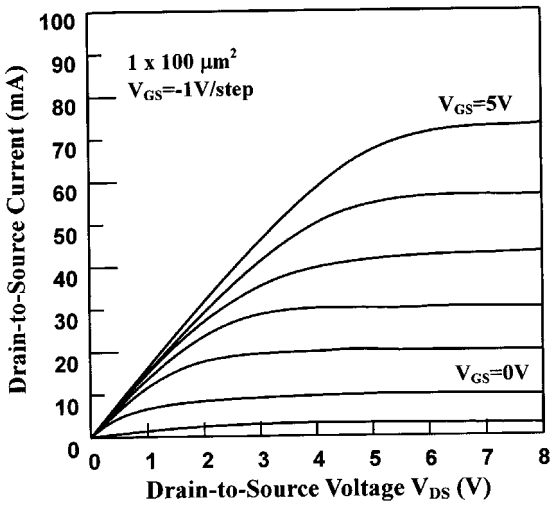

Fig.5. Experimental common-source output current-voltage characteristics of the studied device with a gate dimension of 1x 100 μm^2.

Figure 5 reveals the experimental D-S I-V characteristic of the device. The excellent transistor characteristic demonstrates a maximum drain saturation current of 730 mA/mm and an extrinsic transconductance of 166 mS/mm. The maximum gate forward voltage and threshold voltage are + 5 and – 1 V, respectively. It also exhibits good device linearity (transconductance versus V_{GS}). Furthermore, the large G-S turn-on voltage (two-terminal characteristic) allows the drain output current (three-terminal characteristic) to increase under forward gate bias. The maximum G-S forward voltage is larger as compared to the previously reported GaAs-based homojunction, heterojunction, and even pseudomorphic FETs. As compared to device A, though the maximum transconductance of device B is larger by calculation attributed to the smaller total depletion thickness, it exhibits lower turn-on voltage and relatively poor device linearity especially at large V_{GS}, which is not so suitable for linear amplifier and inverter circuit applications.

In the studied device, the double p^+ layers are critical for determining the device performances. By solving Possion's equation and using the saturated velocity limited model, the effects of the double p^+ layers are briefly described as follows. As fixing the total depletion thickness and the other parameters, the preliminary simulation exhibits that increasing the doping of the first p^+ layer and decreasing the doping of the second p^+ layer could somewhat increase the depletion depth into the channel, barrier height, and maximum transconductance. Oppositely, the gate voltage swing and the magnitude of negative threshold voltage slightly decrease. On the other hand, by fixing the total depletion thickness or the threshold voltage, increasing the doping and decreasing the thickness for each p^+ layer could somewhat decrease the depletion depth into the channel, barrier height, and gate voltage swing. But, the maximum transconductance could slightly increase.

VI. Conclusion

In summary, a novel GaAs double camel-like gate FET has been successfully fabricated and demonstrated. For the studied device, relatively high barrier height, gate turn-on voltage, and broad gate voltage swing are obtained attributed to the insert of another n^+/p^+ layers in the middle region of the double camel-like gate structure. These results indicate that the studied device is promising for linear and signal amplifiers and inverter circuit applications.

Acknowledgements

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