50 Gb/s DFF and decision circuits in InP DHBT technology for ETDM systems

A. Konczykowska, F. Jorge, M. Riet, J. Moulu, J. Godin

Alcatel-Thales III-V Lab, Route de Nozay, F-91461 Marcoussis, France

Fax. +33 1 69 63 17 85, e-mail: agnieszka.konczykowska@alcatel.fr

***Abstract* — In this paper we present two ICs fabricated in InP DHBT technology and devoted to 43 Gbit/s and over transmission systems: reshaping DFF for the transmitter and decision circuit for the receiver. High quality system operation and ease of insertion in system environment are achieved simultaneously with significant reduction of power consumption. 40 -50 Gb/s measurements are presented.**

I. Introduction

The important increase of communication services, and particularly Internet traffic, requires adequate transmission capability. Terabit/s optical networks [1] are based on a combination of dense wave division multiplexing (DWDM) and high bit-rate (over 40 Gb/s) per wavelength realized by electrical time division multiplexing (ETDM). To optimize the transmission parameters, various system enhancements like using forward error correction (FEC [2]) or advanced coding [3] are studied. These improvements add new constraints on the quality of ICs used in operational systems.

In this paper we present two ICs fabricated in InP DHBT technology and devoted to 43 Gbit/s and over transmission systems: reshaping DFF for the transmitter and decision circuit for the receiver. Measurements at 40-50 Gb/s show high quality signal of DFF and excellent sensitivity and clock phase margin (CPM) for the decision circuit. Power consumption is reduced by 40-50 % compared to previous versions.

II. Technology

The InP/InGaAs Double Heterojunction Bipolar Transistor (DHBT) technology presents several attractive aspects for the fabrication of high speed circuits. Very high frequency characteristics are achieved due to excellent electron transport properties of InP and InGaAs; the small bandgap of InGaAs base results in a low turn-on voltage, which means a potential for low power consumption; the double heterojunction gives a high breakdown voltage, necessary for large signal applications such as optical modulator drivers; finally, the vertical technological process yields a very good built-in threshold voltage uniformity, very convenient for differential bipolar logics such as CML and ECL.

An in-house InP/InGaAs self-aligned DHBT technology has been developed [4]. The transistors exhibit a high breakdown voltage (BV_{CE0} >7 V) as the result of the double heterojunction structure. Additional base optimisation results in 190 GHz F_t and 220 GHz F_{max} for circuit oriented devices at a current density about 2 mA/μm². Three Ti/Au interconnection levels, TaN resistors, MIM capacitors and spiral inductors are available to realise the circuit layout. In Fig. 1. F_t and F_{max} versus I_c for three transistors emitter sizes (3x2, 6x2 and 10x2 μm²) are shown.

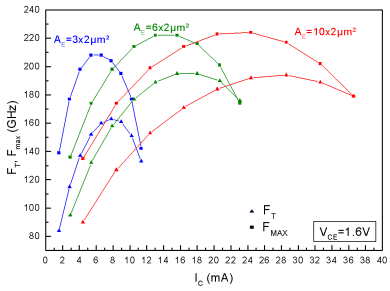

Fig. 1. F_t and F_{max} versus I_c

III. DFF circuit in ETDM systems

The synoptic of the ETDM system is presented in Fig. 2. DFF circuits are present at different locations of such a system. At the transmitting side, the multiplexed signal (at 40+ Gbit/s) is reshaped, resynchronized, and reamplified (3R) with the full-rate (i.e. clock frequency being equal to the bit-rate) DFF. At the receiving side, after the photo-receiver, a sensitive DFF can be used as a decision circuit, which also resynchronizes and reamplifies the signal. A DFF is also used in clock recovery part, while a DFF operating at half-rate is also at the core of the demultiplexing circuit. Different design specifications are to be satisfied for each of these functions. In [5-7] high speed DFFs are presented with optimization of different circuit characteristics.

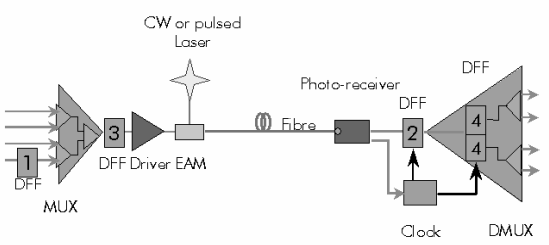

Fig. 2. ETDM synoptic with different DFF functions: 1. Delay, 2. Decision, 3. 3R, 4. DMUX

IV. IC DESIGN

A. Main challenges of DFF and decision circuit design.

The Master Slave DFF (MS-DFF) is composed of 4 main parts: input buffer, clock buffer, DFF core and output buffer. These parts are optimized using different criteria depending on the function of DFF role in the system. Input buffer determines the sensitivity and threshold margin (important for the receiver), output buffer is decisive for the output signal parameters (important for transmitter), clock buffer and core determine speed and clock phase margin. ECL architecture is systematically used to keep good frequency performances in spite of its increased power consumption (added emitter-followers). The two circuits have the same core (Fig. 3) but differ in input, output and clock buffers.

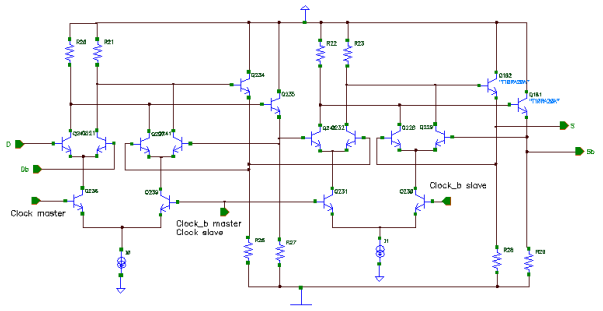

Fig. 3. DFF core electrical scheme

B. Reshaping DFF for the transmitter

The DFF present on the transmitter side, between the MUX and the modulator driver, should provide a large eye opening, both vertically and horizontally, and a sufficient output swing. The horizontal eye-opening is determined by the time jitter. This should be minimized by the adequate design of the clock buffer and the DFF core. The output buffer should not degrade the horizontal eye opening, while assuring such characteristics as: small rise and fall time, central crossing point, reduced oscillations (good S/N ratio). Very careful design of the clock access was done to minimize clock added jitter. The clock buffer was simplified to an emitter follower combined with an offsetting diode. Clock signal reference was obtained by low-pass filtering with a 5 pF capacitance. An additional small (0.3 pF) capacitance was added close to the core to further smooth the reference signal. All layout parasitics were minimized. This approach together with careful design of the output buffer resulted in measured output signal jitter comparable to the clock jitter. The microphotograph of fabricated DFF is presented in Fig. 4.

Output swing necessary for system operation is 0.5 V. We used 2 differential amplifiers to obtain a high quality signal. Beside, depending on the driver type the required output voltage may be either negative (ECL type) or without offset (centered). In general, these different variants are satisfied by using DC-block or bias-T. In our design, the offset control mechanism is integrated in the output buffer to ease integration in the system environment.

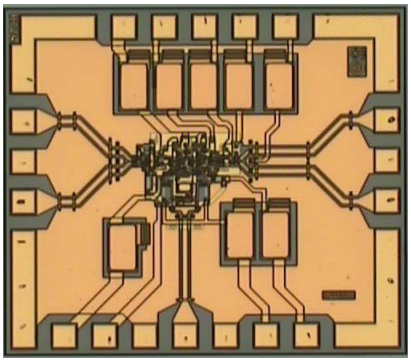

Fig. 4. Microphotograph of fabricated DFF

C. Decision circuit for the receiver

As stated before, the main features to be optimized for the decision circuit are the sensitivity and the clock phase margin. To obtain a good sensitivity, we added a sensitive input buffer using a Cherry-Hooper structure. To enhance CPM characteristics a clock buffer was added. The buffer transforms the single-ended clock signal into amplified, differential one. Master and Slave blocks are provided with clock and $clock_b$ signals.

D. Power consumption

Limitation of power consumption is not a primary goal of ETDM applications. However when more complex circuits are considered and high integration level is reached, the total dissipated power should be controlled in order to avoid self-heating. The excellent frequency performance of InP HBT, which allows to work with a lowered current density, together with the low turn-on voltage allow to realize high performance circuits with low power consumption. In this design we minimized the power consumption by using small transistors and by lowering the operating current and bias voltage, while precisely controlling their impact on circuit performances. As a consequence some power consuming alternatives were preferred (ECL architecture instead of CML one, larger transistors in the core) in order to obtain the highest quality performances. DFF core is realized with 6x2 μm^2 emitter transistors and the bias voltage is –4 V. The core power consumption is 120 mW. The same design policy was used for the design of different buffers. Resulting power consumption is 0.4 W for the DFF and 0.8 W for the decision circuit. A 40-50 % reduction in power consumption is thus obtained compared to conventional previous designs.

V. IC MEASUREMENT AT 40 – 50 GB/S

The presented measurements are performed with a remote 70 GHz sampling head and short cables. Both circuits operate at 50 Gb/s which is the limit of our measurement equipment.

A. Reshaping DFF for the transmitter

In Fig.5, a 44 Gb/s output eye of a transmitter DFF is presented. The rms time jitter is lower than 0.4 ps resulting in 90% horizontal eye-opening. Vertical eye opening is 84%, rise-time 7 ps, fall time 7.5 ps and S/N (Signal to Noise) ratio = 19. Centered output, obtained without any additional elements, is presented in this measurement. The negative signal with similar quality is obtained with different offset bias values.

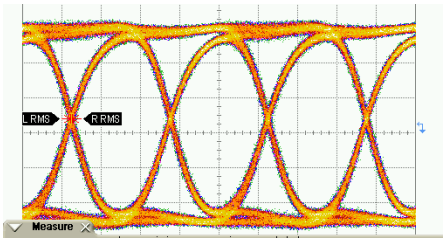

Fig. 5. DFF 3R operation @ 44 Gbit/s (9 ps/div, 100 mV/div)

B. Decision circuit for the receiver

In Fig. 6, a clock phase margin (CPM) estimate for this circuit at 40 Gb/s is shown. 8 ps CPM with a 20 mV amplitude input signal (eye-height only 12 mV) proves the excellent sensitivity of this circuit. In Fig. 7, we show the decision circuit operation at 50 Gb/s. The decision circuit reshapes, resynchronizes and reamplifies an input signal with S/N of only 6.6. The output signal has a S/N>17 and its RMS time jitter 0.53 ps, corresponds to the clock time jitter.

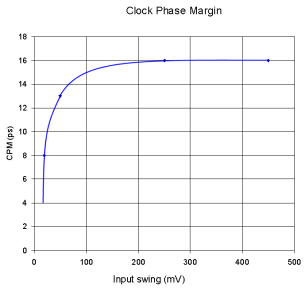

Fig. 6. Decision circuit full-rate CPM @ 40 Gb/s versus input amplitude

VI. Conclusion

Two ICs necessary for 43 Gbit/s ETDM systems were realized in InP DHBT technology. These circuits were optimized according to criteria imposed by system applications. We showed different choices and trade-offs in the design for the DFF structure depending on its role in the system. 40-50 Gb/s measurements show high quality DFF signal and excellent sensitivity and CPM of the decision circuit.

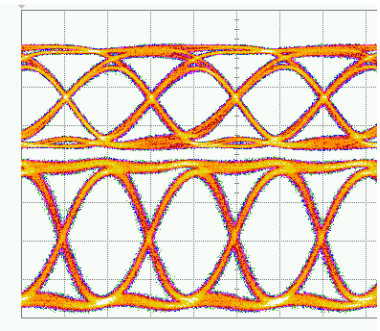

Fig. 7. Decision circuit operation @ 50 Gb/s (8 ps/div, 100 mV/div). Top: input, bottom: output.

Acknowledgement

The authors wish to thank Ph. Berdaguer for technology and A. Scavennec for discussions and encouragement.

References

[1] K. Fukuchi, “Wideband and ultra-dense WDM transmission technologies toward over 10-Tb/s capacity”, in Proc. OFC ’02, Anaheim (USA), March 2002, paper ThX5, pp. 558-559

[2] Y. Miyamoto, K. Yonenaga, S. Kuwahara, M. Tomizawa, A. Hirano, H. Toba, K. Murata, Y. Tada, Y. Umeda, and H. Miyazawa, “1.2Tbit/s (30 x 42.7 Gbit/s ETDM channel) WDM transmission over 3 x 125 km with forward error correction”, IEE Electronics Letters, Vol. 36, N° 9, pp. 812-813, 27th April 2000

[3] M. Yoneyama, et al., “Differential Precoder IC Modules for 20- and 40-Gbit/s Optical Duobinary Transmission Systems”, IEEE Trans. on Microwave Theory and Techniques, Vol. 47, N° 12, pp. 2263-2270, Dec. 99

[4] Blayac, et al., “MSI InP/InGaAs DHBT technology: beyond 40 Gbit/s circuits”, 14th Indium Phosphide and Related Materials Conference, in Proc. IPRM 2002, May, 2002, Stockholm, Sweden, B1-4, pp. 51-54

[5] K. Ishii, H. Nosaka, M.Ida, K. Kurishima, T. Enoki, T. Shibata and E. Sano, “High-input-sensitivity, low-power 43 Gbit/s decision circuit using InP/InGaAs DHBTs”, IEE Electronics Letters, June 2002, vol. 38, N° 12, pp. 557-558

[6] A. Konczykowska, F. Jorge, A. Kasbari, W. Idler, L. Giraudet, K. Schuh, B. Junginger and J. Godin, “High-sensitivity decision circuit in InP/InGaAs DHBT technology and 40-80 Gbit/s optical experiments”, IEE Electron. Lett,. October 2003, vol. 39, N° 21, pp. 1532-1533

[7] Y. Amamiya, Y. Suzuki, J. Yamazaki, A. Fujihara, S. Tanaka and H. Hida, “1.5-V Low Supply Voltage 43-Gb/s Delayed Flip-Flop Circuit”, GaAs IC Symp, San Diego, CA, November 2003, pp. 169-172