An Empirical Large Signal Model for Silicon Carbide MESFETs

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***Abstract* — In this paper, a large signal table-based model for SiC MESFET is presented. A packaged commercially available high power MESFET device (CREE CRF24010) is adopted for the model development. The extracted bias-dependent elements of the small signal model as well as the measured DC data are mathematically described by small modification of Angelov's formulation. Dispersion between DC and RF characteristics of the drain current is also observed and interpreted. The new model is capable to predict small signal as well as large signal performance accurately. A single stage ultra broadband 5 W power amplifier has been developed to verify the derived model. A good agreement has been obtained between simulated and measured results.**

I. Introduction

Silicon carbide (SiC) has received remarkable attention during the last decade as a promising material for high power, high frequency, high temperature device applications due to its high thermal conductivity and high breakdown voltage. Furthermore, application of SiC-MESFETs simplifies impedance matching and results in efficient power coupling and broad bandwidth compared to Si and GaAs devices [1]. The interest in power amplifier design based on this technology necessitates the development of accurate large signal models that can predict the maximum output power level, achievable power added efficiency (PAE), intermodulation behavior and other nonlinear phenomena over the whole bias and frequency range, using harmonic balance (HB) simulation. Today, empirical table-based models are the most widely used models in nonlinear circuit simulators which have the advantage of high flexibility and computation efficiency. A lot of empirical nonlinear MESFET models for microwave circuit simulators have been developed, e.g. [2, 3]. In this approach, the tabulated data that represent the extracted nonlinear elements of the small signal model are mathematically transformed into spline functions which should be differentiable to a high order of derivatives in order to ensure a correct description of harmonics and convergence applying harmonic balance simulations [3]. As an extension to the previous authors' work given in [4, 5], an empirical model based on SiC MESFET has been developed and verified. This paper is organized as follows: Sec. II presents the model incorporating empirical expressions for DC, capacitance and frequency dispersion. The accuracy of the new model will be verified in Sec. III. Based on the derived model, a single stage ultra wideband PA has been designed and small signal as well as large signal simulations and measurements have been demonstrated. The conclusion of the work is given in Sec. IV.

II. Model Description

Our approach is based on a multiple bias small signal model. The extrinsic elements of the small signal model are extracted from cold-FET operation whereas the intrinsic parameters are calculated directly from measured network parameters at various bias points [4]. The equivalent circuit of the proposed nonlinear model is shown in Fig. 1. The nonlinear elements are the gate-drain diode d_{gd}, the gate-source diode d_{gs}, the static drain current source I_{dsDC}, the gate-source capacitance C_{gs}, the gate-drain capacitance C_{gd}, the drain-source capacitance C_{ds} as well as the dispersion current source I_{dsRF}.

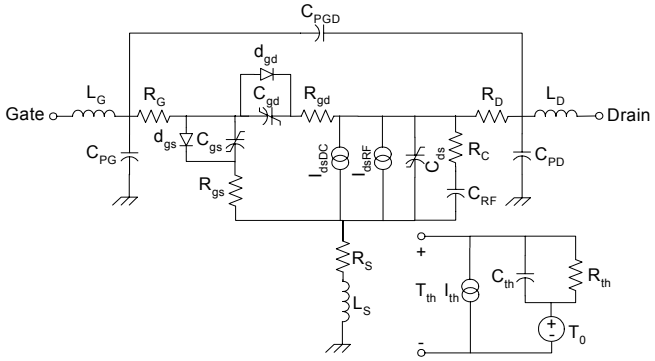

Fig. 1. Large signal model of SiC MESFET.

A. Drain Current Modeling

The DC characteristics of the presented model are based on the approach by Angelov [3]. We use a slightly modified saturation voltage parameter α to match the measured data of the SiC device:

$$\alpha = \alpha_r + \alpha_1(\alpha_2 + \tanh(\psi)) \tag{1}$$

The model has been implemented in ADS from Agilent. Measured and simulated DC characteristics for the Cree SiC MESFET device CRF24010 are shown in Fig. 2. Excellent agreement between measurements and calculations could be achieved over a wide bias range V_{ds} up to 60 V and V_{gs} between –13 V and –5 V. The small letters (ds) and (gs)

indicate intrinsic device voltages. The device was mounted on a heat sink during the measurements providing a ground plate temperature of the device package of about 20°C.

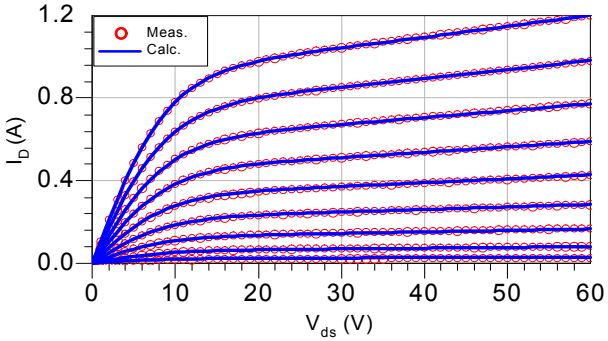

Fig. 2. Measured (symbols) and calculated (solid lines) DC characteristics of the SiC MESFET device CRF24010, V_{gs} = - 13 V to - 5 V, step 1 V.

Table 1 gives an enhanced comparison of the DC model quality with state of the art work. The values of the error function (Table 1) indicate that our model achieves the lowest values of the error function compared with other CAD models.

Table 1. Comparison of the error function values of the most used CAD models in ADS.

Model	Error
Curtice-Ettenberg model [8]	$2e^{-3}$
Materka-Kacprzak model [7]	$8.2e^{-4}$
Statz model [6]	$7.14e^{-4}$
TOM3 model [9]	$2.9e^{-4}$
Our model	$4e^{-5}$

B. Capacitance Modeling

Capacitance modeling becomes more and more important if operating frequencies increase. At higher frequencies nonlinear capacitances have a raising influence on frequency response, harmonic and intermodulation distortion. There are two main approaches for modeling of the gate charge, the capacitance and charge approach. We use the capacitive approach and describe the capacitance voltage characteristics of the device. Again, the formulation used here is similar to the model of Angelov *et al* [3]. Both capacitances show a dual voltage dependence and integration path independency of the capacitance functions has been verified. Unique charge functions and charge conservation are guaranteed this way which are very important suppositions for stable and reliable harmonic balance simulations.

As an example for the capacitance modeling the extracted and modeled gate source capacitance C_{gs} versus V_{ds} (parameter V_{gs}) is shown in Fig. 3. A very satisfactory agreement between measured and simulated data can be observed.

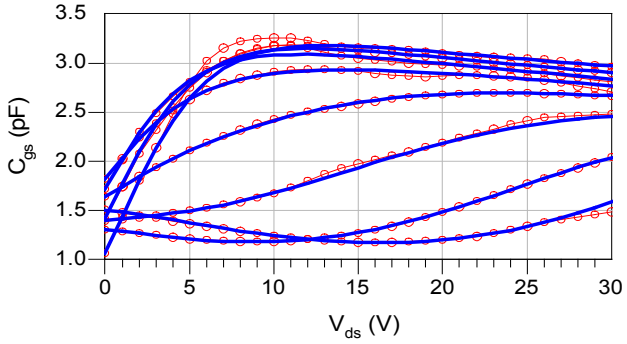

Fig. 3. Measured (symbols) and modeled (solid lines) gate-source capacitance C_{gs} versus V_{ds}, V_{gs} varies from - 13 V (bottom) to - 6 V (top), step 1 V.

C. Frequency Dispersion and Thermal Modeling

Measurements at the SiC device have shown that the RF current characteristics are different from DC ones (low frequency dispersion) done by deep level trapping. This behavior can be described by using two different drain current sources one for the low frequency and one for the RF range, respectively. E. g., the RF current source can be obtained by integration the small signal transconductance g_m and output conductance g_{ds}, respectively:

$$I_{dsRF} = \int g_m dV_{gs} + g_{ds} dV_{ds} \qquad (2)$$

One way to eliminate the differences between high- and low-frequency output conductances is to add a capacitive coupled resistive branch (R_C, C_{RF}) to the output as shown in Fig. 1. The introduction of smoothing functions for matching the differences between low and high frequency operation would be another approach [10]. The resistance R_C is selected to be a bias dependent hyperbolic function in order to eliminate dispersion effects in the entire large signal range. This is important with respect to the ability of the model to predict the nonlinear behavior in the whole operating range with high accuracy and reliability.

$$R_C = R_{C\min} + \eta_1 / (1 + 1/R_{C\max} + \eta_2 \tanh(\psi)) \qquad (3)$$

R_{Cmin} and R_{Cmax} represent the minimum and the maximum dispersion resistances, respectively and η_1, η_2 and ψ are functions of V_{gs}, V_{ds}. The parameters of (3) are being found by optimization of S_{22} at several bias points. Verification of frequency dispersion modeling is finally demonstrated in Fig. 4.

A dynamic thermal model is introduced, too. A low-pass structure which accounts for self-heating effects is shown in Fig. 1. The model based temperature behavior is presented in Sec. III.

III. Model Verification

The proposed model has been implemented as a user-defined model into the harmonic balance circuit simulator

ADS from Agilent and large signal performance has been studied as an extension of the work given in [4].

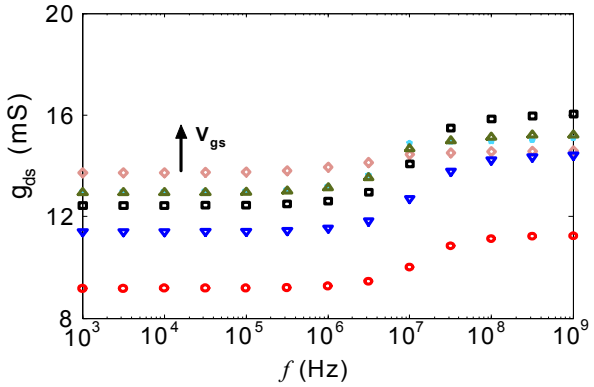

Fig. 4. Dispersion of the output conductance at V_{ds} = 30 V and V_{gs} = – 11 V to – 6 V, step 1 V.

For this reason, a single-stage wideband power amplifier has been designed [5], built up and characterized using the Cree SiC MESFET CRF24010. A heat sink was used during the experiments so that the device temperature was very close to room temperature. In contrast to [5], in this work the verification of the large signal performance of the model (not of the amplifier) is the main goal. The large signal model presented here was not available at publication time of [5].

Simulated and measured power performances of the designed power amplifier are compared in Fig. 4 at 1 GHz. Excellent agreement has been achieved for output power (P_{out}) and power gain (G_P). A 1 dB_{CP} of 37 dBm can be taken from Fig. 5. With respect to the PAE performance, 1 % error for maximum PAE value can be observed.

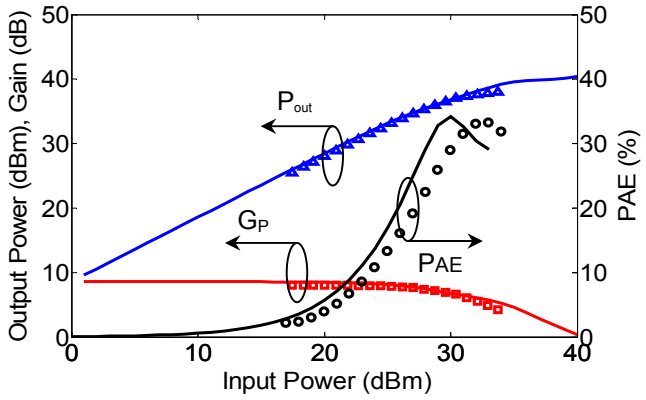

Fig. 5. Measured (symbols) and simulated power performance of the designed PA based on the derived model (solid lines): f = 1 GHz, V_{ds} = 30 V, I_D = 500 mA.

Over the whole frequency band (10 MHz – 2.4 GHz), the power performance as well as the linearity performance (two-tone test) of the designed amplifier have been characterized and compared with simulations based on the proposed model.

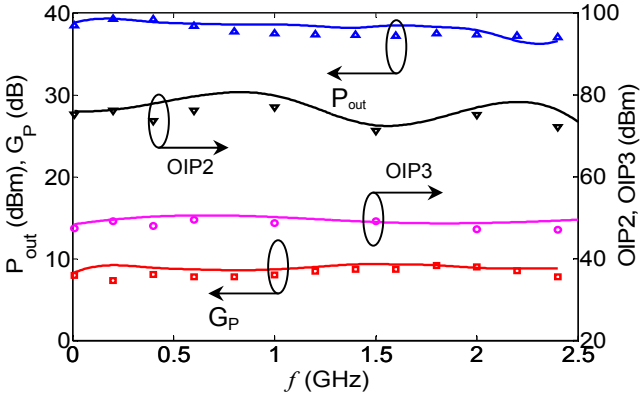

Fig. 6. Measured (symbols) and simulated power and linearity performances of single stage PA over the operating frequency range: V_{ds} = 30 V, I_D = 500 mA and Δ = 200 kHz.

Fig. 6 illustrates the overall simulated and measured performances versus frequency. Regarding the power performance, excellent agreement between simulations and measurements has been achieved. On the other hand, slight differences of 4 dBm and 2 dBm between the measured and modeled second- and third-order output intercept points (OIP2 and OIP3) respectively, can be observed.

The impact of case temperature variation has been studied, too. Fig. 7 shows the simulated and the measured power performance of the single stage PA versus temperature. A good agreement can be noticed with only 0.6 dB power gain deviation at 60 °C between simulations and measurements.

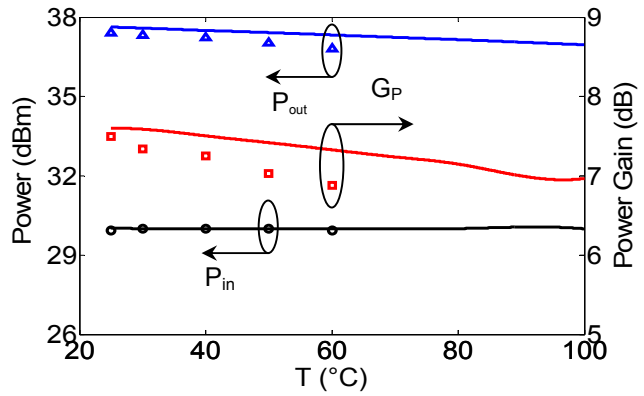

Fig. 7. Measured (symbols) and modeled (solid lines) power stage performance versus temperature: f = 1 GHz, V_{ds} = 30 V and I_D = 500 mA.

In this work we have also investigated the group delay. For minimum distortion the variation of the group delay within the modulation bandwidth has to be as low as possible. Group delay τ is defined as the slope of the transmission phase versus frequency [11]

$$\tau = -\frac{d\phi}{d\omega} \tag{4}$$

where ϕ is the transmission phase in radians, and ω is the radiant frequency in (*rad*/s).

At an input power of 25 dBm, Fig. 8 illustrates the group delay variation over the operating bandwidth of the implemented SiC MESFET power stage. It can be seen that up to 2.5 GHz, a low value of up to 1.4 ns has been achieved.

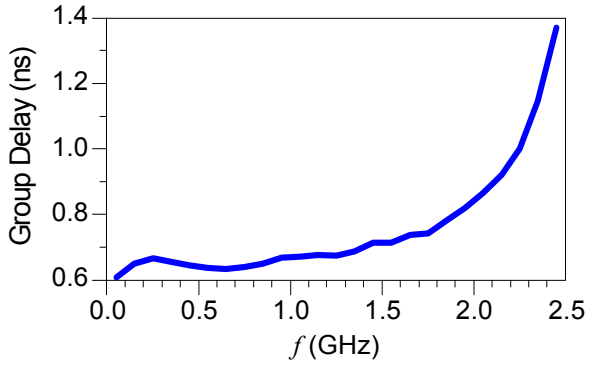

Fig. 8. Simulated group delay of the implemented model based on SiC MESFET: Pin = 30 dBm, VDS = 30 V and ID = 500 mA.

IV. Conclusion

A new large signal table-based model for SiC MESFETs based on Angelov's formulation has been developed. Temperature dependence and dispersion effects are included. The new model has been implemented as a user-defined model in the harmonic balance circuit simulator ADS. Based on an implemented single stage PA, the derived model has been verified. Measured small and large signal performances as well as temperature behavior agree pretty well with simulations.

References

[1] S. T. Allen, W. L. Pribble, R. A. Sadler, T. S. Alcorn, Z. Ring and J. W. Palmour, "Progress in high power SiC microwave MESFETs," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, Anaheim, CA, pp. 321-324, June 1999.

[2] A. Rofougaran and A. A. Abidi, "A table lookup FET model for accurate analog circuit simulation," *IEEE Trans. Microwave Theory and Tech.*, vol. 47, pp. 2350-2357, Dec. 1999.

[3] I. Angelov, N. Rorsman, J. Stenarson, M. Garcia and H. Zirath, "An empirical table-based FET model," *IEEE Trans. Computer Aided Design*, vol. 12, pp. 324-335, Feb. 1993.

[4] A. Sayed and G. Boeck; "Small signal modeling of SiC power MESFETs for ultra broadband power amplifiers," *28th WOCSDICE*, Slovakia, pp. 79-80, May 2004.

[5] A. Sayed, S. von der Mark and G. Boeck, "An ultra wideband power amplifier using SiC MESFETs," *Proc. 34th European Microwave Conf.*, Amsterdam, Netherlands, Oct. 2004.

[6] H. Statz, R. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron Devices*, vol. 34, pp. 160-169, Feb. 1987.

[7] T. Kacprzak and A. Materka, "Compact DC model of GaAs FETs for large-signal computer calculation," *IEEE J. Solid-State Circuits*, vol. Scull, pp. 211–213, April 1983.

[8] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 28, pp. 448–456, May 1980.

[9] R. B. Hallgren and P.H. Litzenberg, "TOM3 Capacitance Model: Linking Large- and Small-Signal MESFET Models in SPICE," *IEEE MTT,* vol. 47, no. 5, pp. 556-561, May 1999.

[10] A. Werthof, "Experimentelle modellierung aktiver bauelemente fuer die simulation nichtlinearer mikrowellenschaltungen," VDI-Verlag GmbH, Page 189. Duesseldorf 1995.

[11] P. Vizmuller, "RF Design Guide: Systems, Circuits, and equations," *Artec House, Inc,* 1995.