Thermal management of power HBT in pulsed operating mode

D. Floriot[1], J-C. Jacquet[1], E. Chartier[1], J-M. Coupat[2], P. Eudeline[2]
P. Auxemery[3], H. Blanck[3]

[1]Alcatel-Thales III-V lab, Rte de Nozay, 91461 Marcoussis Cedex, France.
[2] Thales Airborne Defense – Z.I. du mont Jarret – 76520 Ymare, France

[3]United Monolithic Semiconductor, Domaine de Corbeville, RD 128, 91404 Orsay Cedex, France.

Abstract — **We focus this paper on the improvement of the thermal management of power transistor based on the InGaP / GaAs HBT technology and specially for pulsed mode application Applied to very HBT high power transistor, from 10W to 3W, respectively for L to Ku bands radar applications, a specific study has been done to suggest new opportunities if we take into account the transient or dynamic behavior of the transistor in pulse operating mode. From very short pulse (1 µs) to very long pulse (≈ 1 ms), a analysis has been performed with as a consequence a strong improvement of thermal impedance (Zth) through specific designs of the thermal shunt (material – shape) present at the front side. We chose to develop the concept of "thermal sponge" on power HBT transistor acting as a very efficient thermal capacitance to suppress thermal variation inside the pulse and improving as a consequence the CW thermal resistance. Two approaches have been compared : the first one with the support of very thick metal growth directly on the thin gold thermal shunt, the second one with a very small part of diamond substrate directly on top the same thermal shunt. As a conclusion, for long pulse application greater than 200 µs up to 1 ms, the diamond approach gives superior result with 30% of improvement on the temperature rising.**

I. INTRODUCTION

We focus this paper on the improvement of the thermal management of power transistor based on the InGaP / GaAs HBT technology and specially for pulsed mode application. This one is an already well known technology, with more than 15- years long development and publication and nowadays used mainly for medium power amps and low phase noise source in wireless. Others more stringent applications (Radar for military or space domains) require higher power density with a high PAE to sustain thermal and so reliability specifications. A lot of work have been published on the optimization of the HBT technology to find the best tradeoff between performances and thermal heating. Most of them have been focused on the decreasing of the CW thermal resistance (Rth in °C/W) by appropriate work on the layout of the transistor or through technological development from the front side (thermal shunt) or back side (thinning) of the process. Finally, few of them are devoted to the optimization of the assembling by using efficient raw material with good thermal properties or appropriate assembling (flip- chip for example). Applied to specific very HBT high power transistor, from 10W to 3W, respectively for L to Ku bands radar applications, a specific study has been done to suggest new opportunities if we take into account the transient or dynamic behavior of the transistor in pulse operating mode. From very short pulse (1 µs) to very long pulse (≈ 1 ms), a complete analysis has been performed with as a consequence, the demonstration of new power elementary cell and various attempts to decrease the thermal impedance (Zth) through specific designs of the thermal shunt (material – shape) present at the front side.

II. STATUS ON THE POWER HBT TECHNOLOGY

All the development are mainly based on the open HB20P HBT process line of UMS (United Monolithic Semiconductor) or process under qualification [1]. Very few open sources have been optimized to offer high level of performances up to Ku Band. Typically we speak about of a transistor delivering more than 1 W in CW with a power added efficiency (PAE) greater than 50%. Most of them are based on InGaP / GaAs epitaxial structure and a ledge passivation layer offering as a consequence a high reliability level. Depending on the frequency of the application, power HBT transistor combine elementary fingers with a length ranging from 20 to 100 µm respectively for Ku to L band and for an emitter width of roughly 2 µm. The number of finger depends also of the frequency and the expected performances as the topology of combining of these fingers (fishbone versus parallel). It means that 1W is demonstrated with transistor combining 8 fingers of by 2 x 40 μm^2 in CW with a bias collector voltage of 8V and a collector current density of 30 kA/cm^2. To satisfy this level of performance and an " appropriate thermal junction" , a thermal shunt is used in order to decrease the thermal resistance of each elementary finger and also to equilibrate all the fingers between them. By "appropriate thermal junction", we put as a request an operating temperature compatible with the application in term of mean time of failure (MTF) and derived from the main mechanism of degradation characterized by his energy of activation (Ea). The thermal shunt is processed by the way of a thin gold radiator (4 to 6 µm), connecting all the top emitter (figure 1) and assuming both a thermal spreader and a very low inductance ground path. This design has an impact on the spacing between the

elementary power fingers for which a distance of 30 to 40 µm has to be assessed.

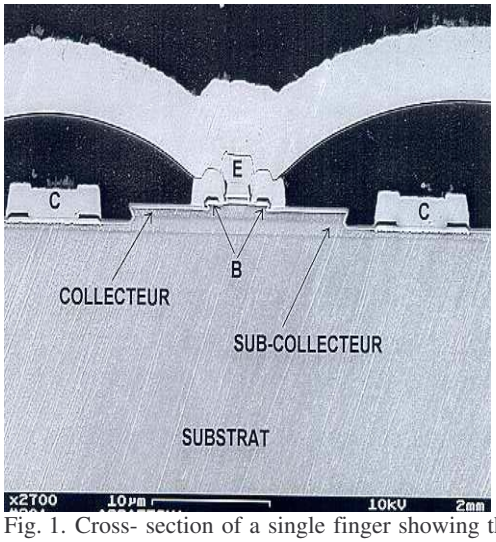

Fig. 1. Cross- section of a single finger showing the thermal shunt connecting the top emitter.

III. HOW TO GO FURTHER

The main idea was to take into account the pulse operating mode so the pulse length and the duty cycle of the applications. One very another important aspect is the expected amount of dissipated power (DP) by finger, this one being fixed by the following relationship :

DP = P_{DC} x (1 – PAE) with PAE = (P_{out} – P_{in}) / P_{DC}.

Pout = Intrinsic Output Power - Pin = Intrinsic Input Power

P_{DC} = Intrinsic dissipated Bias power = Vbe.Ib + Vce.Ic

Note that "Intrinsic" means that all these definitions have to be computed at the level of the intrinsic junction of the transistor corresponding to an equivalent de-embedding.

The first level of thought is to remember the thermal properties of some material commonly used in microelectronics. In the following table 1, the Lt parameter is the thermal transfer length giving the distance for which one thermal pulse senses a infinite volume.

$$Lt = \sqrt{\frac{\lambda}{\rho.Cp}}.\tau$$ where ρ is the density in g/cm^3, Cp the specific heat in J / g. K and τ the pulse length.

Note that this parameter have been computed for three values ranging from 10µs to 1 ms, this criteria giving an excellent view of the thermal properties of key materials.

Material	Specific Heat (J/g.K)	Density (g/cm3)	Thermal conductivity (300K) - W/cm.K	Diffisitivity	Lt (10µs)	Lt (100µs)	Lt(1ms)
Si	0,7	2,33	1,45	0,89	29,82	94,29	298,17
GaAs	0,35	5,3	0,46	0,25	15,75	49,80	157,47
GaInP			0,058				
Au	0,13	19,3	2,7	1,08	32,80	103,74	328,04
Ag	0,234	10,5	4	1,63	40,35	127,59	403,49
Cu	0,39	8,9	3,9	1,12	33,52	106,00	335,20
SiC	1,3	2,97	3,9	1,01	31,78	100,50	317,82
AlN	0,78	3,32	1,7	0,66	25,62	81,02	256,22
GaN	0,49	6,15	1,9	0,63	25,11	79,40	251,10
D	0,52	3,52	18	9,83	99,17	313,59	991,66

Table 1 : Comparison of the thermal transfer length for very common material.

From this table, it explains why no strong effect is awaited on the thinning process of the GaAs substrate down to 50 µm and need to be pushed until 30 µm to obtain a significant improvement. Nevertheless, this way is very complex to follow.

Three metals are very close from each other in term of Lt : Au – Ag – Cu, the Silver being in prime position with 20% of improvement on the Zth.

Another well known approach is to use a flip- chip assembly[2] of the transistor on a dielectric like AlN, SiC or diamond. The advantage of the HBT versus PHEMT would be to offer a direct way from the heat source (collector region) to the thermal remover through the power bump. Nevertheless, regarding the mechanical constraints put inside the elementary cells, the power bump need to be shifted away from the heat source, decreasing the efficiency of this method.

In this paper, we chose to develop the concept of "thermal sponge" acting as a very efficient thermal capacitance to suppress thermal variation inside the pulse (figure 2). Moreover, we obtain also a strong effect on the CW thermal resistance thanks to an improved radiator and also to a better uniformity alongside the fingers.

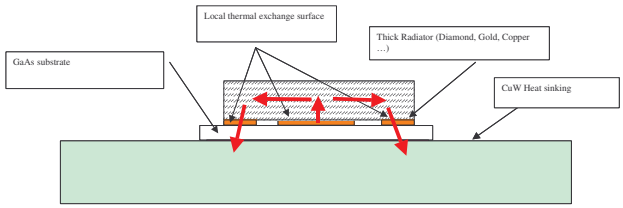

Fig. 2. Ideal view of the concept of "thermal sponge" or thermal capacitance applied to power HBT.

Two approaches have been followed, the first one with the support of very thick metal growth directly on the thin gold thermal shunt already present on the power HBT. The second approach is to mount a very small part of diamond substrate directly on top the same thermal shunt. Both methods are equivalent to act as a thermal capacitance but very different in the final result where the impact of the diamond is stronger.

Preliminary computation have been done to fix the size of the radiator taking into account the processing and electrical constraints. Moreover, this optimization has been applied to two different applications using medium pulse length (10 to 50 µs) and very long pulse (0.2 to 1 ms) for respectively two power HBT of 2 Watts and 10 Watts.

Modeling status

The two following figure give a representation of the two meshing for a which a comparison between a very thick metal and a diamond substrate. A lot of computation have been completed to compare Gold and Copper metals with Diamond. Due to processing constraints, the thickness of the metals are kept close to 35 µm, the diamond substrate having a thickness of 300µm.

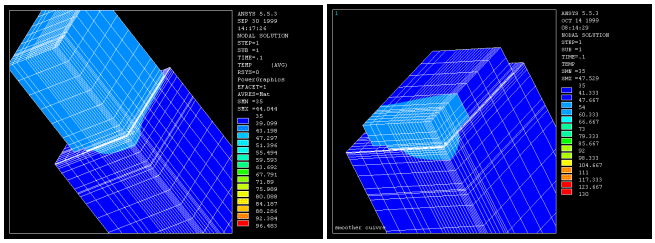

Fig. 3. View of the meshing of power HBT with diamond and thick metal radiator.

As we observe on the figure 4 giving the maximum temperature versus the PAE, for a reference value of 60%, the difference between thick gold and diamond is around 30°C in favor of the latter.

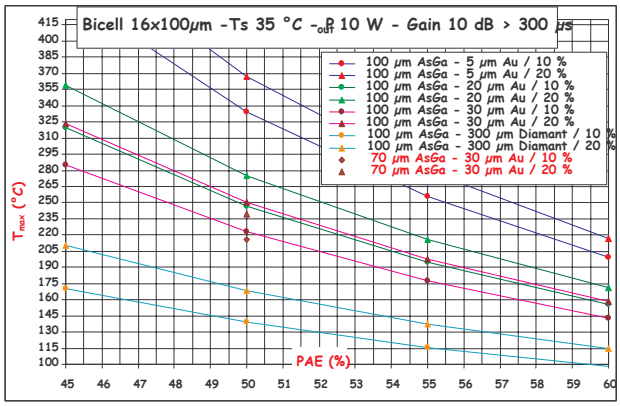

Fig. 4. View of the meshing of power HBT with diamond and thick metal radiator

Processing status

Thermal shunt based on thick metal have been processed with thickness ranging from 20 to 100µm !!. The next photos compare a 4 fingers transistor without and with a 40 µm thick copper radiator, the third figure giving an overview of a 30 µm thick gold radiator on a multi- transistor power bar.

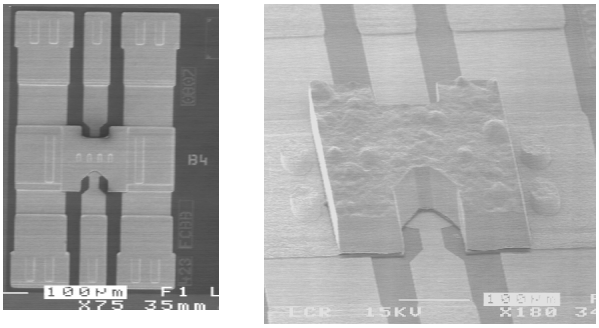

Photo 1 : Comparison of a 4 fingers power HBT without (left) and with (right) a thick copper radiator.

Thermal shunt based on thick diamond substrate has also been applied to power transistor and multi- transistor power bar. The diamond is assembled thanks to a soldering process, a AuSn (80/20) multi layers being present on the face of the diamond in contact with the thin gold thermal shunt. This method allows to make easier the assembly conditions in term of force, temperature and time.

The next two photos gives the comparison before and after the diamond report for which a deliberate shift of the substrate have been applied to make easier the control of the process.

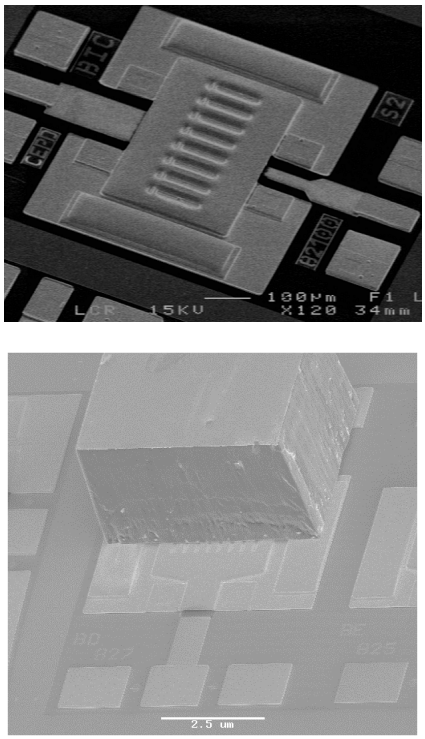

Photo 1 : Comparison of a 20 fingers power HBT without (left) and with (right) a diamond radiator.

IV. Result and Discussion

In the next, we will focus our discussion on the most impressive result coming from the use of diamond substrate as thermal capacitance.

To illustrate the behavior of the transitory, we present figure 5 the collector current pulse for two transistors, with and without diamant. A voltage source is applied and the value is tuned to obtain the same current at the beginning of the pulse for both cases. The strong difference is due to the thermo- electrical feedback present in the transistor without diamond for which a higher temperature causes an extra current consumption Note also, the strong impact of the diamond to suppress any variation during the pulse.

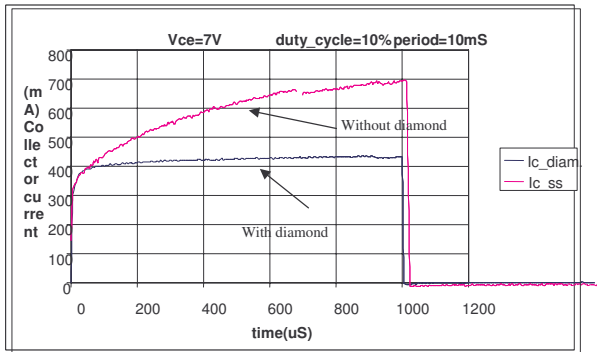

Fig. 5. Variation of the collector inside a pulse of 1 ms length for two transistors with and without diamond heat spreader.

In order to be exhaustive [3], we present figure 6 also comparison between the thick gold and the diamond approaches on a power bar combining 4 HBT of 10W each and giving the decreasing of the temperature after pulse. We observe 30°C in favor to the diamond approach corresponding to 35% of improvement regarding the case temperature of 35°C.

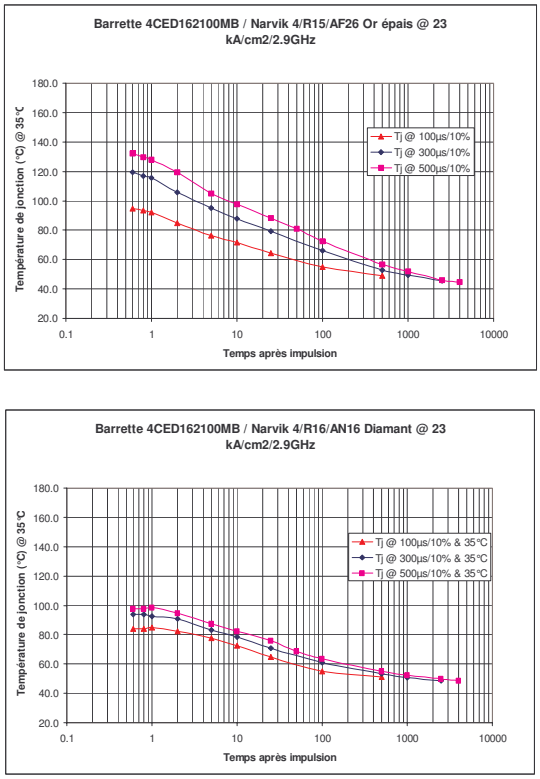

Fig. 6. Estimated relationship between the time an author spends reading these instructions and the quality of the author's proceedings article.

V. Conclusion

We chose to develop the concept of "thermal sponge" acting as a very efficient thermal capacitance to suppress thermal variation inside the pulse and improving as a consequence the CW thermal resistance.

Two approaches have been compared : the first one with the support of very thick metal growth directly on the thin gold thermal shunt, the second one with a very small part of diamond substrate directly on top the same thermal shunt. As a conclusion, for long pulse application greater than 200 µs up to 1 ms, the diamond approach gives superior result with 30% of improvement on the temperature rising.

Acknowledgement

This work has been supported by the French MoD with the contract n° 0034063, by Thales Air Defense and by Thales Airborne Systems.

References

[1] : H. Blanck et al. "Industrial GaInP/GaAs Power HBT Process", *GaAs2000 Conference* – pp.113-11

[2] : O. Vendier, S. George, et al "Power flip-chip assembly for space application using HBT in Ku band"

[3] : S.Piotrowicz[I], E.Chartier[I], J.C.Jacquet[I], D.Floriot[I], J.M.Coupat[II], C.Framery[II] and P.Auxemery[III] " High Power and High Efficiency Compact S-Band HBT power chips with Gold or Diamond Thermal Heat Spreaders"