

Ultra High IP3 Passive GaAs FET Mixers

Andreas Wentzel, Dariusz Pienkowski, Georg Boeck

Technische Universität Berlin, Microwave Engineering
Skr. HFT5-1, Einsteinufer 25, 10587 Berlin, Germany

Email: pienkows@mwt.ee.tu-berlin.de, Tel. (+49)30 314-26895, Fax (+49)30 314-26893

Abstract - This paper describes single-balanced passive GaAs FET mixers with different balancing principles for the lower GHz range. The mixers achieve conversion losses of about 7 dB and input third-order intercept points (IIP3) of up to 44 dBm. Port isolation values of more than 70 dB have been achieved. Different balancing topologies, design process and results are being discussed.

I. INTRODUCTION

Single-balanced mixers are used for improving LO-RF and LO-IF isolation, power compression, intermodulation and noise [1]. Today, high third order intercept point (IP3) mixers are needed for base stations of wireless communication systems, in terrestrial as well as satellite communication and in microwave measurement systems. GaAs MESFETs and pHEMTs have been known as very suitable candidates for realizing highly linear passive mixers [1]-[3], [5]. FET size, LO power, balancing principle and quality as well as frequency range are the parameters primarily determining the linearity properties. Conversion loss and noise behavior of passive FET mixers is very close to those of diode mixers. Details on the operating principle of those mixers are given in [1]. This work investigates ultra high IP3 passive GaAs FET mixers with two different balancing topologies. In the first case, RF- and IF- balancing was performed at the drain whereas the LO at the gate was unbalanced. In the second topology, the LO at the gates and the IF at the sources of the FETs were balanced and RF at the drains was unbalanced. Ferrite transmission line transformers were used for balancing. We will show that the two topologies lead to different linearity properties. The mixers were simulated and optimized using *Agilent's ADS™*, built up and measured. The presented data were taken at RF-, LO-, and IF- frequencies of 1 GHz, 900 MHz and 100 MHz, respectively. Section II describes the operating mode of the two circuits whereas section III compares simulated and measured data. The conclusion in section IV completes this paper.

II. CIRCUIT REALIZATION

Fig. 1a and Fig. 1b show the schematics of both single-balanced resistive mixers. The two RF/IF and LO/IF balanced mixers were built up with commercially available devices: packaged 0.25 μm pHEMTs and ferrite transmission line transformers having an impedance ratio of 1:4 and a insertion loss of about 0.8 dB at 100 MHz. S-

parameter characterization has been performed for the transformers. These S-parameters together with the pHEMT model of Angelov [4] were used for the ADS simulations. All ports were matched to 50 Ω .

A. LO/IF-balanced mixer

Fig. 1a shows the LO/IF-balanced mixer. A 1:4 transmission line transformer was used for the single/double ended conversion of the LO signal. Furthermore the gates are DC-biased by about the FET threshold voltage via a resistor at the transformer center tap. The RF-signal is applied to the drain over a high pass filter for improving the isolation of the RF-port. The balanced IF-output signal at the FET sources is transformed to a single ended one by a transformer, too and low pass filtered for improving the IF-isolation. The capacitors at the FET sources are for the grounding of the RF- and LO-signal, respectively.

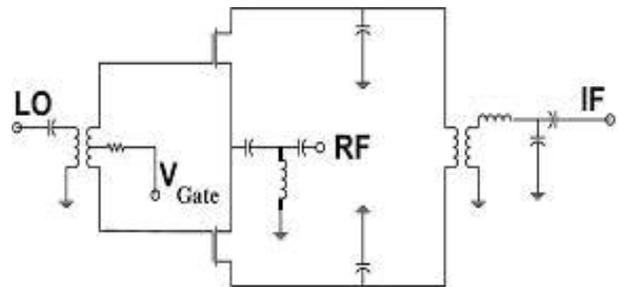


Fig. 1a. Mixer schematic with LO/IF balancing.

B. RF/IF-balanced mixer

At the RF/IF-balanced mixer (Fig. 1b) the single ended LO-signal is applied to the gates of the FETs which implies a common mode excitation of both FETs. Again, the gates can be biased close to their threshold voltage or they can be self biased by rectifying of the LO signal. Both FET sources are directly ground connected. RF/IF-signals occur balanced at the FET drains and are converted to single ended signals by a transmission line transformer, again. RF/IF high/low pass filtering is added for improving the port isolations. At the center tap of the transformer a DC voltage can be applied for additional drain bias. Most interesting, in this operating mode the mixer is active concerning LO operation and passive with respect to RF frequency conversion. It will be shown, too, that the intermodulation behavior changes strongly dependent on applied V_{Drain} .

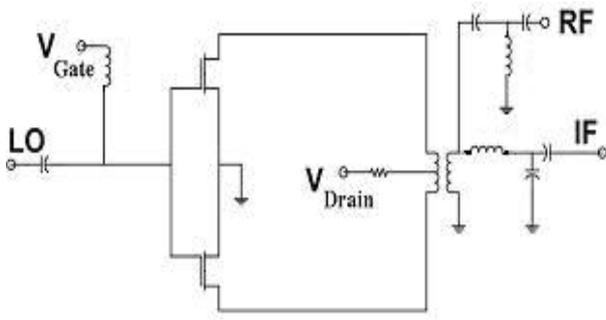


Fig.1b. Mixer schematic with RF/IF balancing.

Fig. 2a and Fig. 2b show photographs of the realized RF/IF- and LO/IF-balanced mixer circuits built up on a FR4-PCB with a thickness of 0.5 mm.

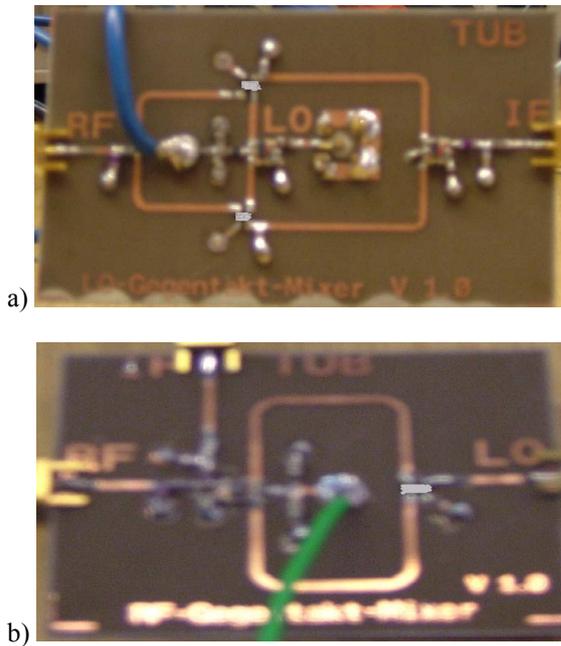


Fig. 2. Photograph of the realized mixers; a) LO/IF-balanced and b) RF/IF-balanced.

III. RESULTS

If not mentioned otherwise the subsequent given results are based on following parameters: $f_{RF} = 1$ GHz, $f_{LO} = 900$ MHz, $f_{IF} = 100$ MHz, RF power = -20 dBm, $V_{Drain} = 0$ V.

Fig. 3 shows the conversion loss of both mixer types versus LO-power. The conversion losses saturate at LO-power of about 15 dBm at 7 dB (3a) and 7.5 dB (3b), respectively. Deviation between simulations and measurements is acceptable. The lower conversion loss in Fig. 3a is due to the fact that the RF-signal of the LO/IF-balanced mixer does not propagate along the transformer in opposite to Fig. 3b where RF- and IF-signals are damped by the transformer.

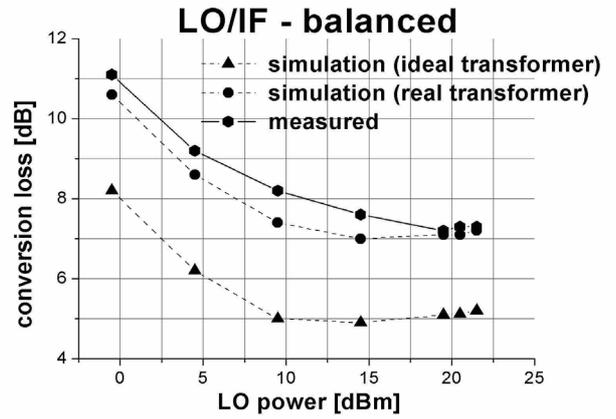


Fig. 3a. Conversion loss vs. LO power for the LO/IF-balanced mixer with gate bias $V_{Gate} = -2$ V.

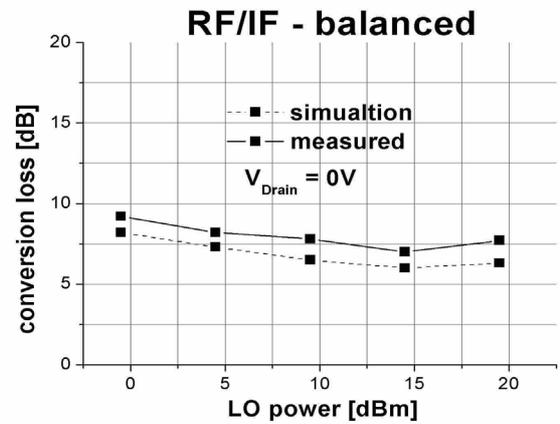


Fig. 3b. Conversion loss vs. LO-power of the RF/IF-balanced mixer with gate bias $V_{Gate} = -2$ V and drain bias $V_{Drain} = 0$ V.

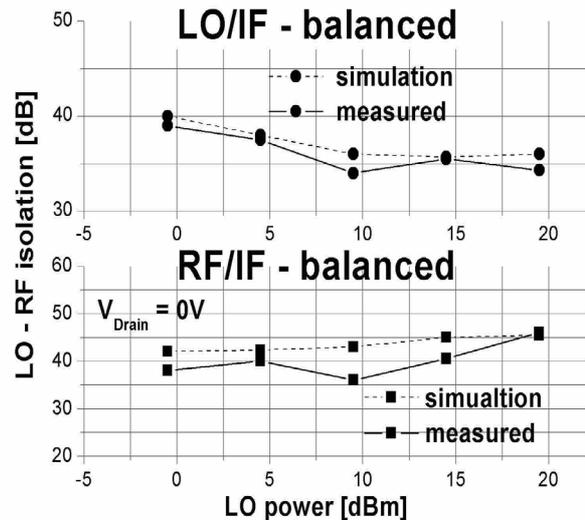


Fig. 4. LO-RF isolation vs. LO power; top: LO/IF-balanced mixer with gate bias $V_{Gate} = -2$ V; bottom: RF/IF-balanced mixer with gate bias $V_{Gate} = -2$ V and drain bias $V_{Drain} = 0$ V.

Fig. 4 shows the LO-RF-isolation. The LO-RF- as well as LO-IF-isolation values are limited by FET capacitances and the transformer imbalance. Fig. 4 shows an in principle different LO-RF-isolation behavior of both mixer types and higher mean values of the LO/IF balanced mixer. The achieved values are very satisfactory and primarily a consequence of properly working balancing. The filters contribute only a few dB to these isolation values.

The LO-IF-isolation is shown in Fig. 5. Compared to the LO-RF-isolation increased values of at least 20 dB can be observed. This is caused by the filtering.

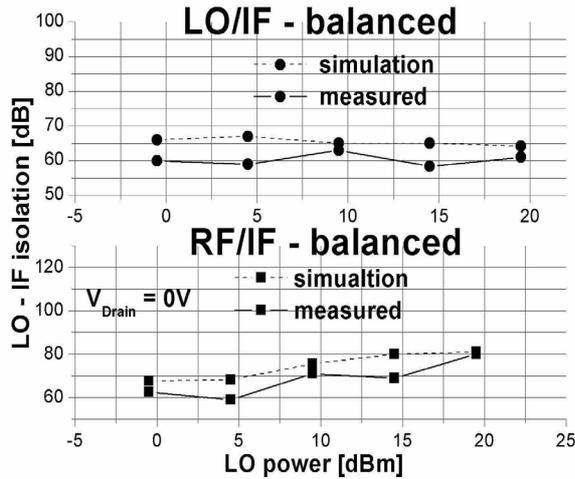


Fig. 5. LO-IF-isolation vs. LO-power; top: LO/IF-balanced mixer with gate bias $V_{Gate} = -2V$, bottom: RF/IF-balanced mixer with gate bias $V_{Gate} = -2V$ and drain bias $V_{Drain} = 0V$.

LO-IF- and LO-RF-isolation can be improved by compensating the mentioned transformer imbalance with additional capacitive and/or inductive elements. The principle is shown in Fig. 6 for the RF/IF-balanced mixer. By using a simple capacitor between gate and drain of the lower FET the LO-RF-isolation can be improved up to 80 dB (Fig. 7) and at the same time the LO-IF-isolation increases by about 60 dB compared to the isolation values of Fig. 5. Both peak values were achieved for a capacitance of about 27 fF which can be realized by an open circuited short transmission line. A similar method can be used for the LO/IF-balanced mixer.

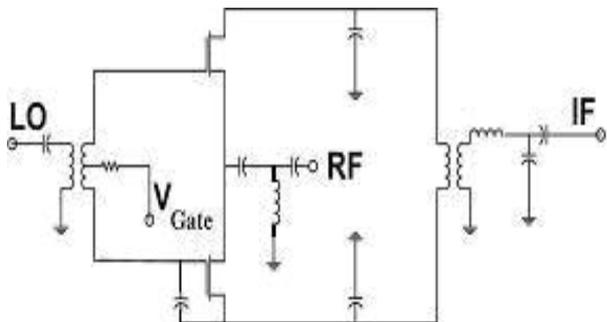


Fig. 6. Mixer schematic with LO/IF balancing. The additional capacitor is used for isolation improvement.

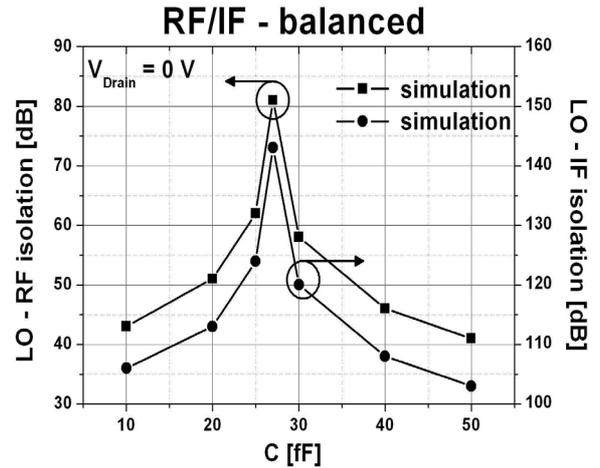


Fig. 7. LO-IF- and LO-RF-isolation vs. capacitance C ; RF/IF-balanced mixer with gate bias $V_{Gate} = -2V$, drain bias $V_{Drain} = 0V$ and LO-power of 15 dBm.

The diagrams in Fig. 8 show the input third order intercept points (IIP3) of both mixer types. A very high IIP3 of up to 44 dBm was measured for the RF/IF-balanced mixer at a drain bias of 4 V and a LO-power of 19.5 dBm. 38 dBm IIP3 was achieved for the LO/IF-balanced mixer at 21.5 dBm LO power. Because of these high IP3 values measurements have to be performed very carefully and IP3 responses of the measurement equipment have to be eliminated from the response of the DUT. This has been done by using Agilent's ESG/PSA measurement equipment providing multi tone and pre-distortion capabilities [6] for eliminating the system errors. Therefore, a high grade of repeatability and reliability could be stated referred to the measurements. On the other hand, this is not true for the simulations. In summary, the ADS based IP3 simulations were very time consuming, unstable and partly inconsistent – all in all not satisfactory especially not with increasing LO-level. It could not be cleared up finally whether this is due primarily by the model or by the harmonic balance simulator. Nevertheless we have added the IP3 simulations to Fig. 8 but we emphasize once more, that they should be seen based on our comments given above.

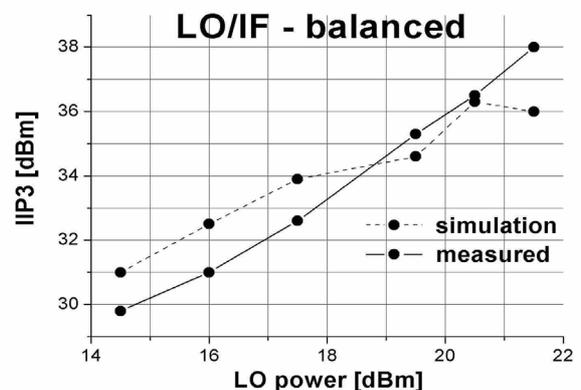


Fig. 8a. IIP3 vs. LO power; LO/IF-balanced mixer with gate bias $V_{Gate} = -2V$.

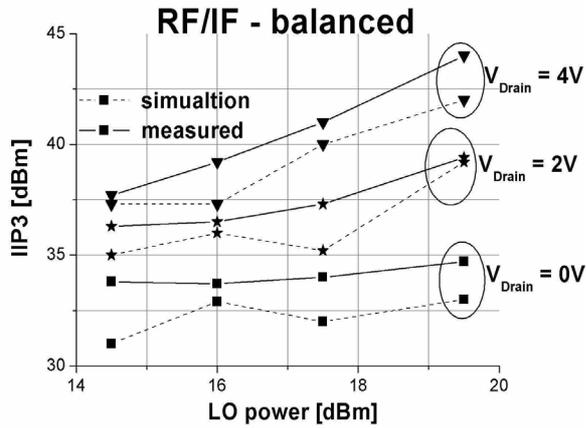


Fig. 8b. IIP3 vs. LO power; RF/IF-balanced mixer with gate bias $V_{Gate} = -2V$ and drain bias $V_{Drain} = 0V, 2V,$ and $4V$.

It can be taken clearly from Fig. 8b that the IP3 values increase with increasing drain bias voltage. This is a consequence of enhancing the usable linearity range of the FET characteristic compared to operation at zero bias. Tab. I summarizes the achieved results.

	IIP3 [dBm]	LO-RF isolation [dB]	LO-IF isolation [dB]	Conv. loss [dB]
LO/IF – balanced	38	39	60	7
RF/IF – balanced	44	46	80	7.5

Table I

Performance comparison of the two mixer types.

IV. CONCLUSION

Two single balanced passive GaAs FET mixers for the lower GHz range have been designed, built up and measured. Conversion losses down to 7 dB, good port isolation and very high IP3 values up to 44 dBm have been achieved. The isolation values can be improved considerable by a simple compensation method. It has been shown, that DC drain biasing can improve the linearity behavior of the RF/IF-balanced mixer. Unfortunately, ADS based IP3 harmonic balance simulations were not reliable and unstable.

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