"Dual chip Ku-band Predistortion Linearizer"

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1. Introduction

Predistorion linearizers constitute an increasingly important building block of most satellite communication payloads. They enable an improved output amplifier linearity, thereby reducing power consumption requirements and increasing the transmit output power, while maintaining the required intermodulation performance. A novel MMIC lineariser chip [1] has been used in conjunction with a MMIC analogue phase shifter to implement a complete predistortion linearizer. The linearizer chip has been designed at ESTEC, and manufactured by Thomson foundry (F) (today UMS) using their MMIC process LN05. The analogue phase shifter chip has also been designed at ESTEC and manufactured by Daimler Benz (D) (today UMS) using their process E05. The capabilities of this linearizer have been demonstrated by integrating it with a Ku-band Travelling Wave Tube Amplifier (TWTA).

2. Ku-band MMIC linearizer

The Ku-band MMIC linearizer layout is shown in fig.1. It is a single bridge, predistortion linearizer where the non-linear path and the linear path active elements are constituted by two MESFETs with different gate widths. In this way it is possible to have, over a certain input power range, the smaller device operating in its non-linear region whilst, over the same input power range, the larger device operating in its linear region, [2], [3], providing the necessary signals for the correct operation of the linearizer.

The input and output couplers have been implemented using lumped elements to minimise the chip area. These couplers have an input impedance of 50Ω and output impedance of 100 Ω, thus reducing the number of capacitors in each coupler by a factor of two. Further more, the capacitors remaining at the coupler output ports are embedded within the linear and non-linear branch matching networks, further reducing the number of components and, hence, the chip size.

For this simple chip, the tuning of the predistortion characteristics can be obtained with an external 100 Ω transmission line, on an alumina substrate, adjustable in length by using bonding wires, connected in series with the non-linear signal path. This provides a variable phase-shift of the signal in the non-linear path of the circuit. With this approach, due to the discrete steps of the external line length, a mild linearization effect has been already demonstrated [2], adequate for a coarse linearization of power amplifiers.

For a more accurate linearisation, the transmission line should be replaced by an analogue phase shifter. For this purpose, a Ku-band MMIC analogue phase shifter has been designed with input/output connections fully compatible with the MMIC linearizer block, to substitute the external tuning line.

3. Ku-band phase shifter design

The analogue phase shifter design was based on a lumped LC all-pass network configuration [4]. With this configuration (figure 2) and by using spiral inductors and bias-dependent capacitance, (i.e. $C(V_d)$ of reversed-biased Schottky diodes), the resonant condition of the all-pass network can be controlled. This is given by equation 1.

$$\omega_o = \frac{1}{\sqrt{L \cdot C(V_d)}} \qquad (1)$$

Indeed, once such a resonant condition is satisfied, the phase can vary as a function of the diode's capacitance value in accordance with the following expression:

$$\Delta\phi = \frac{4}{C(V_d)} \cdot \Delta C \qquad (2)$$

This approach allows a continuos phase shift from 0 to 90 degrees using a single bias supply to control the variation of 4 parallel Schottky diode' capacitance. By adopting two cells in series, a total 180 degrees phase shift has been obtained in a very compact structure, and a resulting small chip area.

Since the impedance match condition of the LC all-pass network is given by the expression:

$$Z_o = \sqrt{\frac{L}{C(V_d)}} \qquad (3)$$

special attention must be given in the design of the input and the output matching networks to assure a good VSWR for all bias conditions (from 0 to 180 degrees of phase shift).

The MMIC has been realized using the E05 process from Daimler Benz foundry which is a recessed gate MESFET technology with 0.5 μm gate length and 150 μm substrate thickness. It allows the implementation of air bridges and via holes. It is intended for low noise and switching applications up to 18 GHz.

The analogue phase shifter has been matched to 100 Ω at both the input and the output to be compatible with the linearizer chip.

The layout of the MMIC analogue phase shifter is shown in figure 3. The chip tile includes two versions of the phase shifter. The first version is the 90 degrees analogue phase shifter cell used for on-wafer testing. the second version is the complete 180 degrees analogue phase shifter for utilization in the predistortion linearizer. The total chip area is 1.1x1.3 mm^2.

In figures 4 and 5 the on-wafer measurements performed at ESTEC on the 90 degrees cell are reported. The overall analogue phase shift of 90 degrees is obtained when the bias varies from 0.5 V to -4 V. The bias control range is limited by the diode breakdown voltage equal to -5 V.

A maximum insertion loss of the order of 3.7 dB and a maximum input/output return loss of the order of -7 dB has been measured on-wafer at Vdd=-4 V. The use of bonding wires at the input and output RF pads, taken into consideration in the design, improved the maximum insertion loss to 3 dB and the maximum return loss below -13 dB. The maximum phase variation versus frequency is 8 degrees/250 MHz.

Measurements on the 180 degrees analogue phase shifter have shown an overall analogue phase shift from 0 to 180 degrees within the same range of bias variation. The maximum insertion loss is of the order of 6 dB and the input/output return loss is below -13 dB, within the frequency bandwidth 12.25 - 12.75 GHz.

4. Integration of the dual-chip linearizer

The MMIC linearizer chip has been integrated with the MMIC analogue phase-shifter in a MIC test-jig. A picture of the two chips assembled is shown in fig.7.

Following the integration, the complete dual-chip linearizer has been measured with different bias settings (Vg1 and Vg2 of the MMIC linearizer chip, and bias voltage of the phase shifter) to explore the complete tuning capabilities. Fig.8 shows, for example, the gain expansion obtainable by the linearizer for various phase shifter settings, while keeping almost constant phase behaviour (fig.9), for Vg1=Vg2=-0.35 V.

5. Integration with a Ku-band TWTA

To demonstrate its capabilities, the dual-chip linearizer has been connected to a Ku-band TWTA which was previously characterized in terms of AM/AM, AM/PM, and intermodulation performance. Using these characteristics, the choice of the linearizer setting has been obtained by computer simulation, by means of the ESTEC developed software CASCA and IMAL-2 [6].

The setting has been selected to maximise the overall AM/AM curve linearity of the TWTA plus linearizer.

Fig. 10 and fig. 11 show the comparison of the AM/AM and AM/PM characteristics, respectively, before and after linearization.

Fig.12 shows the two-carrier, third and fifth order C/I of the TWTA and the TWTA plus linearizer. To maintain a 3rd order C/I of 20 dBc, the output power of the TWTA may be increased by 1.8 dB after linearization. For a typical space TWTA this corresponds to an increase of power added efficiency of about 5 %, which yields a very significant reduction in power consumption.

In figure 12 the comparison with the simulations performed using IMAL2 is also given. The difference are within the numerical tolerance of the tool and are also justified by the limitation of the standard measurement systems for AM/AM and AM/PM single carrier characteristics.

6. Conclusions

A dual-chip Ku-band predistortion linearizer has been developed and tested in conjunction with a TWTA. The linearizer is based on two MMIC devices, a MMIC linearizer chip and a MMIC analogue phase shifter, developed at ESTEC.

Good performance and consistency with predicted results have been obtained for the two chips and for the complete linearizer. Following this successful demonstration, a version of the linearizers using the same conceptual design and operating at C-band is now under development at ESTEC [7].

7. References

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2. G.Gatti, ESA-ESTEC: *A novel MMIC predistortion linearizers*, Proceedings of 5th International Workshop on GaAs in telecommunications, Rome, Italy, April 1995
3. G.Gatti, ESA-ESTEC: *A New Predistortion Linearizers* , ESA Preparing for the Future, Vol.5, no.4, December 1995.
4. N.E.Hodges, M.H.Yam: *A precise analogue phase shifter for SHF SATCOM Phased array*, Proceedings of 1992 IEEE GaAs IC Symposium, Miami, Florida USA
5. G.Gatti ESA-ESTEC: *Dual-chip Ku-band predistortion linearisers*, ESA XRM Technical Notes, Vol.VI, no.3, February 1997
6. G.Gatti, W.Bosch: *IMAL-2*, ESA XRM Technical Notes, Vol.V, no.6, June 1996
7. C.Dana, F.Coromina (ESA-ESTEC): *C-band MMIC lineariser,* ESA XRM Technical Notes, Vol.VI, no.5, April 1997

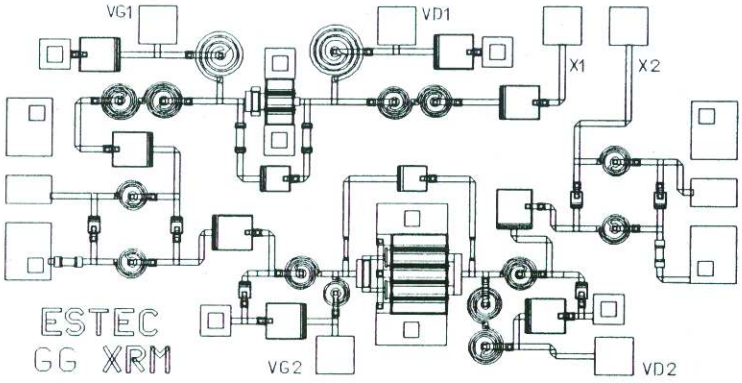

Figure 1 - MMIC linearizers

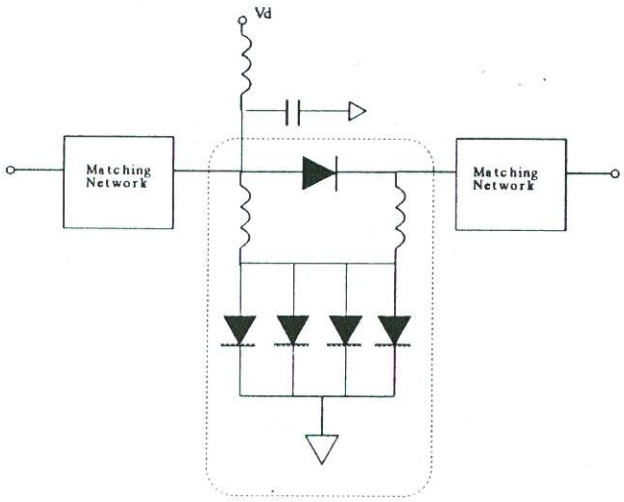

Figure 2: LC all pass network configuration including matching network

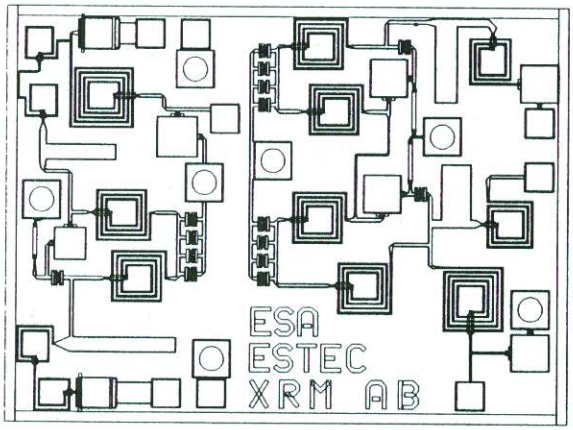

Figure 3: MMIC analogue phase shifter

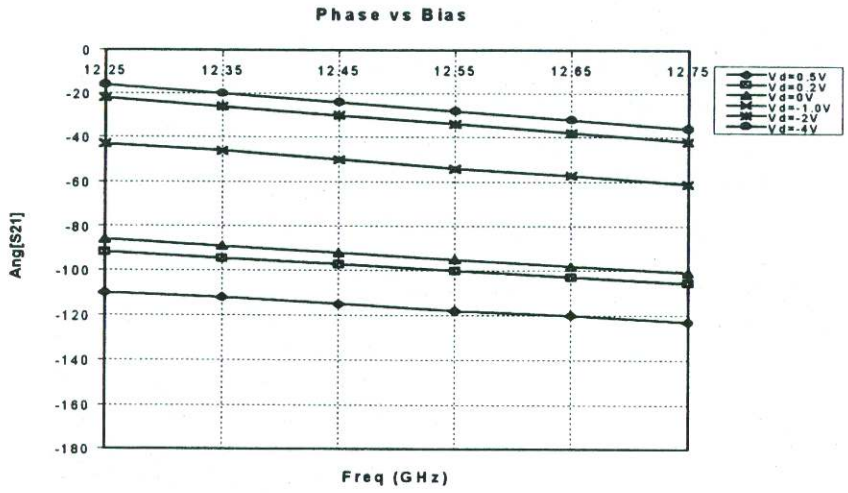

Figure 4: 90 degrees phase shifter cell: Phase vs. Bias (on-wafer measurements)

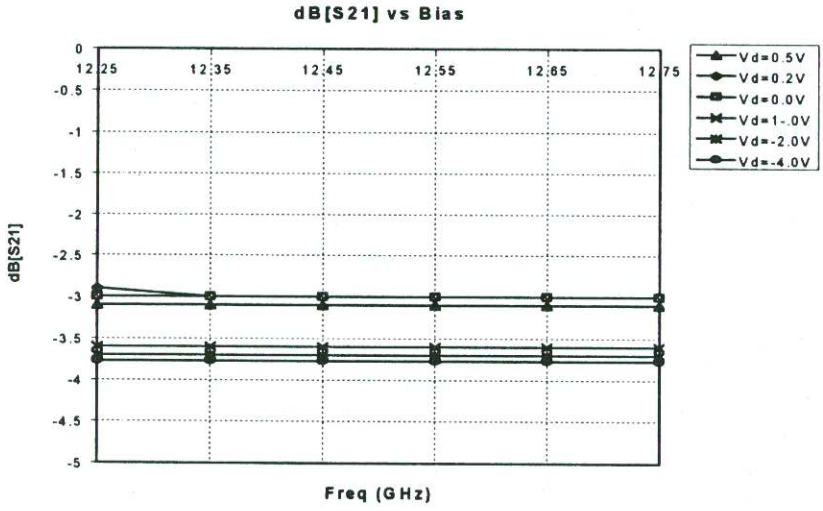

Figure 5: 90 degrees phase shifter cell: Insertion Loss vs. Bias (on-wafer measurements)

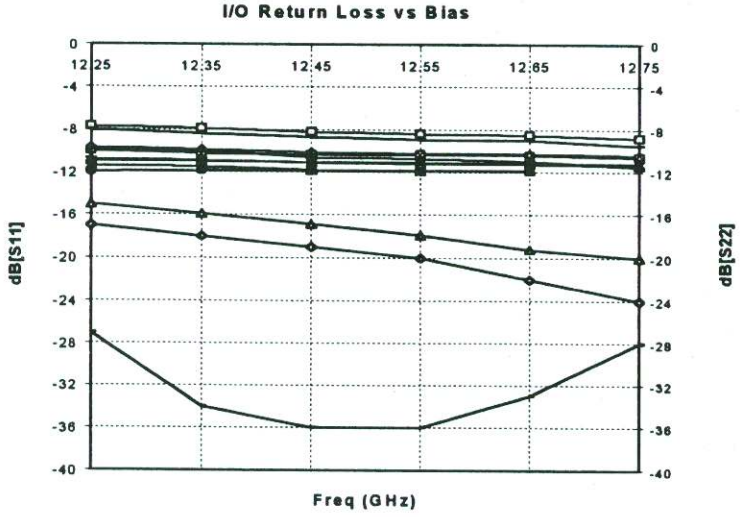

Figure 6: 90 degrees phase shifter cell: Return Loss vs. Bias (on-wafer measurements)

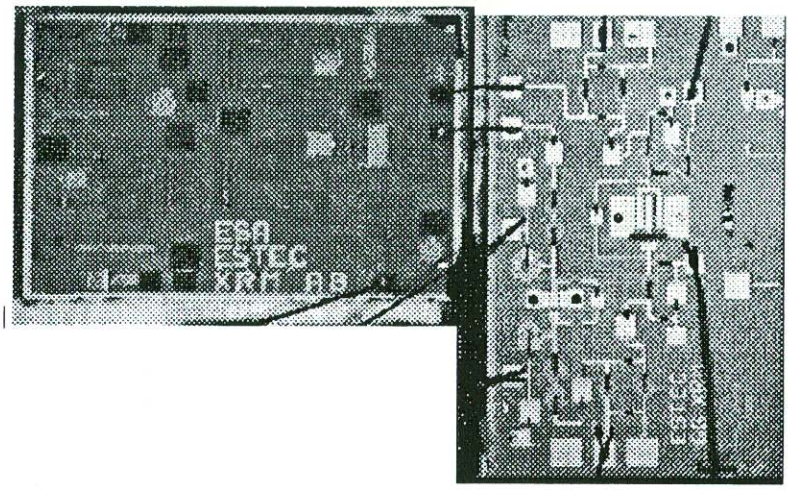

Figure 7: picture of the two chips assembled

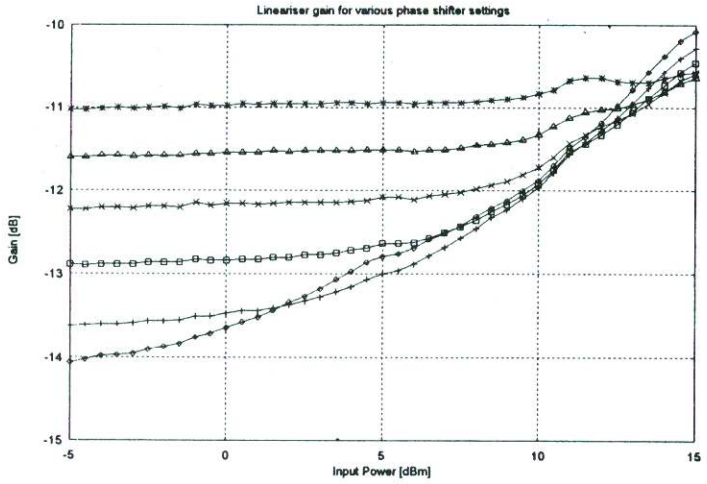

Figure 8: linearizers AM/AM for various phase shifter settings

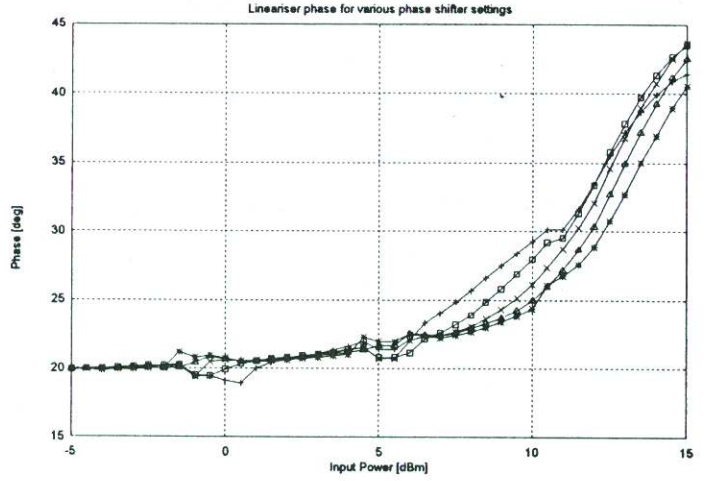

Figure 9: lineariser AM/PM for various phase shifter setting

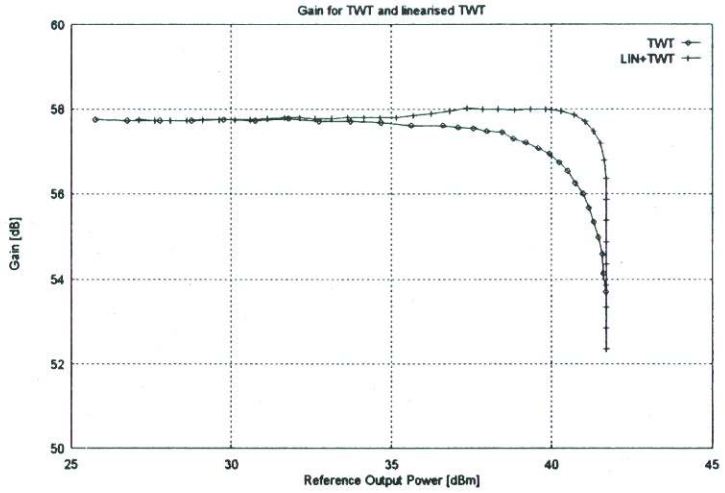

Figure 10: gain of TWTA and linearised TWTA

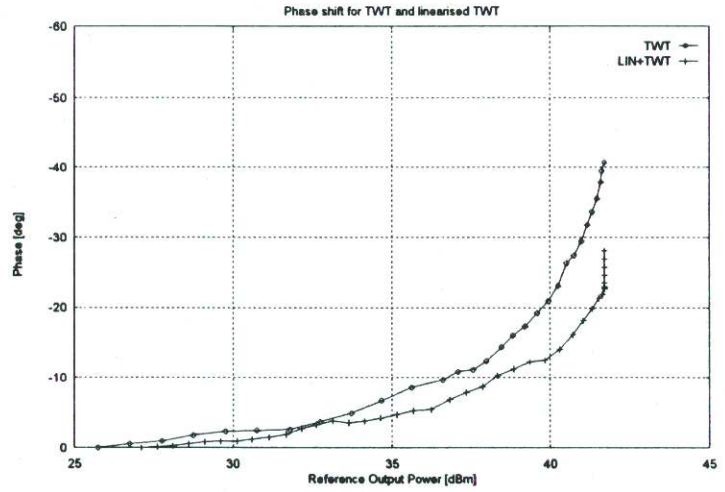

Figure 11: phase shift of TWTA and linearised TWTA

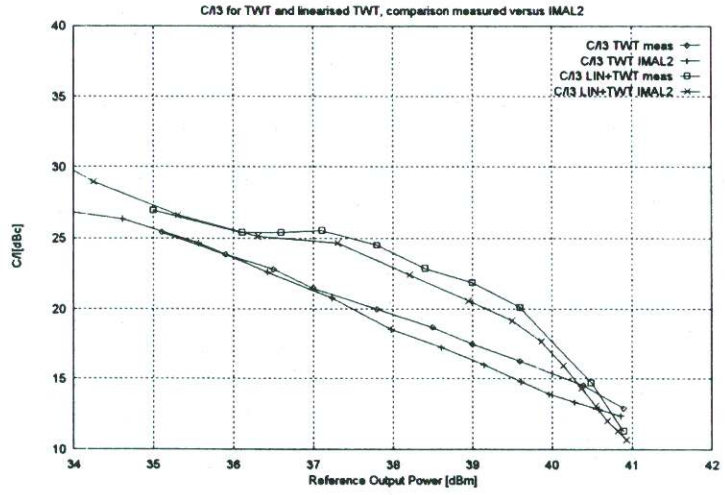

Figure 12: C/I3 and C/I5 of TWTA and linearised TWTA and IMAL-2 simulations