Implementation of non-conventional nonlinear models for electron devices in commercial CAD tools

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Abstract — **In nowadays CAD environments for integrated microwave circuit design, dedicated tools for the implementation of user defined component models are becoming more and more important. These tools are mainly oriented to the definition of equivalent circuit models. However, the need for more accurate prediction of nonlinear electron device performance pushes the modelling community towards the research of new, often non-conventional, modelling approaches (e.g., frequency-domain, behavioural, integral models, look-up-table based, state-space based, etc.). In such a context, the model implementation tools usually available may result not sufficiently flexible. The paper provides useful hints and points out the main limitations which can be encountered in the implementation of non-conventional electron device models. As an example, the implementation of a Nonlinear Discrete Convolution model will be considered by using three different advanced tools: the Model Wizard of AWR Microwave Office, the Model Development Kit and Verilog-A Language of Agilent ADS.**

I. INTRODUCTION

The research activity related to CAD techniques is getting more and more important and the improvement of commercial CAD tools is becoming a basic element of the communication circuit design activity. Useful simulation results can only be achieved with accurate device models and non-ambiguously determined model parameters. Many different models have been proposed over the years and the modelling engineer has different choices for a certain type of transistor. Moreover, many modern simulators allow the definition and implementation of user-defined models by using Symbolically Defined Devices (SDDs) or compiled models (typically in C language). Currently, standardization attempts are underway to develop a language known as HDL-A (Hardware Description Language for Analog Applications) that can be recognized by many simulators.

These approaches are typically well suited for conventional microwave electron device models. In fact they easily enable the implementation of those charge control equations that represent the theoretical basis of most equivalent circuit models. On the contrary, some problems may exist when other approaches are adopted to describe the microwave electron device behaviour. For example the implementation of black-box, look-up-table based behavioural models, which are usually defined on the basis of a general mathematical approach, it is not so easy and straightforward.

This paper deals with issues related to the implementation of advanced, non-conventional electron device models in commercial CAD environments and points out the main difficulties which limit their flexibility. Commercial CAD environments make built-in tools available for electron device model implementation which however show limitations in handling some of the mathematical instruments needed in non-conventional models (e.g., look-up table structures, delayed functions, filtering functions, etc..) [1..7]. The non conventional model considered as an example in this paper is the Nonlinear Discrete Convolution Model (NDC), whose validity is confirmed by accurate simulations and experimental results [2]-[8].

II. NDC MODEL OVERVIEW

A brief summary of the Nonlinear Discrete Convolution model formulation is here recalled. The time-domain current/voltage relationship of a single port electron device can be expressed as:

$$i(t) = \Psi\left|v(t-\tau), V_0, \vartheta_0\right|_{\tau=0}^{T_M} \tag{1}$$

or, equivalently as:

$$i(t) = \tilde{\Psi}\left|v(t), v(t-\tau)-v(t), V_0, \vartheta_0\right|_{\tau=0}^{T_M} \tag{2}$$

where $\Psi|\cdot|$ ($\tilde{\Psi}|\cdot|$) is a suitable functional, which represents the nonlinear dependence of the device current i at the generic instant t on the present and past values of the applied voltage $v(t-\tau)$ over a virtually infinite memory time interval T_M. The dependence of the current $i(t)$ on the average voltage component V_0 and average channel temperature θ_0 has been introduced to describe in a simplified way the low-frequency dispersive phenomena due to "traps" and thermal effects.

The NDC model derives from the basic hypothesis that, apart from low-frequency dispersion and linear parasitic elements which are usually modeled separately, all the other device dynamics is limited to a memory time T_M which is not only practically finite, but also relatively short (i.e., much shorter than the period of the typical operating signals). The validity of such an hypothesis is well verified for the voltage-controlled intrinsic device.

Under the assumption of short T_M values, the voltage deviations $v(t-\tau)-v(t)$ have the property of keeping small even under large signal amplitudes. This enables (2) to be linearised with respect to $v(t-\tau)-v(t)$ leading to a finite memory nonlinear model which has been proved to accurately describe the behavior of very different electron devices. In fact, suitable values of T_M can be found for which the errors due to both memory truncation and linearisation with respect to the dynamic voltage deviations are small enough. Moreover, to make both model extraction and implementation feasible, the memory time of the nonlinear intrinsic device is divided into a suitable number N_D of intervals of width $\Delta\tau$. This leads to the model formulation proposed in [2]:

$$\begin{aligned} i(t) &= F^{LF}\left[v(t), V_0, \vartheta_0\right] \\ &+\sum_{p=1}^{N_D} g_p\left[v(t)\right]\cdot\left[v(t-p\Delta\tau)-v(t)\right] \\ &+\Delta i_{par}(t) \end{aligned} \tag{3}$$

The term $F^{LF}[v(t);V_0,\theta_0]$ in (3) describes the device behavior at DC and low-frequency operation[1]. Different approaches have been developed to define the F^{LF} characteristic [9]-[10].

The second term in (3) represents a discretised purely-dynamic single-fold convolution integral between voltage deviations and a "pulse response function" $g[v(t),\tau]$ nonlinearly-controlled by the instantaneous applied voltage. This term accounts for purely-dynamic nonlinear phenomena which are important at high frequencies. An additional current contribution $\Delta i_{par}(t)$ has also been included in (3) in order to account for the possible presence of a parallel parasitic linear network.

The NDC model can be easily identified on the basis of conventional DC and bias dependent small-signal parameter measurements [2].

III. The Model Wizard MWO Implementation

In the MWO environment a special purpose tool, called "Model Wizard" [11], is available for linear and nonlinear model implementation in the form of dynamically linked models. The wizard enables all the parameters, variables and components used by the model, to be defined by using a SPICE-netlist-like description. In particular nonlinear models are created by combining one or more nonlinear controlled current sources with any number of linear components.

The first two different contributions of the intrinsic NDC model in (3), i.e. the $F^{LF}[v(t),V_0,\theta_0]$ characteristic and the purely-dynamic term, were implemented by using the wizard netlist; the model data are saved in memory in a look-up table form. Fig.1 shows the components which describe the static characteristics and the LF dispersion. In particular it shows the way to define the mean values of the intrinsic voltages (using Low-Pass Filters) and the average dissipated power (using an auxiliary current generator, a 1Ω resistor, a Low-Pass Filter and a current probe) which appear in the description of the dispersive phenomena [9]-[10].

The purely-dynamic contribution of the model consists in N_D current generators, shown in Fig.2, and placed between Drain and Source to describe $I_d(t)$. The current depends on the pulse response function matrix $g_p(v_g,v_d)$ and on the delayed terms of the gate and drain voltages, which are obtained by means of ad hoc components. A similar structure is defined for the gate current. A value of $N_D=3$ was found to be a good trade-off between model accuracy and complexity. It is necessary to add the parallel parasitic linear network and the passive extrinsic network to complete the active device model as indicated in [2].

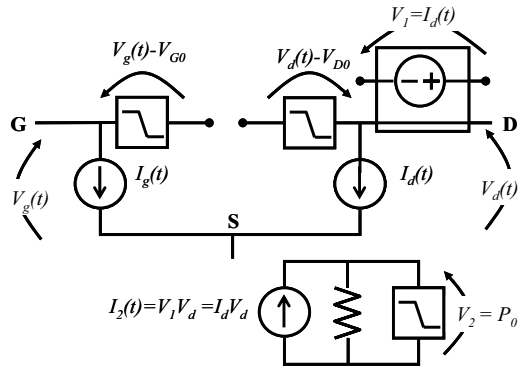

Fig.1. Equivalent scheme for the implementation of the quasi-static characteristic in the Wizard Model.

The Wizard implementation is quite involved, especially in the description of the dispersive phenomena, while the presence of built-in delay elements allows for a very straightforward implementation of the dynamic part of the model. However, it must be outlined, that the Wizard implementation is the only possible solution for implementing look-up table based models [1]-[2]-[4]-[6] in the MWO environment. Indeed, look-up-table based schematic elements are not available within MWO.

IV. The ADS model Implementations

The NDC model implementation in the ADS environment by means of SDD schematic elements has been described in detail in [2].

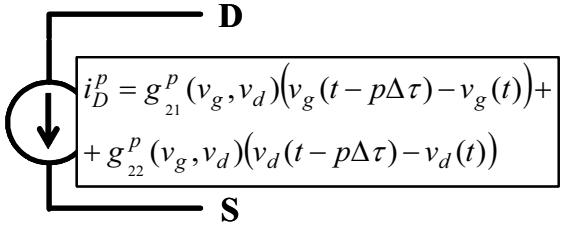

Fig. 2. The p-th generic current source used to implement the high frequency nonlinear dynamic drain current.

[1] Above the frequency cut-off of dispersive phenomena due to traps and self-heating (e.g. 1MHz), yet displacement currents are still negligible.

Two new ADS implementations of the NDC model will be presented in this section. They are based on the Model Development Kit and the Verilog-A language.

The Model Development Kit for User Compiled Models (UCM) [12] is a graphical tool that allows the definition of the model parameters, the model symbol and the model pins. It also creates a template C code which has to be filled by the user, inserting the model equations in proper template fields. The C code is then compiled and linked to a supplied object code, in order to create a dynamically linked library.

The User Compiled Model implementation needs different portions of codes for each type of analysis. The implementation described in this paper concerns the nonlinear and linear analyses, suitable for Harmonic Balance and S-parameter CAD setup, respectively.

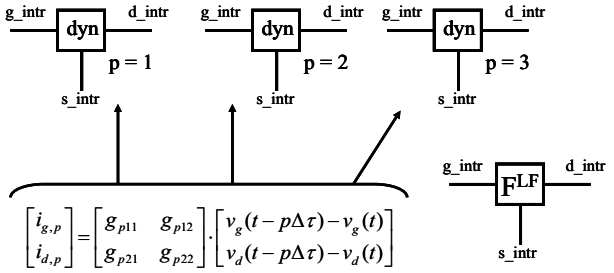

Fig. 3.ADS User Compiled Model implementation.

The UCM nonlinear implementation of the NDC Model is conceptually simple. The model equation (3), defined for the two-port device case, is split up into separate static/low-frequency dispersion contributions and purely dynamic nonlinear effects. This enables two user compiled elements to be defined: a first one which implements the F^{LF} function and a second one that defines the arguments of the summation in (3). The final intrinsic NDC Model is obtained by connecting in parallel the *LF* block, the N_D purely dynamic nonlinear blocks and the Parallel Parasitic Linear Network. This implementation is shown in Fig.3. The model parameters are allocated, as in the Model Wizard implementation, in dynamic look-up table structures.

The implementation of a model with good convergence properties into an Harmonic-Balance nonlinear analysis tool, requires the definition of the exact Jacobian matrix of the model. This makes the definition of a non-conventional model complex because the calculation of a number of derivatives is proportional to the number of netlist nodes and the definition of numerical derivative algorithms are needed. Moreover, the lack of dedicated functions makes the evaluation of the delayed voltages and consequently the netlist definition somehow cumbersome.

The UCM linear implementation of the NDC Model requires a Y-matrix formulation of the model around the chosen bias condition. Thus, the model equation (3) has been linearised around the bias condition and evaluated in the frequency domain. It must be observed that the use of a separate program code for each type of analysis, makes it also possible to define an exact small-signal model by directly implementing the bias-dependent measured Y matrix in a look-up table based structure.

Verilog-A is an Hardware Description Language that enables the designers of analog systems to create and use modules which encapsulate high-level behavioral descriptions as well as structural representations of systems and components. The behavior of each module is described mathematically in terms of voltages and currents at the device ports and external parameters applied to the module.

The implementation in Verilog-A [12] of the NDC Model is very simple. In fact, the current expression (3) modified for a two-port device, can be directly implemented in this case. Differently from previous implementations, the Verilog-A language provides a series of predefined functions (as delays and filters) that avoid the need for schematic components. Unfortunately, the present Verilog-A release (E8886A/AN/T compiler) in ADS does not include yet the fundamental I/O functions for accessing external data files. Thus, the look-up-table values of the static currents and dynamic non-linear conductances have been so far implemented by means of arrays directly in the Verilog-A source code[2].

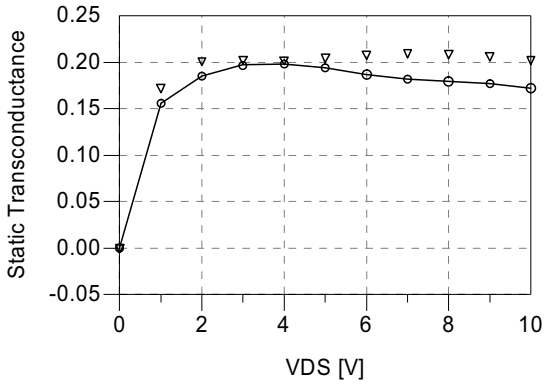

Fig. 4. Static transconductance values (Vds = 0 to 10 V, Vgs = -0.6 V) measured (continuous line) and simulated by means of the SDD (triangles) and UCM implementation (circles).

When user-defined accurate interpolating algorithms are needed [13], as very often happens when using look-up-table based models, the compiled implementation is the only possible solution since ADS-based Data Access Components (DAC) only provide linear or spline interpolators. Moreover, the compiled implementation also gives the opportunity of defining suitable, highly-accurate derivative algorithms different from the ones adopted in the CAD environment. As an example Fig.4 compares the measured device transconductance with the simulated one provided by the ADS SDD and UCM

[2] The insertion of very-large arrays in a single Verilog-A code may cause system crash during the code execution. Different modules, each one holding a subgroup of arrays corresponding to the LF and HF current sources were defined.

model. The discrepancy between the SDD model and measurements is due to the coarse bias grid and to the linear interpolator adopted. The same level of accuracy of the UCM model could be obtained by increasing the grid density and using a spline interpolator in the SDD model.

Simulation times (with a Pentium4 PC at 2.8GHz with a Windows XP operating system) required by the three implementations discussed above, are shown in Table I. As it can be seen an excellent time improvement (with the same simulation accuracy) can be obtained with the C-compiled implementations with respect to the Verilog-A language implementation: this is particularly evident for the HB simulations. Anyway, the novel implementations give an improvement in simulation time of several order of magnitudes with respect to previous SDD implementations in ADS.

Simulation	Verilog-A	C-code Compiled (UCM/Wizard)
DC Vgs = -1.5 V – 0 V, step = 0.3 V Vds = 0 – 11 V, step = 0.5 V	*~40 sec*	*~10 sec*
S parameter Freq = 1 GHz – 50 GHz, step = 1 GHz	*~100 sec*	*~5 sec*
HB single tone Freq = 39 GHz Power = -6dBm – 10dBm, step 1dBm	*~300 sec*	*~10 sec*
HB intermodulation Prediction F1= 39 GHz F2=39.01GHz Power = -6dBm – 10dBm, step 1dBm	*~4 hours*	*~40 sec*

Table I. Simulation time comparison between different electron device model implementations.

V. Conclusion

The implementation of a non-conventional electron device model in different CAD environments has been described. In particular the model has been implemented by means of the Model Development Kit and the Verilog-A language used in Agilent's ADS2003C and the Model Wizard of AWR's Microwave Office.

Despite the implementation procedures require quite a lot of work and a good knowledge of programming languages, a considerable improvement in simulation speed has been obtained with respect to previous implementations.

The advantages/disadvantages pointed out for the examined implementation tools provide useful hints for nonlinear model implementation with particular emphasis on non-conventional models.

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