A low-noise X-band microstrip VCO with 2.5 GHz tuning range using a GaN-on-SiC p-HEMT

A.P.M. Maas, F.E. van Vliet

TNO Defence, Security and Safety, Oude Waalsdorperweg 63, 2597 AK Den Haag, Netherlands, +31703740000

***Abstract* — A low-noise X-band microstrip hybrid VCO has been designed and realised using a 2 x 50 µm GaN-on-SiC pseudo-morphic HEMT as the active device. The transistor has been manufactured by TIGER and features a gate-length of 0.15 µm, an f_T of 22 GHz, a break-down voltage of 42 Volts and an I_{dss} close to 1 A/mm. The VCO has been assembled with standard SMD reflow and chip-on-board technology on Rogers 4003 substrate material. The circuit is biased at +15 Volts and 38 mA and has a measured tuning range from 8.1 to 10.6 GHz, an output power level of +19 dBm and an average phase-noise level of -114 dBc/Hz @ 1 MHz offset.**

I. Introduction

As part of a large European consortium, investigating the properties and possibilities of using GaN for low-noise applications in microwave systems, an X-band VCO is designed in order to evaluate the phase-noise performance realisable with this technology.

II. Active Device Technology

The active device is manufactured by TIGER, which is a cooperation between THALES and IEMN on Gallium Nitride technology research. In comparison with GaAs, GaN has much higher breakdown voltages (up to 10x), resulting in higher output power densities. The noise behaviour of the technology has not been fully investigated yet, and this work is part of such an investigation.

Several samples from TIGER have been measured using a microwave on-wafer probe-station. These GaN devices have a gate-length of 0.15 µm, a gate-width of 2 x 50 µm and have been grown on a Silicon-Carbide (SiC) substrate. Some measured and extracted basic DC and RF parameters are shown in table 1.

parameter	value	unit	conditions
I_{dss}	94	mA	V_{ds} = 6V, V_{gs} = 0V
V_{po}	-5.5	V	V_{ds} = 12V, I_{ds} = 0.01 * I_{dss}
g_m	20	mS	V_{ds} = 12V, I_{ds} = 0.50 * I_{dss}
f_T	22	GHz	V_{ds} = 12V, I_{ds} = 0.50 * I_{dss}
$V_{dg, breakdown}$	> 42	V	V_{gs} = -7V

TABLE I
MEASURED 2 X 50 MICRON GAN DEVICE PARAMETERS

III. Oscillator Design

The VCO design is based on the negative impedance approach. The transistor is embedded in a network with source series feedback, effectively creating a negative input impedance at the gate. At the input of this network, a microstrip resonator is coupled to define the frequency and conditions for oscillation. Then the output network is designed for optimum output power efficiency to the 50 Ohms load. Several design iterations (simulations) are needed to achieve the desired performance.

Both Agilent's ADS and Orcad's PSpice were used to design and predict the performance of the oscillator. Simplified models for varactor and transistor were extracted from measured DC and S-parameters.

In ADS, only the measured s-parameters were used to model the transistor. The approximate large-signal s-parameters were generated by modifying the magnitude of S_{21} to simulate 1 to 6 dB of forward gain compression in steps of 1 dB. Using this approach, the amount of gain compression and the frequency at which the oscillation will take place, can be estimated. To minimise the level of phase-noise due to upconversion of low-frequency noise sources inside the circuit, the angle at which the resonator impedance-versus-frequency line and the inverse of the transistor input impedance-versus-compression line cross in the Smith Chart (at the frequency of oscillation) should be as close as possible to 90 degrees over the complete tuning range of the VCO (for every frequency within the tuning range of the VCO).

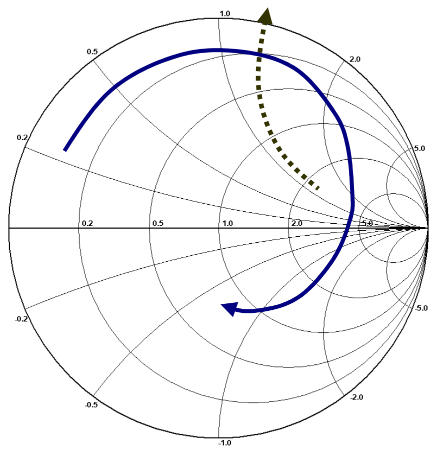

Fig. 1. Smith Chart analysis of the VCO circuit. (dotted line: inverse of the negative input impedance vs increasing gain compression of the transistor for one frequency. solid line: the reflection vs frequency of the resonator)

In order to avoid unwanted resonances other than from the resonator itself, 0402 lumped element components are used for most biasing/decoupling parts of the VCO. Several 10 Ohms resistors are used to damp any resonances that might occur somewhere in the bias circuits.

The FET is self-biased by a source resistor, and is set at roughly 45 % I_{dss} (40 mA) and a V_{ds} of 12 V. With these values, a reasonable power dissipation of around 400 mW is achieved, which should be low enough to avoid excessive channel temperatures. The varactor is a MA46H200 hyperabrupt GaAs type from M/A-Com, with a typical Q of around 15 at 10 GHz. The overall unloaded Q of the resonator (varactor, microstrip line and bias circuits) will not be better than 10.

Based on the modified equation from Leeson (1), it is possible to make a rough estimate of the SSB phase-noise level of the oscillator:

$$L(f_m) = 10\log\left\{\left[1+\frac{f_0^2}{(2f_m Q_l)^2}\right]\left(1+\frac{f_c}{f_m}\right)\left[\frac{FkT}{2P_{sav}\left(1-\frac{Q_l}{Q_u}\right)}\right]+\frac{2kTRK^2}{f_m^2}\right\} \quad (1)$$

f_0 = center frequency (Hz),
f_m = modulation frequency (Hz),
f_c = 1/f corner-frequency (Hz),
Q_u = unloaded quality factor of resonator,
Q_l = loaded quality factor of resonator,
P_{sav} = average signal power (W),
F = large-signal noise factor of the active device,
k = Boltzmann's constant (J/K),
T = operating temperature (K),
R = effective noise resistance of varactor (Ohms),
K = VCO modulation sensitivity (Hz/V).

Based on the known VCO parameters and taking 10 dB for the estimation of the large-signal noise factor of the GaN device, 5 MHz as its 1/f corner-frequency and 1000 Ohms for the noise-resistance of the used varactor (typical value), the estimated phase-noise is calculated and plotted in figure 2.

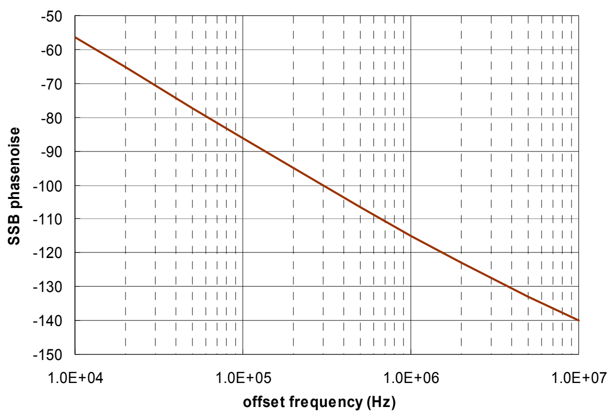

Fig. 2. Predicted GaN-VCO SSB phase-noise level versus offset frequency.

In PSpice, a simple transient model was generated for both the GaN transistor and the selected GaAs varactor from M/A-Com. Using this circuit, the design was analysed in the time-domain, enabling a check of correct start-up of the oscillation and of the existence of possible spurious modes.

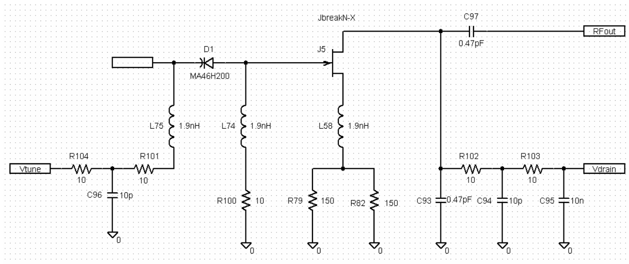

Fig. 3. Simplified lumped element schematic of the VCO.

The predicted oscillator frequency and output power by this simulation is not very accurate. In the complete schematic used in the PSpice simulation (not shown here), all transmission lines are modelled by multiple L-C-R sections and the basic parasitics of every physical component are included. The simulated oscillator output power level and frequency versus tuning voltage is shown in figure 4.

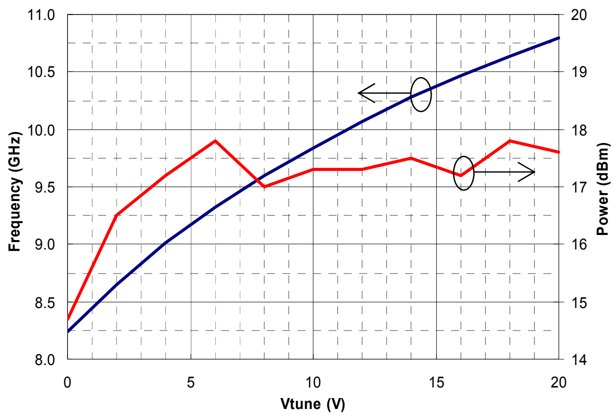

Fig. 4. PSpice simulated VCO frequency and output power versus tuning voltage.

In figure 5, the completed layout is shown of the circuit, including a 6 dB π-attenuator (with 0402 resistors) and a surface-mount SMP-type output connector. The 6 dB attenuator has been included to reduce the influence of the connector and cable mismatch on the VCO performance due to load pulling effects.

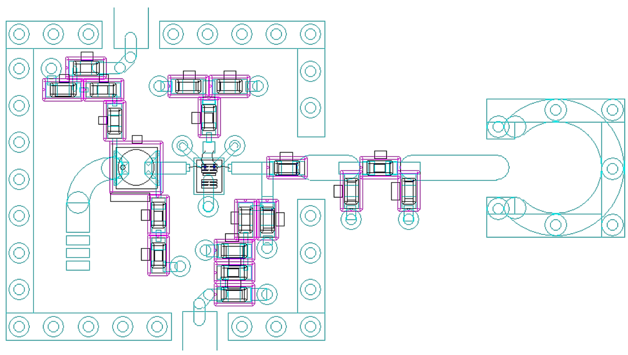

Fig. 5. Layout design of the VCO.

IV. Oscillator Assembly

The mechanical design of the VCO is based on standard chip-on-board and surface-mount technology. The printed-circuit-board material used is RO4003 (manufactured by Rogers Corporation). The substrate thickness is 0.508 mm (20 mil) and the Copper layer thickness is 17.5 µm (0.5 oz). All via's are 0.5 mm diameter plated and the Copper surface is finished with bondable Gold plating (2 µm thickness). All components are mounted using a manual surface-mount pick-and-place workstation and soldered in a standard infra-red reflow oven.

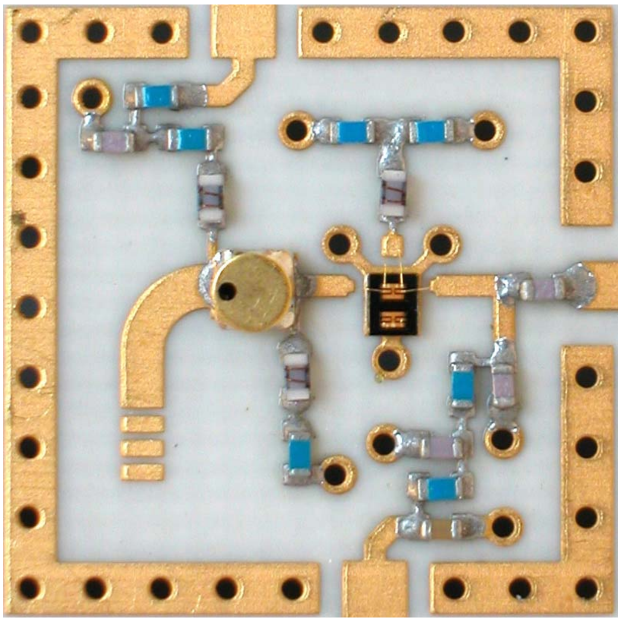

Fig. 6. Close-up photograph of the assembled VCO

After reflow, the GaN transistor is connected to the tracks using the wedge-wedge bonding technique with 25 µm diameter Gold bond-wires.

V. Measured Performance

Without any modifications, the VCO produced a stable signal with no visible spurious. When varying the tuning voltage from 0 to 20 Volts, the frequency of the oscillator tuned monotonously from 8.1 to 10.6 GHz with very low variation in output power. The measured output power over the entire frequency range varied between +18.3 and +19.3 dBm. Both curves are shown in figure 6. It can be seen that the measured frequency and output power characteristics of the VCO are fairly close to the simulated values.

The supply current was measured at 38 mA, close to the designed value of 40 mA from a +15.0 Volt supply voltage.

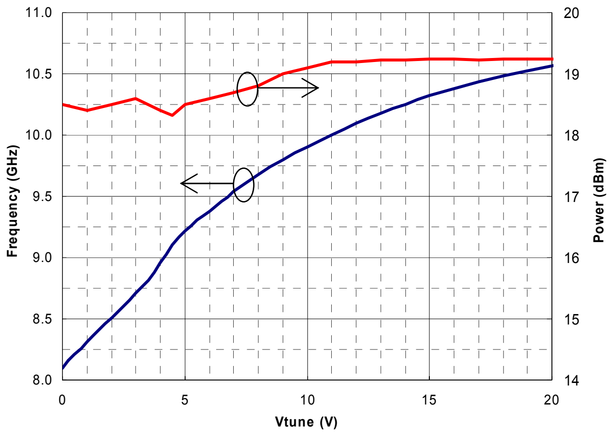

Fig. 6. measured VCO frequency and output power versus tuning voltage.

The phase-noise performance of the free-running oscillator has been measured using a HP8563E spectrum analyzer. The nominal SSB phase-noise levels @ 100 kHz and 1 MHz offset frequencies were measured at -84 and -114 dBc/Hz respectively. The phase-noise level is relatively insensitive to the oscillator frequency, as shown in figure 7.

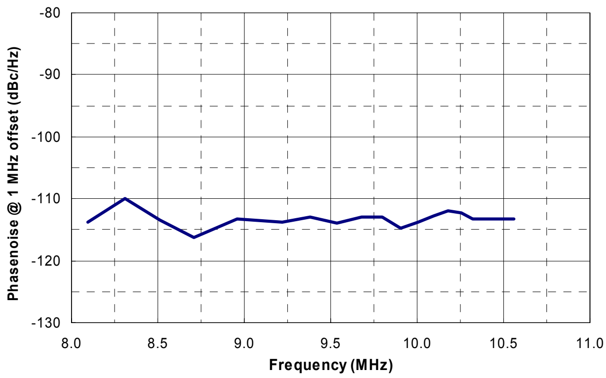

Fig. 7. measured phase-noise @ 1 MHz offset versus VCO frequency

From the phase-noise levels at different offset frequencies, it can be concluded that from 100 kHz to 1 MHz there is a 30 dB per decade slope, indicating that the 1/f-noise corner frequency of the active device is certainly higher than 1 MHz, and possibly close to the 5 MHz used to predict the phase-noise with Leeson's equation.

Lowering the supply voltage from +15 to +12 Volts resulted in a significant reduction of the phase-noise level, down to -88 dBc/Hz @ 100 kHz and -118 dBc/Hz @ 1 MHz offset. This is probably due to the less non-linear behaviour at the lowered power level of the oscillator, resulting in a lower large-signal noise-factor of the active device. At +12 Volts bias, the oscillator output power level decreases to +17 dBm.

The measured supply voltage pushing figure of the oscillator is around 20 MHz/V, a very reasonable value for an oscillator with 2500 MHz tuning range. When increasing the supply voltage up to 20 Volts, the output power level increases to +20 dBm. With an improved thermal design of the circuit, even larger output powers will be possible (with an adjusted output matching circuit), since the GaN device can, in principle, be biased at voltages of 30 Volts and higher.

In table II, the results of the designed and tested VCO are compared to existing publications on similar circuits. The combination of output power, tuning range and phase-noise at X-band frequencies of the presented design seems to be quite good.

ref	Freq. (GHz)	tuning range (MHz)	output power (dBm)	phase-noise (dBc/Hz) 100kHz	active device material / technology	active device type
[4]	8.25	900	5	-102	Si BFP420	bipolar
[6]	10	1000	15	-90	GaAs	FET
[2]	9.6	400	-	-89	SiGe	HBT
[5]	6.0	600	18-27	-92	AlGaN/GaN	HEMT
this work	**9.35**	**2500**	**17/19**	**-88/-84**	**GaN on SiC**	**HEMT**

TABLE II

VCO PERFORMANCE COMPARED TO PUBLISHED PAPERS

VI. CONCLUSION

A GaN-based low-noise X-band VCO has been succesfully designed and realized. The measured performance shows the potential for this new technology. The phase-noise results compare well with equivalent circuits published using GaAs and other technologies. The output power of +19 dBm exceeds by far the output power realisable with GaAs-based oscillators using a 2 x 50 µm size transistor.

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