A REVIEW OF FLIP-CHIP GaAs CIRCUITS, MODELS, INTERCONNECTIONS AND MODELLING TECHNIQUES IN USE AT MARCONI

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ABSTRACT

Broadband high frequency systems are increasingly utilising MMIC technology to reduce circuit design uncertainties. At frequencies above 6 GHz the MMIC interconnections become critical, bond wire inductances become significant and bond length variations in the assembly process cause significant performance variation. At Marconi Electronic Systems the benefits of solder bump connections to the MMIC are being explored. These benefits include very low inductance, self-alignment and repeatable connections. The technology is also extremely well suited to automatic and semi-automatic production, making multiple channel systems such as phased arrays more cost-effective. This paper is a review of recent work (2-40 GHz) on solder bumped MMIC circuits and covers broadband flip-chip S-parameter circuit interconnect modelling, thermal modelling of HEMT transistors connected by solder bump arrays. Additional layers to the MMT H40 Foundry process have been specially designed to facilitate solder bump connection.

I. INTRODUCTION

Flip-chip bonding can be defined as "a method of providing simultaneous electrical connection and physical attachment between a component and substrate". The connection is provided by an array of small pillars of metal, either compression bonded or soldered in place. It is attractive for low cost, volume manufacturing because it is an inherently high yielding, wafer-scale, process. Further advantages include self-alignment of component and substrate, with the interconnection being small in area and package-less. The solder bumps also provide a low and repeatable inductance with small parasitic capacitances compared with typical bond wires. This characteristic is particularly important for high frequency circuits such as 40 GHz point-to-point microwave links, phased array radar modules, and 70 GHz automotive radar.

Marconi Electronic Systems (MES) have recognised that solder bump interconnection is one of the enabling technologies necessary to realise a low-cost method of manufacturing highly integrated microwave modules. In fact, work has been carried out at Marconi Materials Technology (MMT) Caswell on the use of GaAs MMICs in a flip-chip environment since as early as 1989 when the capability of performance improvement was demonstrated [1,2]. Today MES, through services provided by MMT, now has access to state-of-the-art flip-chip technologies which include:

- A wafer scale fine detail high precision flip-chip process on both Silicon and GaAs.
- Individual 'known good die' solder bumping process for low volume applications and development work.
- Solder bump electroplating on alumina MIC carrier substrates.

Currently a 3 year applied research Pathfinder partnership between Marconi Electronic Systems and the Defence Evaluation Research Agency (DERA) Malvern is using the above technologies to characterise high frequency connection methods to MMICs as well as investigate automated and semi-automated assembly methods. Three types of MMIC solder bump connection are being investigated, flip-chip microstrip and coplanar circuits, and an RF-through-via approach requiring the definition of a pattern on the MMIC back face ground plane for RF and DC connections [Figure 1]. The possible advantages of RF-through-via connection are better grounding and heat sinking, solder is kept away from the delicate transistor circuitry, and existing foundry models apply.

The programme of work involves extensive 3D electromagnetic modelling, thermal modelling, a reliability study, and the design and manufacture of characterisation and circuit wafers, all of which are described briefly in this review.

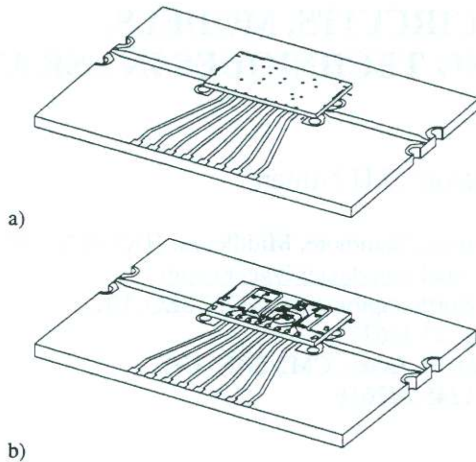

FIGURE 1 : SCHEMATIC SHOWING : a) A CONVENTIONAL FLIP-CHIP, AND b) AN RF-THROUGH-VIA MOUNTED MMIC

Other MES companies making use of flip-chip technologies include Marconi Electro-Optic Systems for IR detectors and EEV for some microwave devices.

II. ENABLING TECHNOLOGIES

MES has various technologies available depending on the application. For transitional development work the ability to solder bump individual 'known good die' MMICs is extremely important. This means initial investigations can take place without the expense of requiring whole wafers to be solder bumped. This technique has been further developed to flip-chip mount a 0.4 mm x 0.4 mm photodetector PIN diode onto a specially designed MMIC 2-18 GHz Travelling Wave Amplifier (TWA) [Figure 2] resulting in halving the responsivity ripple compared to its conventional wire bonded predecessor. A recent development has been the flip-chip mounting of a Horizontal Access Diode (HAD) onto an ultra broadband 4-40 GHz TWA.

For a more production orientated technique MES specialises in fine-feature on wafer flip-chip processing. The metal interconnects are electroplated through apetures in a developed-out layer of photoresist. Wafers up to 6 inch diameter can be processed with a minimum feature size of 9µm diameter at 5µm spacing. Two variants of the flip-chip process are practiced by MES; compression bump bonding and solder bonding. Compression bump bonding exploits pillars of either pure indium or pure gold, and uses a thermal/pressure cycle to effect a solid state diffusion bond. This form of flip-chip bonding is used by Marconi in the assembly of some of its non-optical imaging products [3]. Solder bump bonding processes use either the lead/tin solder or, more recently developed for fluxless attach, 80:20 gold/tin (%wt) eutectic solder. Solder bumps can be applied to either the wafer or the substrate as a two-layer deposit of tin over gold. The electroplate needs to be fused to form the eutectic alloy and this is achieved by providing a short thermal excursion.

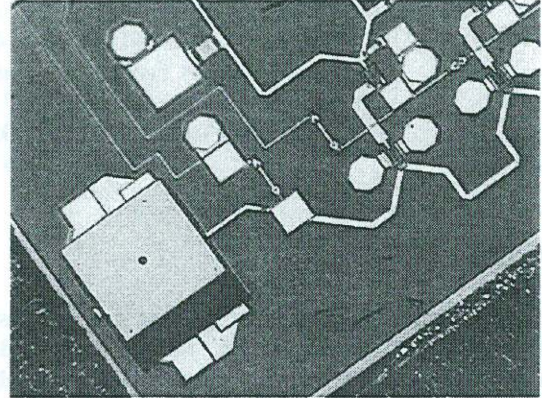

FIGURE 2 : A HYBRID OPTICAL RECEIVER

Figure 3 shows an RF multi-chip module. This relatively advanced product exploits two MMICs and some silicon integrated circuits mounted on a multi-layer silicon "circuit board". The MMICs are attached and interconnected by flip-chip bonding to provide the combination of low assembly cost, while maximising RF performance. The silicon devices use traditional aluminium wire bonds for their interconnects. Around the periphery of the silicon substrate is an array of large solder balls. These permit the entire assembly to itself be flip-chip mounted directly onto a printed circuit board (Direct Module Attach - DMA), resulting in a highly miniaturised and low profile product.

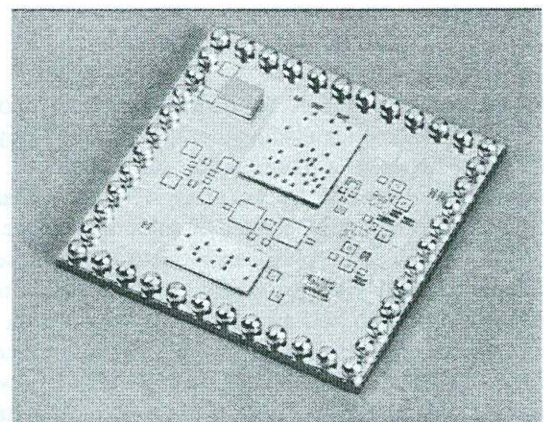

FIGURE 3 : MCM-D HIPERLAN ASSEMBLY WITH FLIP-CHIP BONDED GaAs MMICs IN A DMA PACKAGE.[PICTURE BY KIND PERMISSION OF INTARSIA CORPORATION].

III. TECHNOLOGY DEVELOPMENT

H40 Foundry Process Modifications

For flip-chip characterisation a wafer of devices was designed on the MMT H40 Foundry process. This required the introduction of additional layers specifically to aid die to substrate solder attachment [TABLE 1]. Layers were specified for both flip-chip and RF-through-via attachment methods, the latter requiring the development of a back face patterning process. For the first time a new CFC-free via etch process (developed at MMT) was used giving 25% smaller diameter vias, with the same inductance as the current process.

LAYER	DESCRIPTION
	FLIP-CHIP
18	Front Face Seal - 1000Å Titanium to provide non wettable region on front face bond pad.
19	Front Face Wet - evaporated 0.5μm TiPtAu wettable contact to define area to which the solder will adhere.
20	Front Face Solder- Optional solder layer, for solder bumps on MMIC.
	RFTV
26	Back Face Pattern - Defines back face metallisation.
27	Back Face Seal - 1000Å Titanium to provide non wettable region on front face bond pad.
28	Back Face Wet - 0.2μm TiAu wettable contact to define area to which the solder will adhere.
30	Back Face Solder- Optional solder layer, for solder bumps on MMIC.

TABLE 1 : ADDITIONAL MASK LAYERS TO THE MMT H40 FOUNDRY PROCESS FOR FLIP-CHIP AND RF-THROUGH-VIA ATTACHMENT.

Figure 4 shows the front and back face of a MMIC designed specifically for RF-through-via attachment. This particular MMIC is a double balanced K-Band Mixer with integrated back face baluns – the dark regions are where the MMIC ground plane has been selectively etched to form the baluns, the light spots are solder connection positions). Results from the characterisation wafer were unavailable at the time of going to press.

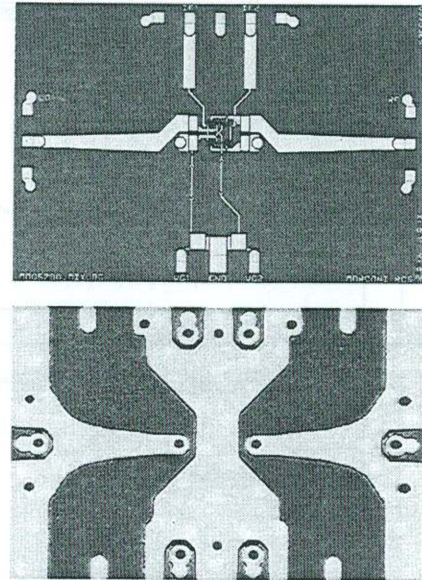

FIGURE 4 : RF-THROUGH-VIA DOUBLE BALANCED K-BAND MIXER MMIC WITH TAPERED BROADSIDE COUPLED BALUNS.

Thermal Modelling

The use of flip-chip bonding raises a number of thermal issues. Two of the most important thermal problems have been analysed using a finite difference method with a non-uniform mesh. The first compared the temperature rise in a linear array of gates, representing a large power amplifier, for different substrate mounting techniques in order to assess the effectiveness of heat sinking. The mounting arrangements were full area solder bonding, a back surface solder bond array and a flip-chip solder bonded wafer [Figure 5]. The main conclusions were as follows:

1. The use of an array of solder balls on the back face of a conventional power MMIC is very nearly as effective as the use of a continuous solder layer, with the reduced area of contact compensated by the thinner, better controlled solder balls. In practice the use of a continuous preform solder layer can lead to voids, particularly beneath vias, which gives a significantly reduced thermal conductance.

2. Conventional flip-chip attachment gives a significantly increased thermal impedance, larger by a factor of at least 40% even when the effect of the front face metallisation is taken into account. This is a consequence of the smaller area of contact between the GaAs and the heatsink.

The second problem concerned the temperature profile in a specified circuit (the MMT P35-5104 TWA), with a total dissipation of 360mW. The calculation gave a predicted maximum temperature of 40°C for a base temperature of 20°C, with little variation between the active devices. This was higher than the 26°C calculated for a continuous solder layer. Average MMIC temperature rises were calculated as approximately 4°C for the whole volume and 5°C in the central area encompassing all heat sources, from which the strain on the solder balls can be estimated and used to identify any potential reliability problems. As a result of the temperature difference between GaAs and the alumina substrate shear strains are generated in the solder bonds of up to 0.1%. This information is being used as an input to the prediction of reliability.

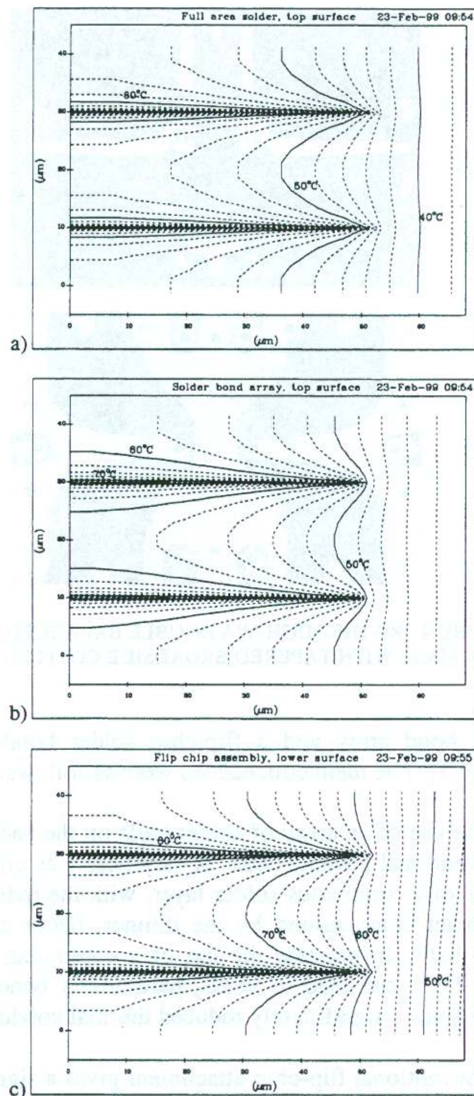

FIGURE 5 : MODELLED TEMPERATURE CONTROL PLOTS FOR A HEMT GATE ARRAY WITH a) A CONTINUOUS SOLDER LAYER ON THE BACK FACE, b) AN ARRAY OF SOLDER BONDS ON THE BACK FACE, AND c) FLIP-CHIP MOUNTED.

Interconnect Modelling

At relatively low frequencies flip-chip assemblies incorporate solder bonds which are quite small with respect to wavelength. This allows them to be safely considered from a lump-circuit equivalent point of view in which inductance terms often dominate. However as operation stretches up into the millimetre wave region this approach cannot be wholly relied upon. Detailed geometric profiles of the solder bonds, and carrier substrate and chip grounding vias becomes significant. Radiation effects as the field confinement in the substrates fall, leads to greater parasitic coupling and other interactions such as surface waves and trapped resonances.

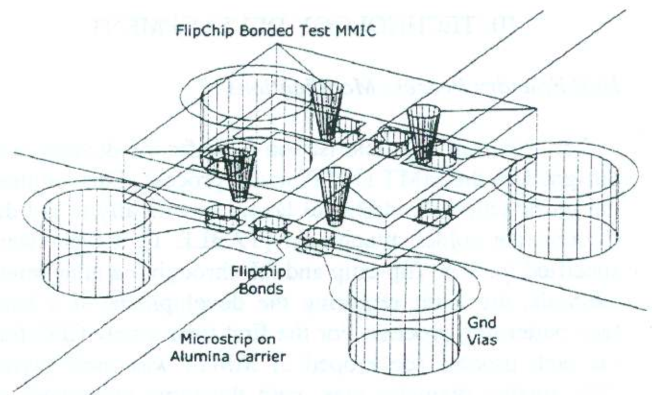

FIGURE 6 : FLIP-CHIP GEOMETRY MODEL FROM 3D EM SIMULATOR.

Development of flip-chip techniques can be greatly assisted if precise modelling can provide results which complement practical assessments using test structures on MMICs. Once confidence is established that models closely agree with test results a number of avenues open up. Measurements alone normally give s-parameters which can be insufficient for a full insight for flip-chip bond behaviour. Models based on 3D numeric tools can additionally provide electromagnetic field information at any point within the structure which can highlight coupling, radiation and resonance mechanisms. Once set up they also provide a quick way of exploring extra geometry variables or frequencies whilst avoiding the potential waste of a length and expensive wafer fabrication cycle.

Within the programme at Marconi Electronic Systems a wide variety of active and passive test MMICs are being assessed. However as EM modelling tools are principally suited to passive devices, the modelling task has focussed on a number of relatively simple MMICs which essentially incorporate through lines. This allows for easier interpretation of results and a shorter route to directly de-embed the bond junction characteristics.

Although the MMICs and the alumina carrier substrates are largely planar objects, they do incorporate three-dimensional features, and non-uniform currents in the vias and bonds. Only a true 3D electromagnetic solver can model such effects. At Marconi Research Centre (MRC) a commercial finite element package has been used. Direct transfer of mask geometry using the 2D DXF format by email gave accurate templates on to which model geometry can be snapped. The microstrip carrier substrates, and MMICs are created as independent submodels resulting in a library which enables combinations to be brought together quickly with, for example, variations in solder bump height. This has been performed for both classical microstrip flip-chips and the

alternative RF-through-via scheme. A close-up of a flip-chip geometry model is shown in Figure 6 where details such as tapered profiles in the MMIC grounding vias are evident.

The initial modelling phase concentrated on careful model verification in wideband sweeps up to 20 GHz where predictions can be fairly easily compared with test results, and close correlation has been obtained. One early observation is that much of the detail in the models coincide with the presence of the primary fields and currents leading to self-seeding as the finite-element mesh is adaptively refined. This factor assists convergence and accuracy. At the time of writing this work has been extended up in to the 30 and 40 GHz ranges where radiation issues start to occur, and require attention to model boundary conditions. It is believed that geometry for higher frequency MMIC processes where bond sizes and finer MMIC features are incorporated will allow further scaling and expansion of model capability up to 50 GHz. At the same time effort is also being directed at producing reliable circuit simulation models for such bonds so that in future they can be quickly and directly accounted for in the MMIC design process.

Amongst our preliminary conclusions is that the trapped field energy between MMIC and the carrier substrate along with the lengthy inductances associated with the grounding vias, points to potential benefits in the alternative RF-through-via approach

IV. CONCLUSIONS

Major benefits of the use of solder bump interconnections for high frequency microwave systems have been identified at Marconi Electronic Systems. It is anticipated that such interconnections will be the enabling technology for low-cost, highly-integrated multi-channel microwave modules over the next 5 to 10 years.

A programme of work, part sponsored by DERA under the Pathfinder scheme, has begun to characterise various high frequency GaAs MMIC connection methods by thermal modelling, and a combination of extensive 3D electromagnetic modelling and specially designed test devices using a modified MMT Caswell H40 Foundry process.

V. ACKNOWLEDGEMENTS

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VI. REFERENCES

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