Scaleable Coplanar Waveguide Transmission Lines and Discontinuities on Gallium Arsenide MMIC Substrates

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***Abstract* - New scaleable circuit models for Coplanar Waveguide transmission lines and discontinuities have been developed for the Philips GaAs MMIC foundry processes. The models were developed from extensive simulation of Coplanar circuits using Sonnet™, a 2.5D electromagnetic simulator. The simulation results were validated up to 80 GHz using measurements of passive structures from the Philips ED02AH process.**

I. INTRODUCTION

Coplanar Waveguide (CPW) [1] as a transmission medium for Microwave Monolithic Integrated Circuits (MMIC) fabrication has a number of advantages over the more traditional microstrip circuits[2]. CPW requires no backside processing of the wafer, leading to less expense and faster processing of the wafer. CPW structures tend to be more compact and also lend themselves more easily to recent developments in mm-wave packaging, such as Flip-Chip[3]. Hence there is a need for CPW passive models characterised to mm-wave frequencies. To date most foundry guides contain models only for microstrip transmission lines and associated discontinuities, or limited CPW lines and discontinuities which have fixed width and spacing.

This paper describes a scaleable CPW transmission line model which accounts for the multilayered structure of the GaAs MMIC. Thus permitting the user to vary the characteristic impedance of the transmission line, rather than having to use the predefined impedances set by the foundry guides. Therefore techniques such as quarter-wave transformer matching may be implemented in the MMIC design.

Further scaleable models including CPW right-angle bends, ground interconnects, which are used for suppression of slot line modes, and tapered CPW transmission lines are also outlined. All of the models are implemented in HP-MDS circuit simulator.

II. GAAS MMIC TRANSMISSION LINE MODEL

Models are normally based upon measured results, however for passive structures on multilayer substrates electromagnetic simulation carefully validated offers advantages over models based upon measurement alone. Simulation permits many variants of the structures to be addressed with associated lower cost as less MMIC fabrication is required.

The basic layer structure of the Philips GaAs MMIC is shown in Figure 1. The metallisation layer most commonly used in the Philips process lies on a silicon dioxide and silicon nitride layer, a second silicon nitride layer encapsulates the circuit, therefore a uniform dielectric constant of 12.9 cannot be assumed.

The CPW transmission line MDS circuit model was compared to the results achieved through simulation and the dielectric constant adjusted accordingly. It was found that dielectric constant varied with the width and spacing of the CPW line, as shown in Figure 2, and could be represented by equation 1. A limit of the model is also specified due to leakage of the fields outside the GaAs substrate beyond this point. Equation 1 holds for different substrate heights, simulated up to 620 μm, as long as this limit is obeyed.

$$\varepsilon_r = \left(5.4 s^{0.17}\right) \cdot \left(w^{0.15 s^{-0.41}}\right) \qquad (1)$$

limit $w + 2s \leq \frac{h}{2}$ $\quad h \leq 620\ \mu m$

$w \leq 160\ \mu m$

$s \leq 80\ \mu m$

where w = width of centre conductor (μm)
s = spacing to ground planes (μm)
h = height of substrate (μm)

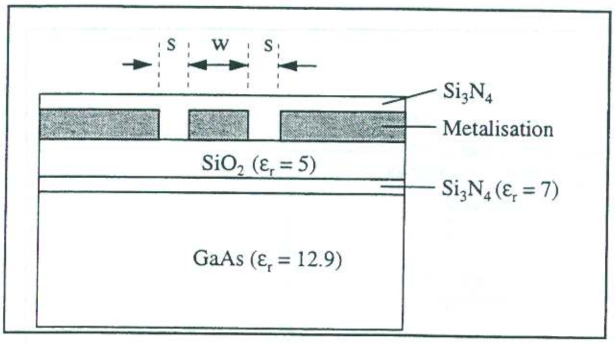


Fig.1 LAYER STRUCTURE OF PHILIPS GAAS MMIC

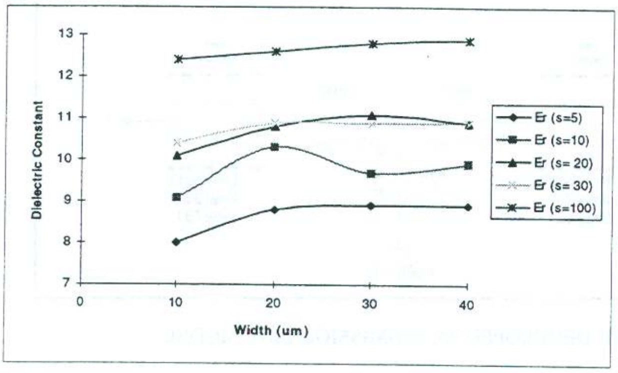


Fig.2 DIELECTRIC CONSTANT OF CPW TRANSMISSION LINE AS WIDTH AND SPACING IS VARIED

III. GAAS MMIC CPW DISCONTINUITIES

A. Ground Interconnects

To suppress the slot line mode occurring in the CPW, the ground planes are interconnected by a layer which passes underneath the signal line [4], this method was chosen rather than air-bridges due to criteria set in the Philips foundry process. A 3-D view of the ground interconnect method used is shown in Figure 3. This discontinuity can be represented by a capacitance to ground between transmission line sections. This capacitance is again dependent on the width and spacing of the CPW lines and may be represented by equation 2. As the Philips processes also permit air bridges, for smaller dimensions, the capacitance for ground interconnects can be reduced by the signal line passing above an air pocket where the ground interconnect occurs. The capacitance for this type of interconnect is given in equation 3. The width of the ground interconnect was kept fixed at 5 μm.

$$Capacitance = 0.36w + 0.05s \qquad (fF) \qquad (2)$$

$$Capacitance = 0.15w + 0.05s \qquad (fF) \qquad (3)$$

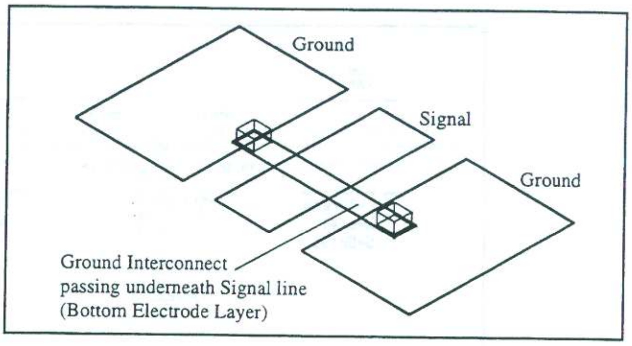


Fig. 3 A 3-D VIEW OF THE GROUND INTERCONNECT METHOD

B. Right-Angle Bends

The circuit model for the CPW right-angle bend is shown in figure 4 . The model is developed from simulations which were de-embedded to the edge of the ground planes. Therefore the length of the transmission lines are a function of width and spacing, as given in equation 4. It was found that the inductance could be represented by equation 5, while the capacitance remains constant.

$$Length = \frac{w}{2} + s \qquad (\mu m) \qquad (4)$$

$$Inductance = -6.9e^{(0.035s+0.35)\cdot\sqrt{\frac{w}{w+2s}}} \quad (pH) \qquad (5)$$

The simulation results show that the length of the line is actually reduced when using a CPW right-angle bend, hence the requirement for a negative inductance in the circuit model. This behaviour has also been observed for the Microstrip right-angle bends in the Philips GaAs MMIC process.

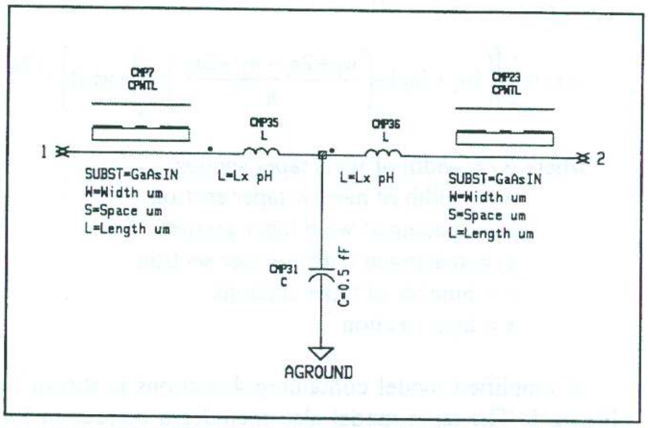


Fig. 4 CIRCUIT MODEL FOR CPW RIGHT ANGLE BEND UTILISING MDS CPW TRANSMISSION LINE MODEL

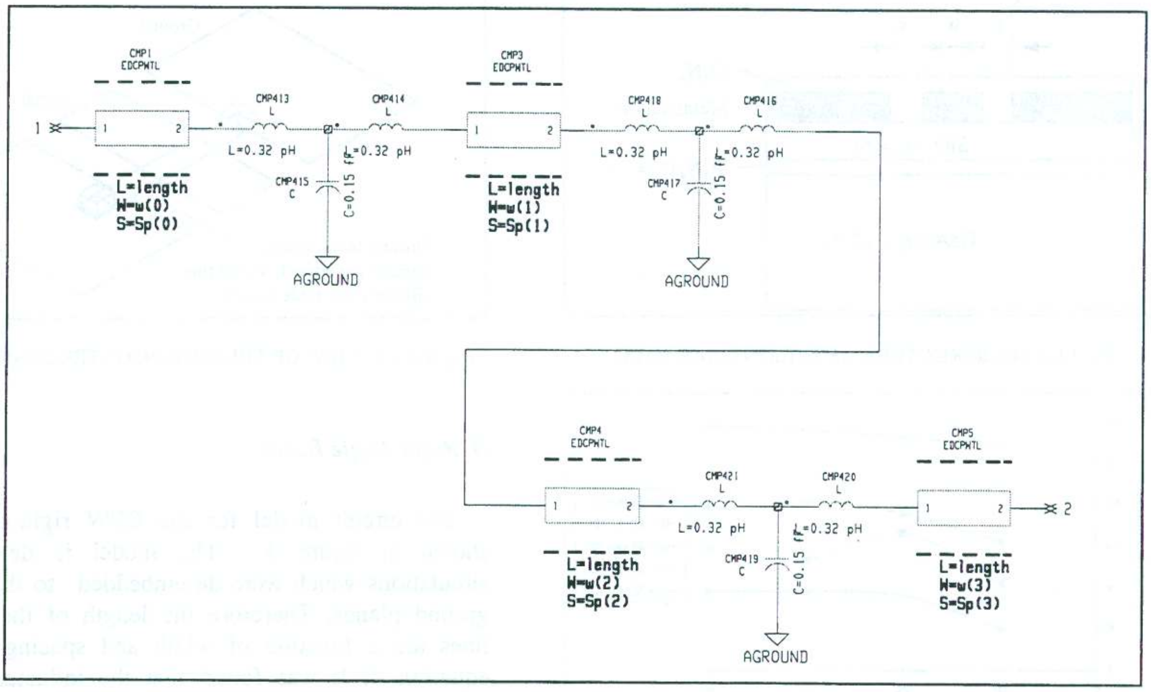


Fig 5. FOUR SECTION CPW TAPER MODEL WITH DEVELOPED TRANSMISSION LINE MODEL

C. Tapers

The taper model is constructed from a number of CPW transmission line models, described in section II, in which the width and spacing are varied in each section until the desired width and spacing is achieved. The equations to determine width and spacing for the intermediate sections are given in equations 6 and 7 respectively.

$$w(x) = w_1 - \frac{(w_1 - w_2)}{n} \cdot x \qquad (6)$$

$$s(x) = \frac{1}{2}\left\{\left((w_1 + 2s_1) - \left(\frac{w_1 + 2s_1 - w_2 + 2s_2}{n}\right) \cdot x\right) - w(x)\right\} \qquad (7)$$

where w_1 = width of wide taper section
w_2 = width of narrow taper section
s_1 = spacing at wide taper section
s_2 = spacing at narrow taper section
n = number of taper sections
x = taper section

A simplified model containing 4 sections is shown in Figure 5. The taper model also includes a correction for the small step in line width and spacing between each section. The values of the inductances and capacitances were determined by calculating the total discrepancies between the circuit model without correction and the EM simulation results for a relatively long taper. The total values of inductance and capacitance calculated were then distributed along the circuit model.

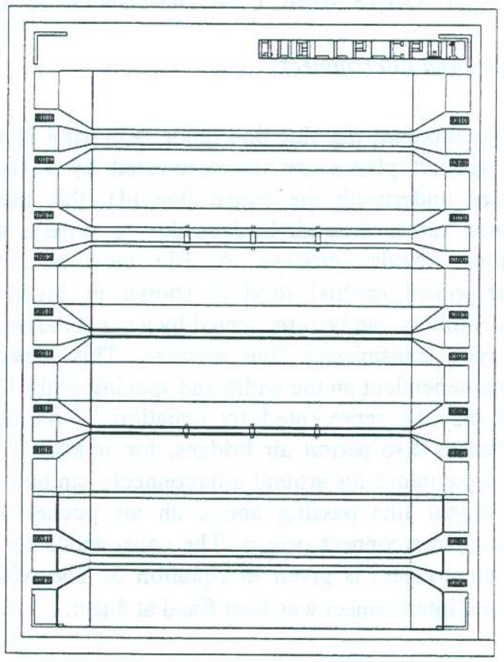


Fig. 6 FABRICATED CPW TRANSMISSION LINES STRUCTURES ON GAAS MMIC

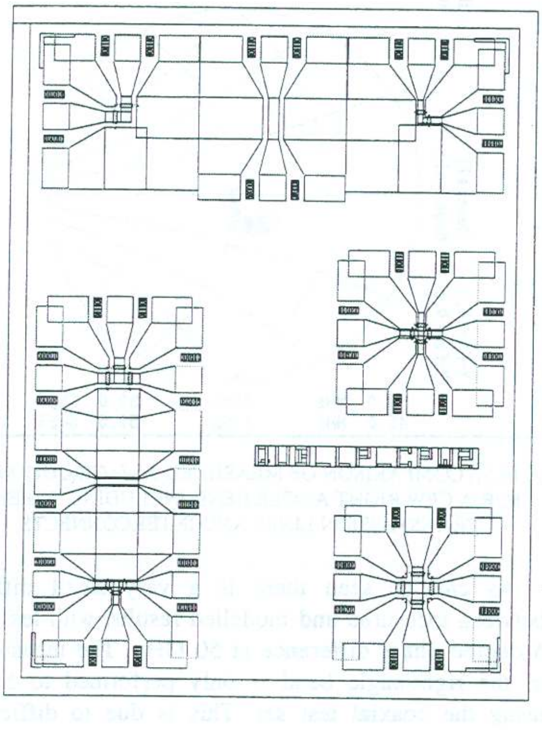


Fig. 7 FABRICATED CPW DISCONTINUITIES ON GAAS MMIC PROCESS

IV. MEASURED RESULTS

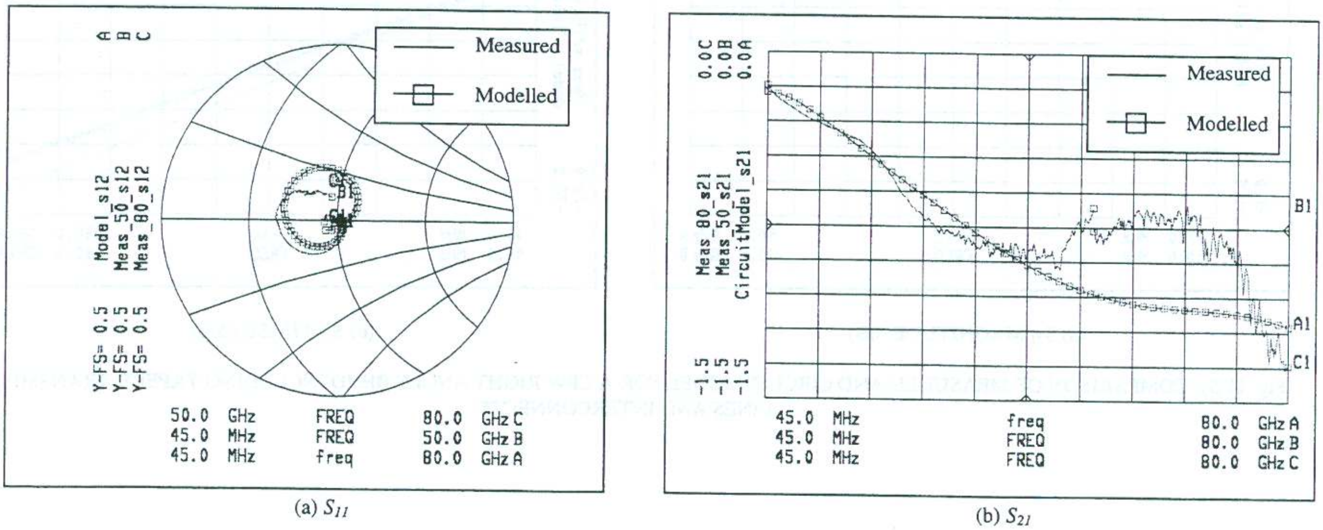
The GaAs MMIC structures used to validate the EM simulations and assess the circuit models are shown in figures 6 and 7 respectively. Both were fabricated using the Philips ED02AH.

The measurements were performed On-Wafer using an HP8510C Vector Network Analyser. The system was calibrated using an On-Wafer Load Reflect Match (LRM) calibration.

A comparison of measured and circuit simulator for some of the CPW transmission lines are shown in figure 8. A discrepancy is shown in the measured results at 50 GHz, which can be attributed to the transition between the coaxial and waveguide test sets. The V-band waveguide measurements are also much noisier than the coaxial measurements.

Above 45 GHz some differences appear between the measured and modelled results. This has been attributed to the restricted height of the substrate used (100 μm) being compatible with the Philips microstrip process. At these high frequencies there is some 'leakage' of the electromagnetic fields out of the GaAs substrate. To limit this effect the MMIC's were measured while mounted on a 620 μm Alumina substrate. However this does not solve the problem completely due to differences in the dielectric constants and material properties of the two substrates.

A comparison of the measured results with the circuit model prediction for the w = 30μm, s = 15μm CPW transmission line is shown in figure 9. The effect of electromagnetic field leakage into the alumina substrate, as expected, is more pronounced using this wider CPW transmission line.



(a) S_{11}

(b) S_{21}

Fig. 8 COMPARISON OF MEASURED AND CIRCUIT MODEL FOR A CPW TRANSMISSION LINE WITH AIRBRIDGE INTERCONNECT MOUNTED ON AN ALUMINA SUBSTRATE
(w = 16 μm, s = 5 μm)

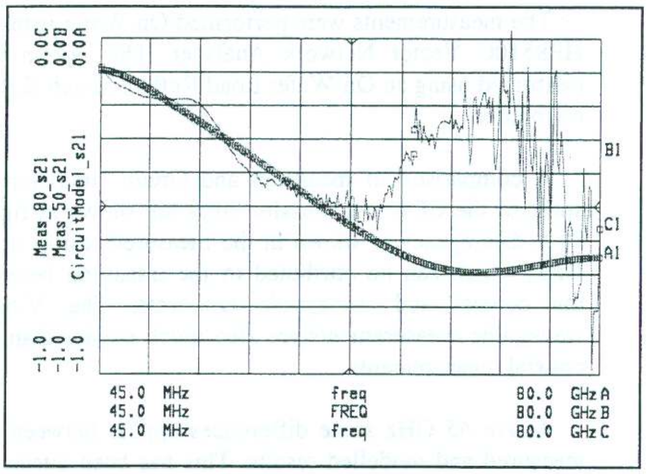


Fig. 9 COMPARISON OF MEASURED AND CIRCUIT MODEL FOR A w = 30 µm, s = 15 µm CPW TRANSMISSION LINE INCLUDING AIRBRIDGE INTERCONNECT

A comparison between the circuit model and measured results for the CPW right-angle bend is shown in figure 10 and 11. The complete MDS circuit model of the measured right-angle bend including tapers, transmission lines and airbridge interconnects being shown in figure 12.

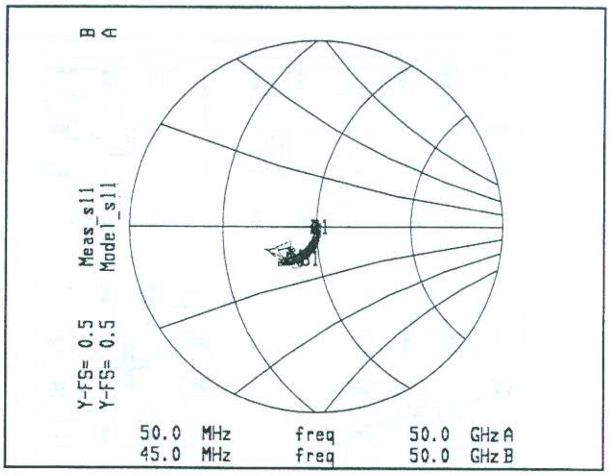
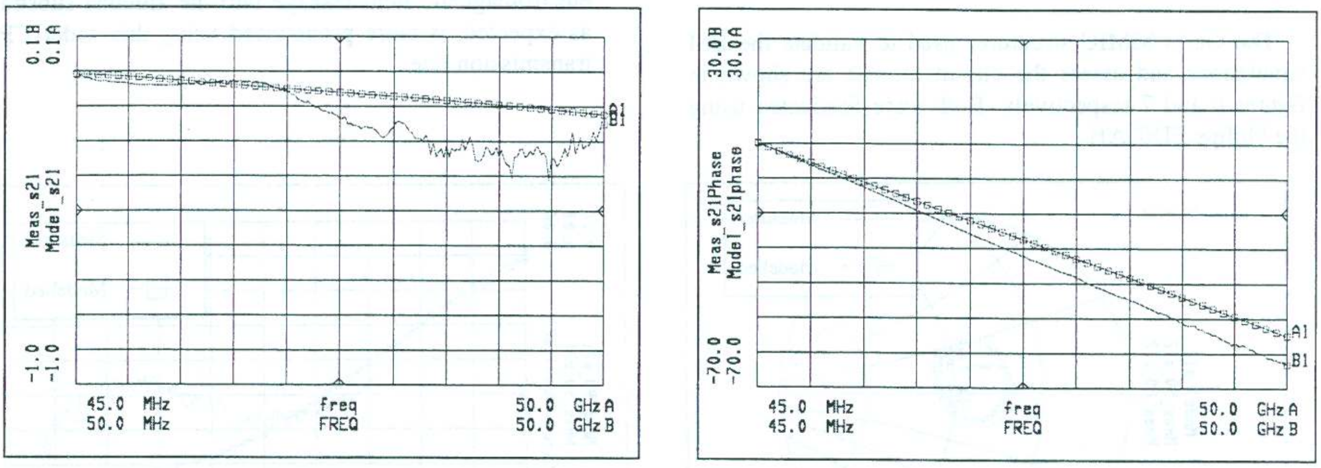


Fig. 10 S_{11} COMPARISON OF MEASURED AND CIRCUIT MODEL FOR A CPW RIGHT ANGLE BEND INCLUDING TAPERS, TRANSMISSION LINES AND INTERCONNECTS

As can be seen there is a very small difference between measured and modelled results, with less than a 5 degree phase difference at 50 GHz. The measurement of the right-angle bend is only performed to 50 GHz using the coaxial test set. This is due to difficulty in orientating the V-band waveguide probes in the North-East position required for measurement.



(a) S_{21} MAGNITUDE (dB)

(b) S_{21} PHASE (deg)

Fig. 11 S_{21} COMPARISON OF MEASURED AND CIRCUIT MODEL FOR A CPW RIGHT ANGLE BEND INCLUDING TAPERS, TRANSMISSION LINES AND INTERCONNECTS

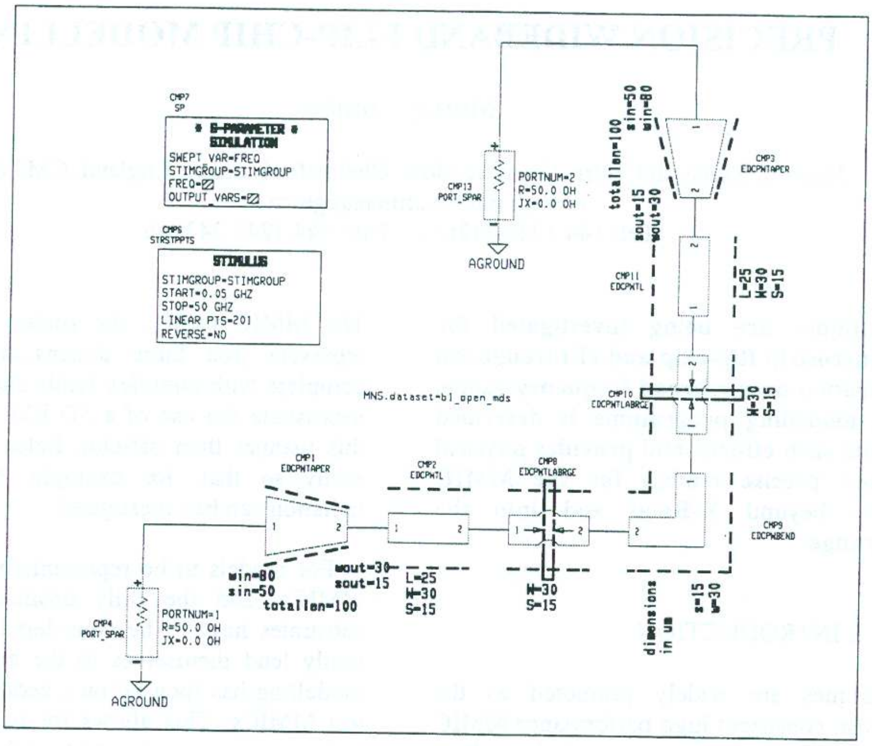


Fig. 12 CIRCUIT MODEL SCHEMATIC FOR MEASURED CPW RIGHT ANGLE BEND

V.CONCLUSIONS

A new scaleable CPW passive circuit model library which accounts for the multilayer structure of the GaAs MMIC has been developed through extensive electromagnetic simulation. Thus permitting fast and accurate design of CPW GaAs MMIC circuits. The models have been verified through measurement of lines and discontinuities on the Philips ED02AH process. The small discrepancies between measurement and the circuit models have also been accounted for.

VI. ACKNOWLEDGEMENTS

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