Scaling of GaInP/GaAs HBT Equivalent-Circuit Elements

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Abstract — **In this paper, GaInP/GaAs HBT's equivalent-circuit elements are investigated with respect to their dependence on layout geometry. A large number of extracted parameters for HBT's of different layouts is given, as well as simple formulas, relating the element values with properties of the layout. The results are useful for large-signal modeling and layout optimization.**

I. INTRODUCTION

Heterojunction bipolar transistors (HBT's) are well suited devices for circuits in modern wireless systems. They are used in high linearity RF amplifiers in digital communication systems due to their capability to operate at high current densities and their high linearity. Another important parameter of an amplifier is its noise behaviour. This is related to noise parameters and gain of the transisitor and is excellent for HBT's, too. Another advantage of an HBT is, that it only needs one supply voltage. This simplifies circuit design.

Optimization of the fabrication process must include the vertical semiconductor layer structure and the lateral layout as well. The required information can be obtained from a systematic investigation of the small-signal equivalent-circuit of devices with several physical layouts.

In this investigation, we present scaling laws for the small signal equivalent circuit elements for HBT's with different layouts, i.e. a different number of emitter fingers and various emitter areas.

The results can be used for optimizing the transistor layout for different applications:

- A high value of the maximum frequency of oscillation $f_{\max}$ can be obtained by minimizing the total base-collector capacitance $(C_{bc}+C_{ex})$ and the total base resistance (R_b+R_{b2}).
- The noise parameters are optimum with R_b+R_{b2} and the the emitter resistance R_e as small as possible [1].
- A small value of the parasitic capacitance between collector and emitter is favorable for output matching of a power transistor.
- A scaleable large-signal transistor model developed for a certain transistor layout can be transferred to another one with a different layout [2, 3].
- The scaling laws for several equivalent circuit elements can be used for process monitoring, even if different transistor are compared, not only a special monitor device [4].

To obtain the scaling laws of the small-signal parameters, various HBT's with different layouts are considered, and detailed scaling functions for the different elements are given.

II. MODEL PARAMETER EXTRACTION

The different layouts under consideration are single-emitter HBT's with emitter sizes of $3\times15\mu\text{m}^2$, $3\times30\mu\text{m}^2$, $3\times60\mu\text{m}^2$, $4\times30\mu\text{m}^2$, and $6\times30\mu\text{m}^2$. Also, multi emitter HBT's were investigated: $2\times(3\times30)\mu\text{m}^2$, and $10\times(3\times30)\mu\text{m}^2$.

Schematic cross section and layout of a single-emitter HBT are shown in Fig. 1, and 2, respectively. In the employed mesa process, the device isolation is obtained by etching down to the semi-insulating substrate. The schematic shows only the contact metallisation of the HBT itself. The air bridges connecting the HBT to the coplanar environment, are not shown for simplicity. Multi-emitter HBT's are designed by parallelization of these single-emitter HBT's.

S-parameters were measured on-wafer up to 40 GHz in order to extract small-signal equivalent-circuit elements. The parameter extraction was done using an analytical method [5], which yields all equivalent circuit elements without numerical optimization. The equivalent circuit without reactive parasitics is shown in Fig. 1.

III. RESULTS

The intrinsic parameters are bias dependent. Values are given for different current densities J_c in the range $5\times10^3 \ldots 1\times10^5$ A/cm^2. The collector-emitter voltage V_{ce} is fixed at 3 V. For all HBT layouts, the maximum transit frequency f_t is achieved at $J_c \approx 3\times10^4$ A/cm^2 (see Fig. 8). For higher current densities, the base push-out effect occurs.

Scaling of the equivalent circuit parameters is observed to be dependent on different geometrical regions of the HBT. These regions are:

1. **The emitter area** A_E. The active part of the HBT is assumed to be a rectangular cell under the emitter (see Fig. 1). The extrinsic emitter resistance R_e and the intrinsic base-emitter and base-collector elements R_{be}, C_{be}, and R_{bc}, C_{bc} scale with A_E. Values are not given for R_{bc}, since it is too large to be extracted properly ($\gg 10\,\mathrm{k\Omega}$). Also not shown is C_{be}, since it is shunted by the small value of R_{be}.
    - Despite some scatter, the scaling law of R_e is found to be

      $$R_e \times A_E = 160\,\Omega\mu\mathrm{m}^2.$$

      See Fig. 3.
    - R_{be} yields the value expected from physics: $R_{be} = (n_e V_{th})/I_c$, with the thermal voltage $V_{th} = (kT)/q_e \approx 26\,\mathrm{mV}$ and the ideality factor of the base-emitter diode $n_e \approx 1$. The scaling law is therefore:

      $$R_{be} \times A_E = \frac{26\,\mathrm{mV}}{J_c \times 10^8}.$$

      See Fig. 5.
    - For C_{bc} it is found: $C_{bc}/A_E = 0.17\,\mathrm{fF}/\mu\mathrm{m}^2$, at $J_c = 3 \times 10^4\,\mathrm{A/cm}^2$. For $J_c \to 0$, C_{bc}/A_E reaches the value expected from physics of

      $$\begin{aligned} C_{bc}/A_E &= \sqrt{\frac{\varepsilon q N_B N_C}{2(N_B + N_C)(\phi_D + V_{cb})}} \\ &= 0.22\,\mathrm{fF}/\mu\mathrm{m}^2 \end{aligned}$$

      for the depletion capacitance with no collector current. N_B and N_C are the doping levels of base and collector, and ϕ_D is the diffusion potential of the base-collector pn-junction. C_{bc} first decreases due to the current and finally increases dramatically at higher current densities due to high collector current base push-out effect [6, 7, 8, 9, 10]. See Fig. 4.
2. **The base regions** A_B **and** A'_B. A_B is formed by the area of the base metallisation. A'_B is formed by the area of the extrinsic base mesa. The first one determines the value of the extrinsic base resistance R_b, while the latter one determines the semi-extrinsic base-collector capacitance C_{ex}.
    - The scaling law of R_b is found to be

      $$R_b \times A_B = 120\,\Omega\mu\mathrm{m}^2,$$

      similar to the behaviour of R_e.
    - The extrinsic base-collector capacitance C_{ex} describes the part of the total base-collector capacitance, that is outside the active region of the HBT. It is therefore expected to be independent of current and to have the same scaling rule as C_{bc}, at $J_c = 0$. It has been found:

      $$C_{ex}/A'_B \approx 0.2\,\mathrm{fF}/\mu\mathrm{m}^2.$$

      See Fig. 6.
3. **The region between the base contact and the active part of the HBT** determines the intrinsic base resistance R_{b2}. This element is expected to be mainly proportional to the total length of the emitter. Although the values of R_{b2} scatter about 25%, scaling is observed:

   $$R_{b2} \times 2l_e/w_{be} \approx 400 \cdots 700\,\Omega\square,$$

   with the emitter length l_e and the distance between base contact and emitter mesa w_{be}. See Fig. 7.
4. The extrinsic collector resistance R_c is determined by the layout of the collector contact and the subcollector. Thus, R_c can only approximately be correlated with layout properties. In our case, the main geometrical property is the **circumference of the active region**, given by length l_e and width w_e of the emitter. The scaling rule is:

   $$R_c \times 2(l_e + w_e) \approx 160\,\Omega\mu\mathrm{m}.$$
5. The current gain $\beta = 1/(1-\alpha)$ is virtually **independent of geometry**, which means, that recombination at base surface is negligible. It is only controlled by the vertical layer structure.

IV. CONCLUSION

The small signal equivalent circuit elements of HBT's with different layout were compared in order to determine variation of these parameters. Detailed scaling rules are given relating the small-signal equivalent circuit elements to the HBT's layout geometry. The resulting scaling functions can support the design of devices for different applications. It also can be used to develop a scaled large-signal model and to optimize the technology.

V. REFERENCES

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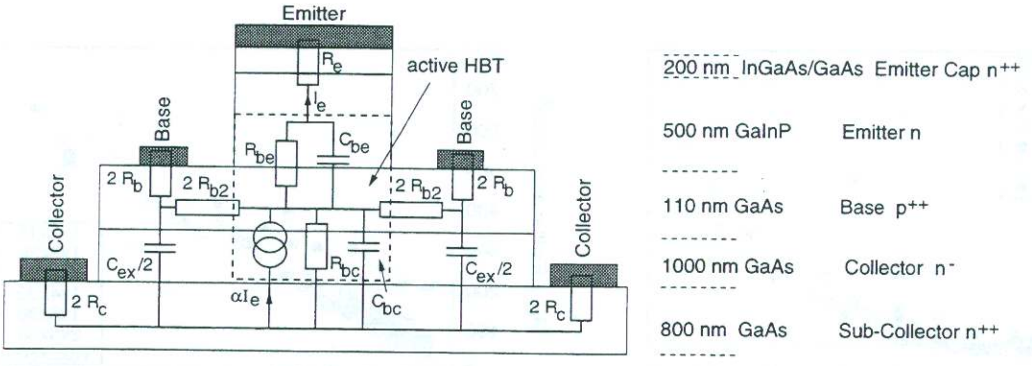

Fig. 1: Schematic cross section of HBT with small-signal equivalent-circuit.

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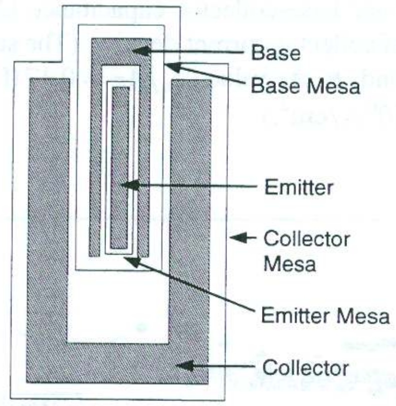

Fig. 2: Schematic top view of single emitter HBT layout. The contact metallisation is connected to the coplanar environment with air bridges (not shown). Multi-emitter cells are designed of single emitter HBT's by parallelization.

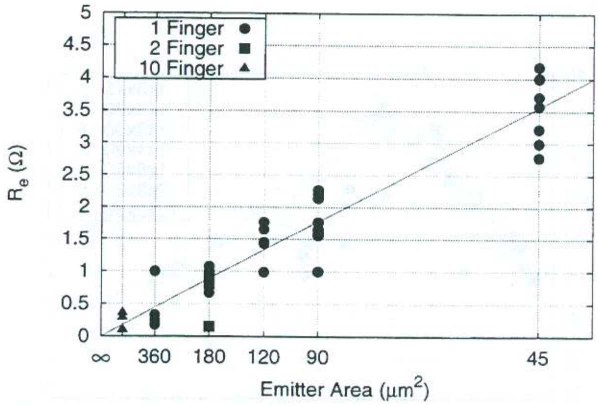

Fig. 3: Extrinsic emitter resistance R_e versus emitter area. (The straight line denotes the scaling rule given above.)

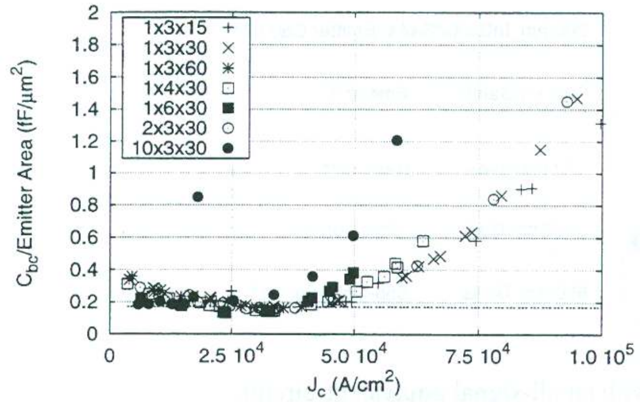

Fig. 4: Intrinsic base-collector capacitance C_{bc}/A_E as function of collector current density. (The straight line corresponds to the value $C_{bc}/A_E = 0.17\,\mathrm{fF}/\mu\mathrm{m}^2$ at $J_c = 1\times10^4\,\mathrm{A/cm}^2$.)

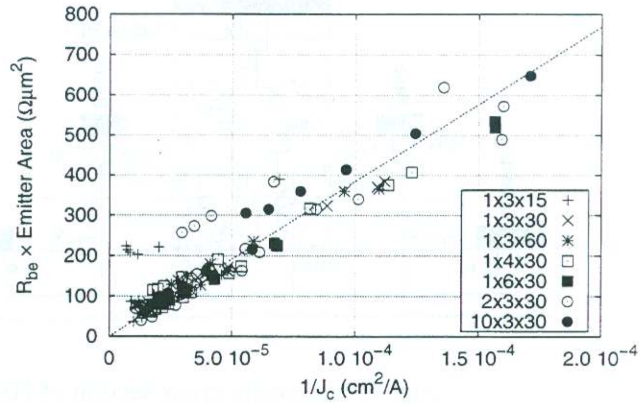

Fig. 5: Intrinsic base-emitter resistance $R_{be}\times A_E$ as function of collector current density. (The straight line denotes the value expected from physics.)

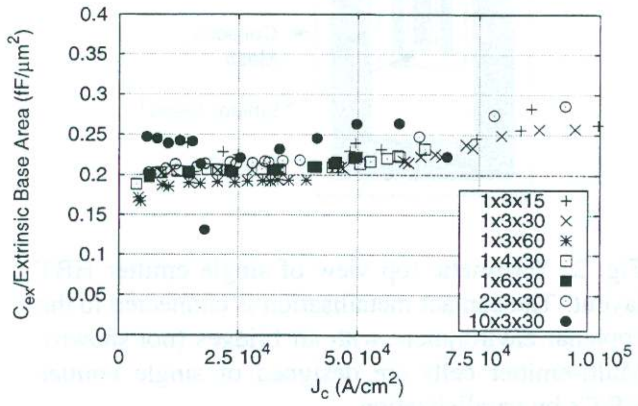

Fig. 6: Semi-extrinsic base-collector capacitances C_{ex}/A'_B as function of current density.

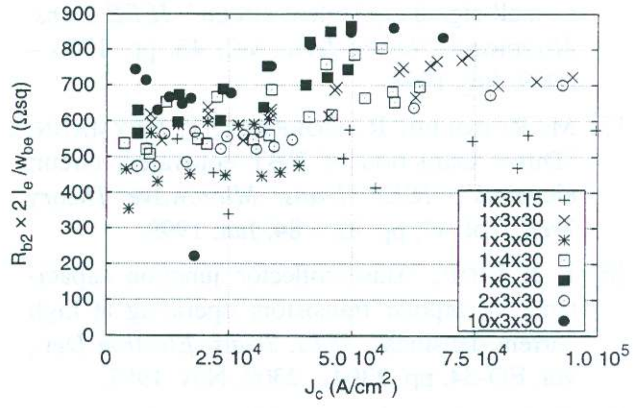

Fig. 7: Intrinsic base resistance $R_{b2}\times 2l_e/w_{be}$ as a function of current density.

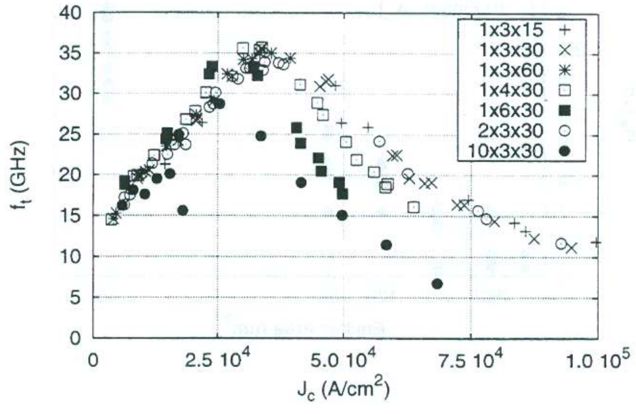

Fig. 8: Transit frequency f_t as a function of current density.