ELECTRON DEVICE MODEL BASED ON NONLINEAR DISCRETE CONVOLUTION FOR LARGE-SIGNAL CIRCUIT ANALYSIS USING COMMERCIAL CAD PACKAGES

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Abstract — **An empirical, purely mathematical electron device model is derived, without introducing any constraint on the physical device structure, under simple assumptions widely verified in practical microwave circuit design. In particular, the model is based on a new approach which greatly simplifies the implementation in commercially available CAD programmes for microwave circuit analysis, with respect to previous similar approaches [1,2]. Experimental results are presented which confirm the validity of the model.**

I. INTRODUCTION

In the last few years a number of mathematical approaches [1÷4] have been proposed for the look-up-table based nonlinear dynamic modeling of electron devices. The basic aim of these methods is that of providing accurate large-signal performance prediction directly in terms of commonly available experimental data (i.e., DC characteristics and bias dependent small-signal AC measurements), without the need for equivalent circuits and technology-dependent analytical functions to describe the nonlinear device characteristics.

The proposed empirical model, besides preserving the same kind of approach, is particularly suitable for the implementation in commercial CAD tools for the analysis of nonlinear microwave circuits. In particular, a purely mathematical functional description of the nonlinear dynamic behaviour is adopted, where the instantaneous intrinsic device currents depend on both "present" and "past" applied voltages. This kind of description can be simplified by assuming that the functional relation between currents and voltages only involves memory effects, which are short in relation with the typical operating frequencies of the device. The validity of such an hypothesis on the device behaviour has been verified by considering both accurate two-dimensional numerical device simulations and actual measurements on devices not affected by strong parasitic . The latter can be taken into account by additional linear elements as shown in Fig. 1, where also a linear parallel parasitic network has been considered. In such conditions, a finite-memory model, with a suitably chosen memory time T_M, can be adopted without introducing important approximations in the dynamic device response [2]. It is interesting to note that conventional quasi-static models are a special-case of finite memory models with $T_M \rightarrow 0$.

In Section II the Nonlinear Discrete Convolution (NDC) model is presented in the case of a single port device for simplicity. Multiport device modeling is simply obtained by vectorial re-interpretation of the single port expressions. In Section III the closed-form model identification based on static and small-signal conventional measurements is described. Section IV will be dedicated to the implementation of the NDC model into the commercial CAD package HP-MDS in the common case of two-port electron devices. Experimental results validating the model are finally presented in Section V.

II. THE NDC MODEL

The time-domain current/voltage relationship of a single port electron device can be expressed as:

$$i(t) = \lim_{T_M \rightarrow \infty} \Psi \left| v(t-\tau), V_0 \right|_{\tau=0}^{T_M} \qquad (1)$$

where $\Psi|\cdot|$ is a suitable nonlinear functional or *"line-function"*, which formally represents the nonlinear dependence of the electron device current i at the generic instant t on the present and past values of the applied voltage $v(t-\tau)$ over a virtually infinite memory time-interval T_M. The dependence of the current $i(t)$ on the DC component V_0 of the voltage has been introduced here in order to describe in a simplified way, according to the approaches proposed in [5,6], the low-frequency dispersive phenomena due to "traps". This is important in order to separate the "long lasting" memory of the charge "trapping" phenomena from the relatively "short" memory dynamics associated with all the other charge storage phenomena within the device. In fact, the main simplification which leads to our model equations derives from the basic hypothesis that, apart from low-frequency dispersion and linear parasitics which can be easily modeled separately, all the other device dynamics is limited to a memory time T_M which is

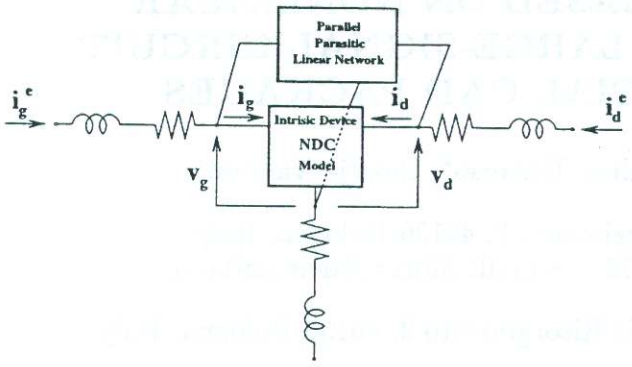


Fig. 1: Equivalent scheme for parasitic modelling in the Nonlinear Discrete Convolution Model.

not only practically finite, but also relatively short (i.e. much shorter than the period of the typical operating signals). The validity of such an hypothesis has been verified for a large family of almost intrinsic devices (i.e. devices not affected by strong parasitics, or after de-embedding from parasitics), both through accurate numerical device simulations and experimental results.

When the short memory condition is satisfied, so that a small, finite T_M can be used in eqn.(1) without introducing any relevant "memory truncation error", the device dynamics can be more conveniently described in terms of *"dynamic voltage deviations"* $e(t,\tau) \doteq v(t-\tau) - v(t)$, suitably defined as the difference between the "past" value $v(t-\tau)$ of the applied voltage with respect to the present value $v(t)$:

$$i(t) \simeq \Upsilon \left| v(t), e(t,\tau), [v(t) - V_0] \right|_{\tau=0}^{T_M} \qquad (2)$$

In the above equation the variable V_0 has been replaced by $v(t) - V_0$; this involves no loss of generality with respect to eqn.(1), since eqn.(2) also involves an explicit dependence on $v(t)$.

If the time value T_M is short enough in relation to the operating frequency of the applied voltage, the dynamic voltage deviations $e(t,\tau)$ can be considered small even in the presence of large signal conditions. Thus, the nonlinear functional dependence on $e(t,\tau)$ in eqn.(2) can be linearised and described in terms of a linear convolution with respect to $e(t,\tau)$:

$$\begin{aligned} i(t) &= F^{LF}[v(t), V_0] + \\ &+ \int_0^{T_M} g[v(t),\tau]\,(v(t-\tau) - v(t))\,d\tau \end{aligned} \qquad (3)$$

The term $F^{LF}[v(t), V_0]$ in eqn.(3) describes the device behaviour at DC and low-frequency operation by taking also into account the effects of dispersive phenomena through the additional dependence on the mean value V_0 of the applied voltage [5,6]. Moreover, the second term in eqn.(3) represents a purely-dynamic single-fold convolution integral between voltage deviations and a "pulse response function" $g[v(t),\tau]$ nonlinearly-controlled by the instantaneous applied voltage. This term accounts for purely-dynamic nonlinear phenomena which are important at high operating frequencies.

Eqn.(3) represents a finite memory nonlinear model which can correctly describe the behaviour of a given electron device provided that, for a given set of voltage signals v, suitable values of T_M can be found for which the errors due to both memory truncation and linearisation with respect to the voltage dynamic deviations are small enough, as it has been empirically verified [2].

In order to make model extraction and implementation feasible, the memory time $[0, T_M]$ of the nonlinear intrinsic device is divided into a suitable number N_D of intervals of width $\Delta\tau$. This allows for a new formulation of the model where the dynamic deviation is a function of a finite number of points in the τ-domain, while the voltage-controlled dynamic pulse response is expressed by means of a p index which "discretises" the convolution integral by a finite summation:

$$\begin{aligned} i^e(t) &= F^{LF}[v(t), V_0] + \\ &+ \sum_{p=1}^{N_D} g_p[v(t)][v(t-p\Delta\tau) - v(t)] + \Delta i_{par}(t) \end{aligned} \qquad (4)$$

In this expression an additional current contribution $\Delta i_{par}(t)$ has also been included in order to account for the possible presence of a parallel parasitic linear network, as shown in Fig. 1 for the two-port case. The parasitic term in eqn.(4) can be explicited in the following form:

$$\Delta i_{par}(t) = \sum_{p=N_D+1}^{N_{DL}} \Delta y_p[v(t-p\Delta\tau) - v(t)] \qquad (5)$$

In fact, it is reasonable to assume that not only the active intrinsic device but also the parasitic linear network can be described in the time domain in terms of the intrinsic voltage through a convolution integral over the finite time T_{ML}. The terms Δy_p are the $(N_{DL} - N_D)$ pulse response samples of the parasitic network corresponding to each elementary time interval of its memory T_{ML}. Since the parallel parasitic network is linear, there is no need for any "short" memory constraint in this case. Thus, for better model accuracy, values of T_{ML} which are still finite but quite longer than T_M can be chosen. Moreover, without loss of generality, the parasitic network pulse response has been assumed equal to zero over the short memory interval $[0, T_M]$. This in order to avoid ambiguities in model extraction, owing to the parallel connection of the parasitic network with the intrinsic transistor.

Eqn.(4) represents the general purpose NDC model capable of accurate prediction of the dynamic behaviour for different electron devices under large-signal operating conditions. It can be easily identified starting from conventional DC and pulsed characteristics and bias dependent small-signal parameter measurements, while its analytical form allows for a simple and systematic implementation in commercial microwave circuit simulators such as HP-MDS.

III. MODEL IDENTIFICATION

The model extraction procedure simply starts from the DC and pulsed I-V characteristic measurements on the electron device, which lead to the identification of the $F^{LF}[v(t), V_0]$ term in eqn.(4). Once the F^{LF} function has been identified, the "weights" $g_p[v(t)]$ and Δy_p of the voltage dynamic deviations can be computed for any value of the controlling voltage $v(t) = V_B = V_0$ by minimising the mean square discrepancy between the measured small-signal admittance $Y_{mis}[V_B, \omega_i](i = 1, ..., N_\omega)$ and the corresponding value predicted by model eqn.(4). More precisely, by linearising and then Fourier transforming eqn.(4) the model "fitting" to the measured intrinsic admittance $Y_{mis}[V_B, \omega_i]$ can be expressed in the form:

$$\begin{aligned} Y_{mis}[V_B, \omega_i] &= g^{LF}[V_B] + \\ &+ \sum_{p=1}^{N_D} g_p[V_B][e^{-j\omega_i p\Delta\tau} - 1] + \\ &+ \sum_{p=N_D+1}^{N_{DL}} \Delta y_p[e^{-j\omega_i p\Delta\tau} - 1] \quad (6) \end{aligned}$$

where $g^{LF}[V_B]$ is the differential conductance corresponding to the low-frequency term F^{LF}.

When a suitably wide set of different bias points $V_{B_l}(l = 1, ..., N_{B_1})$ and frequencies $\omega_i(i = 1, ..., N_w)$ has been chosen, expression (6) provides a set of $N_{B_1}N_w$ complex equations, which impose the congruence between the model small-signal response and the measured admittance Y_{mis}. It should be noted that these equations are linear with respect to the $N_{DL} + (N_{B_1} - 1)N_D$ unknowns $g_p[V_{B_l}]$, for $l = 1, ..., N_{B_1}, p = 1, ..., N_D$ and Δy_p for $p = N_D + 1, ..., N_{DL}$, which are the characteristic parameters of the purely dynamic part of the NDC model. Thus, the model extraction procedure can be based on simple and reliable algorithms for the mean-square solution of overdetermined systems of linear equations. This is an important advantage with respect to conventional models, whose parameter extraction normally involves nonlinear optimisation algorithms, which may suffer from different convergence problems, like the strong dependence on the starting point due to multiple local minima. Our model, instead, involves a much larger number of parameters, but their extraction from measured data can be carried out with simple and highly reliable numerical techniques.

In order to reduce the dimensions of the linear systems of equations to be solved, the above outlined model extraction procedure can be partitioned into two, smaller-sized subproblems. First, in order to derive the characteristic parameters Δy_p of the parallel parasitic network, which are in a relatively large number (owing to the longer memory time T_{ML}) but all bias independent, a smaller set of N_{B_2} different bias points V_{B_l} can be used. Then, with the given values of Δy_p, the bias-dependent characteristic parameters $g_p[V_{B_l}]$ of the nonlinear model can be more easily computed, for each of the many values of V_B to be considered over the device operating region. This can be done by separately solving a linear system of equations whose number of unknowns is small, owing to the much shorter memory time T_M.

The model extraction procedure enables the voltage-controlled terms $g_p[v]$ to be computed only over a grid of voltages $v = V_B$ within the device operating region, thus providing only a sampled characterisation of the nonlinear model functions. Clearly, since continuous and highly regular model functions are needed for accurate circuit simulation, suitable general-purpose methods for the interpolation or approximation of nonlinear functions defined by look-up tables are needed. In our model implementation, a recently proposed approach for nonlinear function approximation, based on sampled-signal theory [7], was adopted for its high flexibility in accurately describing different nonlinear electron device characteristics.

All the above considerations, which have been presented by considering for simplicity the case of a single-port device, can be easily generalised to multiport devices. In particular, it can be shown that the large-signal model eqn.(4) and the associated small-signal eqn.(6) used for model parameter extraction from small-signal bias-dependent measurements, are still valid, after obvious transformations from scalar to matrix form, also for multiport devices, as will be confirmed by the FET modelling results presented in Section V.

IV. MODEL IMPLEMENTATION IN HP-MDS

The implementation of the NDC model in the framework of commercial microwave circuit CAD tools can be easily performed due to the characteristics of its analytical formulation. Usually, the nature of such commercial available CAD tools only allow the user to insert device models through the standard interface. Previously proposed approaches [1,2] involved the representation of the device currents by means of nonlinear integral equations which generally can not be managed through this standard user interface. This caused the need for further approximations on the models equations in order to develop a quite different representation which was compatible with the constraints imposed by the CAD tool interfaces: a possible loss of accuracy was introduced only to make the model implementation feasible.

The NDC model expressed by eqn.(4) overcomes such a limitation. Its analytical representation describes the dynamics of the device just by a nonlinearly voltage controlled discrete convolution: this allows for an easy implementation of the model, with no loss of generality, by simply using the tools (i.e. nonlinear purely algebraic functions and delay operators) normally available for the construction of user-defined models.

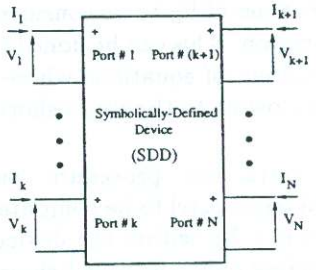


Fig. 2: General N-port SDD device available in the HP-MDS schematic environment.

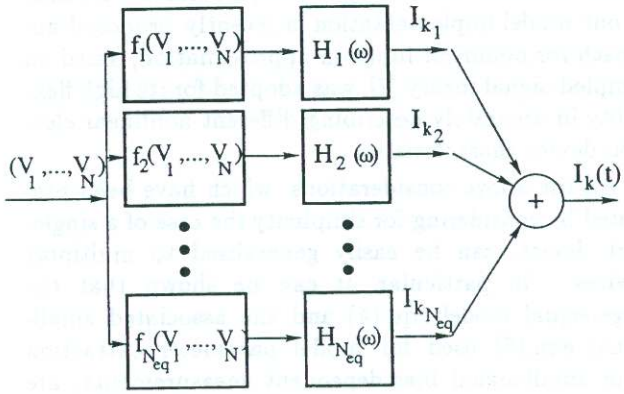


Fig. 3: Evaluating process of a generic SDD-port current i_k starting from the applied voltages $v_1, v_2, ..., v_N$.

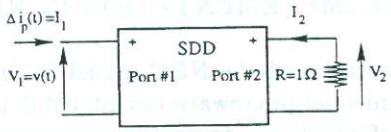


Fig. 4: Implementation of the p-th current contribution $\Delta i_p(t)$ in the NDC model formulation for a single port device by means of a two port SDD element.

In the following of this paper the NDC model implementation in the framework of the HP-MDS microwave circuit simulator will be considered. In particular the Symbolically-Defined Device (SDD) shown in Fig. 2 is adopted, as an user-interface tool capable of accurate implementation of quite complex voltage controlled current contributions, such those that appear in the purely dynamic term in eqn.(4). In general, a SDD element is a N-port network whose instantaneous current values i_k $(k = 1, ..., N)$ can be described by means of N_{eq} nonlinear functions of the applied voltages v_k, as shown in eqn.(7):

$$i_k = f_1(v_1, v_2, ..., v_N) + ... + f_{N_{eq}}(v_1, v_2, ..., v_N) \quad (7)$$

Moreover, before the final value i_k is calculated, a weighting function $H_i(\omega)$ can be applied to the harmonics of each contribution $f_i(v_1, v_2, ..., v_N)$. Fig. 3 shows the evaluation process of i_k.

The result is a quite flexible tool which not only allows for the simulation of nonlinear memoryless characteristics i=$F(v)$, but also the implementation of current contributions as those in the NDC model eqn.(4). In particular for each term of the single port modelled device $p \in [1, ..., N_D]$:

$$\Delta i_p(t) = g_p[v(t)](v(t - p\Delta\tau) - v(t)) \quad (8)$$

a two-port SDD element, composed by a main port and a second auxiliary port, has been taken into account as shown in Fig. 4. The voltage v_1 applied to the first port of the SDD component corresponds to the voltage $v(t)$ of the modelled device, while the current contribution $\Delta i_p(t)$ is obtained by inserting the following equations in the SDD definition form:

$$i_1 = g_p[v_1](v_2 - v_1) \quad , \quad i_2 = -v_1 \quad (9)$$

where the voltage v_2 corresponds to the delayed term $v(t - p\Delta\tau)$, since the delay weighting function $H_p(\omega) = e^{-j\omega p\Delta\tau}$ has been applied to the current i_2.

Altogether, $N_D + 1$ two-port SDD elements are needed to implement the complete monodimensional device, with no approximations on the general NDC model formulation (4). It is important to note that, with short memory time T_M, just a small number N_D of delayed terms (8) are needed in eqn.(4) to achieve good agreements between the NDC model prediction of the device dynamics and experimental results: thus the number of SDD elements used to perform the HP-MDS implementation of the NDC model (4) is quite limited.

The two dimensional extension of the NDC model for a transistor device is described by eqn.(10):

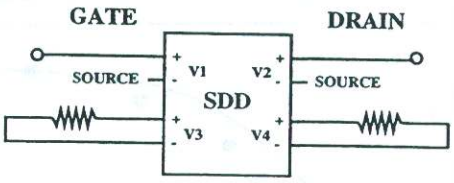
$$\begin{aligned} \underline{i}(t) &= \underline{F}^{LF}[\underline{v}(t), \underline{V}_0] + \\ &+ \sum_{p=1}^{N_D} \underline{g}_p[\underline{v}(t)][\underline{v}(t - p\Delta\tau) - \underline{v}(t)] + \\ &+ \underline{\Delta i}_{par}(t) \quad , \quad \underline{i}(t) = [i_g(t), i_d(t)] \end{aligned} \quad (10)$$

where the $\underline{g}_p[\underline{v}(t)]$ parameters, which characterise the purely-dynamic behaviour of the device, are now N_D[2x2]-matrices whose elements (indicated as "gp_ij" in Fig. 5) are functions of the voltages $(\underline{v}(t) = [v_g(t), v_d(t)]$) applied respectively to the transistor gate and drain. The HP-MDS implementation of each dynamic current contribution $(p \in [1, ..., N_D])$:

$$\Delta \underline{i}_p(t) = \underline{g}_p[\underline{v}(t)][\underline{v}(t - p\Delta\tau) - \underline{v}(t)] \quad (11)$$

involves a four-port SDD element (the two gate-source and drain-source main ports and two auxiliary ports closed on $R = 1\Omega$ resistors) and is performed according to the same approach described for the monodimensional device. The MDS-like schematic presented in Fig. 5 shows the actual lay-out of the p-th SDD device.

As far as the DC and low-frequency device modeling is concerned, the $\underline{F}^{LF}[\underline{v}(t), \underline{V}_0]$ term in the two



PORT CURRENTS

PORT	W.F.	EXPRESSION = I
1	0	IgpHF
2	0	IdpHF
3	2	-V1
4	2	-V2

WEIGHT. FUNCT.

W.F.	EXPR.
0	1
2	DELAYp

EQUATION: IgpHF = gp_11[V1,V2]*(V3-V1)+gp_12[V1,V2]*(V4-V2)
EQUATION: IdpHF = gp_21[V1,V2]*(V3-V1)+gp_22[V1,V2]*(V4-V2)
EQUATION: DELAYp = COS(omega*p*dtau)-J*SIN(omega*p*dtau)

Fig. 5: HP-MDS implementation of the p-th current contribution (see eqn. (11)) of the nonlinear high-frequency purely dynamic part of the NDC model. In the figure, "gp_ij" (with i,j=1,2) are "dataset variables" corresponding to the terms $\underline{g}_p[\underline{v}(t)]$ and *dtau* represents the elementary delay.

dimensional model formulation (10) can be analogously implemented using a four-port SDD element, but with different constitutive equations. The complete expression of current contribution $\underline{F}^{LF} = [F_g^{LF}, F_d^{LF}]$ can be expressed as [1]:

$$\begin{aligned} F_g^{LF}[\underline{v}(t)] &= F_g^{DC}[v_g(t), v_d(t)] \\ F_d^{LF}[\underline{v}(t), \underline{V}_0] &= F_d^{DC}[v_g(t), v_d(t)] + \\ &+ g_{21LF}[v_g(t), v_d(t)][v_g(t) - V_{G0}] + \\ &+ g_{22LF}[v_g(t), v_d(t)][v_d(t) - V_{D0}] \end{aligned} \quad (12)$$

where g_{21LF} and g_{22LF} are suitable functions identified starting from conventional DC and low-frequency small signal measurements as:

$$\begin{aligned} \widetilde{g}_{21}^{LF}[v_g, v_d] &= Real\{Y_{21}[v_g, v_d]\} - g_{21}^{DC}[v_g, v_d] \\ \widetilde{g}_{22}^{LF}[v_g, v_d] &= Real\{Y_{22}[v_g, v_d]\} - g_{22}^{DC}[v_g, v_d] \end{aligned} \quad (13)$$

In particular, the admittance parameters Y can be obtained by means of S-parameter measurements performed at a suitable frequency above the cut-off due to dispersive effects but low enough to neglect transistor reactive effects, and by subsequent matrix transformation formulae.

The four-port SDD device used in the implementation is characterised by port number one and two which coincide with the gate and drain device ports, while port three and four are needed in order to evaluate the mean values V_{G0} and V_{D0} required in eqn.(12). To this aim, a *rectangular* $H_{LPF}(\omega)$ weigthing function

[1] Eqns.(12) represent simplified model expressions for low-frequency dispersive effects since they do not take into account self-heating phenomena. More accurate modelling approaches may be considered such as those presented in [5,6].

PORT CURRENTS

PORT	W.F.	EXPRESSION = I
1	0	IgDC[V1,V2]
2	0	IdDC[V1,V2]+IdLF
3	2	-V1
4	2	-V2

WEIGHT. FUNCT.

W.F.	EXPR.
0	1
2	lpf

EQUATION: IdLF = fg[V1,V2]*(V1-V3)+fd[V1,V2]*(V2-V4)

Fig. 6: SDD's equations for the nonlinear DC and low-frequency dynamic part of the NDC model. In the figure, $IgDC, IdDC$ are the "dataset variables" corresponding to the gate and drain static current look-up tables and fg, fd the "dataset variables" corresponding to the $\widetilde{g}_{21}^{LF}$ and $\widetilde{g}_{22}^{LF}$ functions. Currents are defined positive when flowing into the SDD. Resistances value: 1Ω; lpf: low-pass filter "dataset variable" implementing $H_{LPF}(\omega)$.

($H_{LPF}(\omega) = 1$, $\omega \in [0, 2\pi f_{cut}]$, $H_{LPF}(\omega) = 0$ elsewhere) that sintethises an ideal low-pass filter transformation [2] is applied to the currents ($i_3 = -v_1$, $v_1 = v_g(t)$ and $i_4 = -v_2$, $v_2 = v_d(t)$) at port three and four, which are closed on $R = 1\Omega$ resistors: as the result of the SDD elaboration, voltages v_3 and v_4 at these ports coincide with values V_{G0} and V_{D0} respectively. Figure 6 shows the equations of the four-port SDD device which implements the term $\underline{F}^{LF}[\underline{v}(t), \underline{V}_0]$. The contributions F_g^{DC} and F_d^{DC} are indicated with the notation $IgDC$ and $IdDC$.

V. EXPERIMENTAL RESULTS

Experimental validation tests have been carried out by applying the implemented NDC model for the large-signal intermodulation prediction of a cold-FET mixer (i.e., $V_{DS} = 0V$) based on a PHEMT device with $f_{LO} = 2$ GHz, $f_{RF1} = 13.99$ GHz, $f_{RF2} = 14.01$ GHz. First, the DC characteristics and small-signal S-parameter measurements have been de-embedded from parasitic resistances and inductances. Then the NDC model and the parallel linear parasitic network were identified on the basis of the outlined procedure by using $T_M = 6ps$, $N_D = 3$ ($\Delta\tau = 2ps$), $N_{DL} = 30$. The good agreement shown in Fig. 7 between measured and simulated small-signal scattering parameters confirms that the small-signal frequency response of the device is not substantially modified after adopting the short memory time T_M (good agreement was generally found for a large number of different bias conditions).

In Fig. 8 the NDC-based, harmonic balance two-tone simulation of the cold-FET mixer versus local oscillator power is compared with measured data. Good prediction accuracy is obtained both at high P_{LO} val-

[2] The ideal low-pass filter can be chosen with a cutoff frequency comparable with that of the dispersive effects due to traps and thermal phenomena. For example, f_{cut} = 10KHz was here adopted.

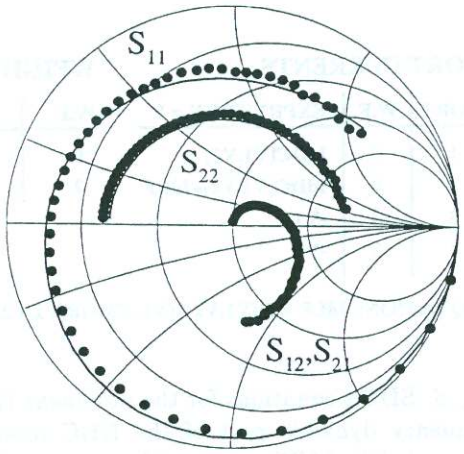


Fig. 7: Comparison between S-parameter (1-50GHz) measured (•) and simulated (—) through the NDC Model for a PHEMT device (V_{GS}=-1V, V_{DS}=0V).

	MOD.	MEAS.
C_G	-7.3 dB	-8.5 dB
$IP3$	14.3 dBm	14 dBm

Table 1: Intermodulation prediction for a cold-FET mixer based on a PHEMT device using the NDC Model (V_{GS}=V_P, P_{LO}=8.5dBm, P_{RF1}=P_{RF2}=-2dBm, f_{LO}=2GHz, f_{RF1}=13.99GHz, f_{RF2}=14.01GHz). Measured data after [8].

ues where the v_{gs} voltage swing covers the whole safe operating range, and at very low P_{LO} values where the "local" properties of the model (and the interpolator/approximator algorithms) play an important role. Moreover, the intermodulation distorsion analysis results presented in Tab.1 indicate that the NDC model is capable of accurate predictions also under low-amplitude RF input signals (the results in Fig. 8 and Tab .1 were obtained applying in nonlinear simulations the highly accurate interpolation techniques described in [7]).

VI. Conclusion

A Nonlinear Discrete Convolution model for electron devices has been proposed. The model provides accurate performance prediction under nonlinear operation at microwave frequencies and can be identified through a simple, systematic and unambiguous procedure on the basis of conventional DC and small-signal measurements. In the paper, beside the model experimental validation, details have been given on the model implementation in the HP-MDS environment by means of Symbolically Defined Devices.

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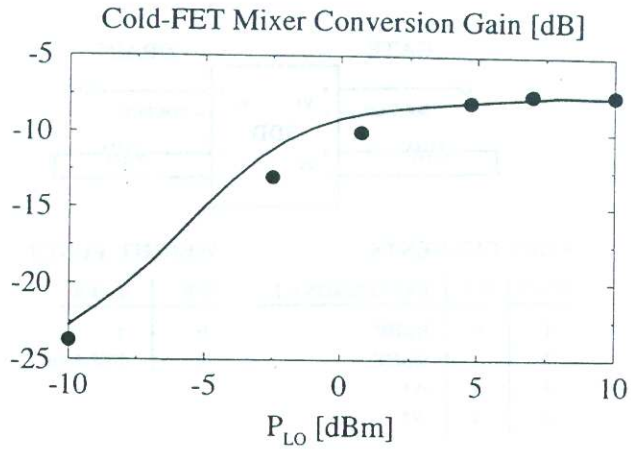

Fig. 8: Conversion gain prediction for a cold-FET mixer based on a PHEMT device using the NDC Model (V_{GS}=-0.55V, P_{RF}=-5dBm, f_{LO}=2GHz, f_{RF}=14GHz). Measured data after [8].

VII. References

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