High Efficiency 1.4 W Power Amplifier for K-Band Satellite Communication System

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***Abstract* - A high efficiency 1.4 W MMIC power in the K-Band frequency band has been developed. A process technology optimized for high efficiency performance and an accurate design technique allowed us to achieve a power added efficiency of 42% with good noise power ratio figure. These performance make this device suitable for K-Band commercial satellite systems as part of antenna element array.**

I. INTRODUCTION

Next generation of K-Band commercial satellite systems are projected to use highly integrated circuit assemblies as parts of the critical antenna element array. One key component is the power amplifier which has to provide very high efficiency and stable output power at extreme temperatures. The best candidate technology presenting such characteristics in K-Band is the power pseudomorphic HEMT (pHEMT). This technology has been developed in Fujitsu achieving a high power added efficiency higher than 65% [1]. An antenna array on board satellite systems requires a large number of power amplifiers covering a wide range of output power levels. At each power level the efficiency must be maximized. Multiple stage amplifiers of medium output power such as 200-400mW will provide an optimum combination of p-PHEMT size and matching circuit losses to achieve highest efficiency. In fact, the size of the active device is reasonably small but in the same time the operational point of each active device is very close to the gain compression region (maximum efficiency). Low output power amplifiers have lower efficiency due to the limitation of the driver stage. Indeed, the smallest gate width allowed by the process is necessary at the first and second stages but the operational power can be anyway several dB output back-off (low efficiency). This will bring a strong degradation in the overall amplifier efficiency figure. Amplifiers with high output power (Pout>0.5W) exhibit also significantly lower efficiency as compared with those of medium power. This is due to large size gate width FET layout, complex interstage configurations, output matching loss and chip area limitations. However, the high power devices have the major impact on the overall antenna element array efficiency. We realized a high power amplifiers with output power better than 31dBm while maintaining the power added efficiency very high. Design, measured performance details of this MMIC amplifier is presented in this paper.

II. PROCESS TECHNOLOGY

The process technology used is the power pHEMT. This device has an N-AlGaAs/InGaAs/N-AlGaAs double hetero-structure. In order to obtain the highest efficiency, we optimized device parameters such as the gate length, double recessed structure, and the location of recessed region between ohmic electrodes. The doping density in AlGaAs layers was also optimized in order to achieve the higher gain and efficiency. The gate length is 0.25um. We adopted a highly reliable WSi/Au T-shaped gate structure.

The power performance of the pHEMT was measured at 18GHz with total gate width Wg=600um. The unit gate width is 50um. We used both active and passive load-pull technique to derive the maximum efficiency. No intentional harmonic tuning was applied. Figure 1 shows the test results of load-pull measurement at Vds=7V, Ids=20mA(50%-Idss, Class-A). As shown in this figure, we achieved the 64% power added efficiency at 1dB gain compression point with 22.8dBm output power and 9.2dB power gain. The peak value of the power added efficiency is 68% with 23.5dBm (225mW) output power and 81% drain efficiency at the 2.5dB gain compression point [1]. This efficiency is the highest value compared with the reported K-band solid state power transistors[2]. Our power pHEMT shows over 60% power added efficiency up to Vds=9V. It means that this device is of great advantage to achieve high power, high gain and high efficiency MMIC.

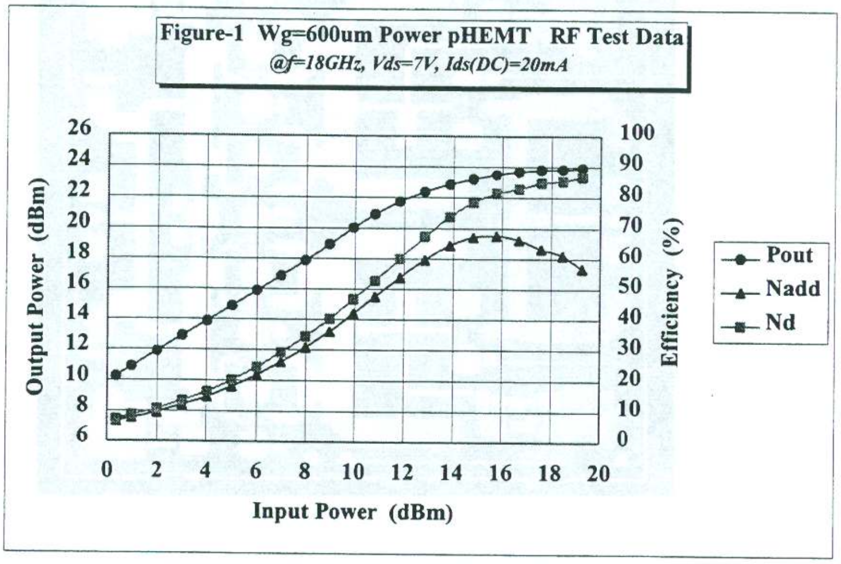

Fig. 1 – 600um Power pHemt performance

III. DESIGN APPROACH

We designed a 1.4 Watt 2-stage MMIC amplifier in the 18-21GHz band using this power pHEMT technology. For this design we imposed the impedance of the output matching network fixed at the maximum efficiency condition that was given by load-pull measurement at the fundamental frequency 19 GHz. Particular attention was given to minimize output and interstage matching circuit losses due to their dominant role in achieving high efficiency. The first stage was matched also for high efficiency and the size of the active device has been chosen such that the peak of efficiency can be reached at the desired output power level.

The second harmonic has been short circuited at the output of the first stage pHEMT. No intentional tuning of the second harmonic has been applied at the output stage but the magnitude of output impedance at the second harmonic has been mantained as much as possible close to 1 to minimize the effect of the second harmonic on the time domain voltage. In this way the voltage across the drain-source current generator is almost a pure sinusoid. A compromise between the control of the second harmonic, chip size and simplicity of the circuit has been necessary.

We chose a GaAs substrate thickness of 75μm to reduce the substrate loss, allowing the use of smaller gate width devices, and by increasing the overall size of the chip. The use of lumped elements has been minimized to improve the yield in production especially in the output stage.

The output stage has a gate width size of 5.28mm and it is realized by the combination of eight 660μm pHEMT. The use of small unit pHEMT cells increases the efficiency and the gain. The matching from 50 ohm to the desired optimum impedance has been realized within the combining network to reduce the chip size and the overall loss. The loss due to the combination and the matching are of the order of 0.7dB that translates to a network efficiency of 91%.

The overall device performance have been optimized at the bias point Vds=6V and Ids=50%Idss where we have the best compromise between power added efficiency and linearity.

The chip size of the 2-stage amplifier is shown in Fig.2 and the chip size is $3.6x3.7mm^2$.

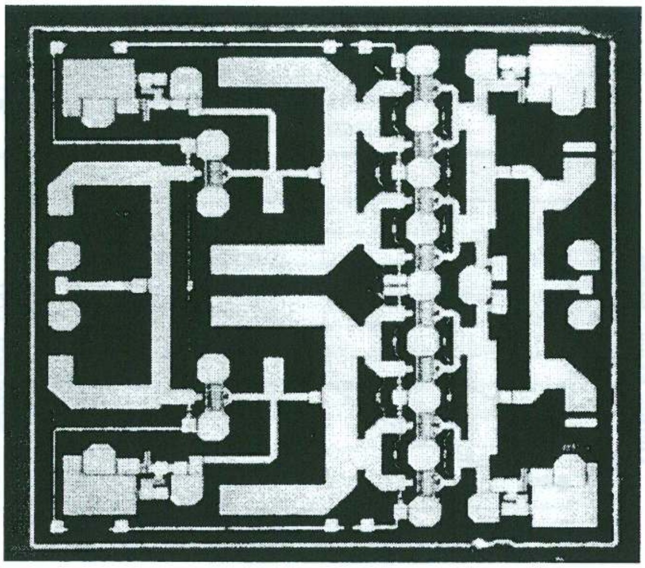

Fig. 2 – Picture of the 1.4W MMIC amplifier

IV. TEST RESULTS

The two stage amplifier has been tested and a 42% power added efficiency with 31.5dBm output power (1.4W) and 18dB of linear gain at Vds=6V Ids(DC)=50%Idss (class AB) has been achieved. In Figure 2 and 3 the performance of the amplifier are shown. Figure 4 shows the picture of the chip. The overall chip size is 3.4x3.5mm^2. This amplifier, when biased at Vdd=8V, delivers an output power higher than 32 dBm with a power added efficiency of 41%.

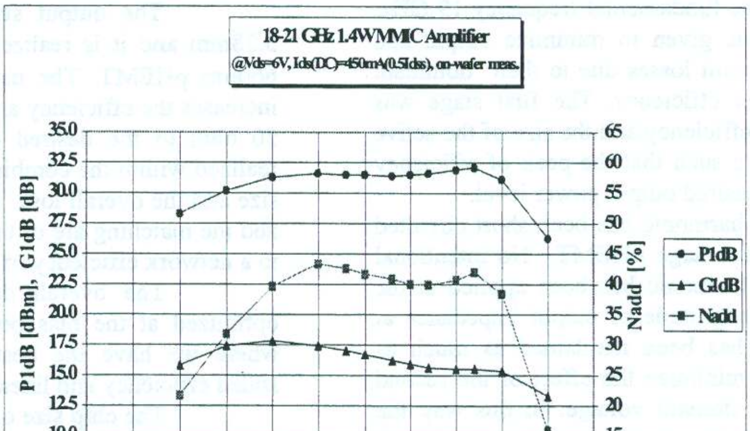

Fig.3 – 1.4W MMIC Performance

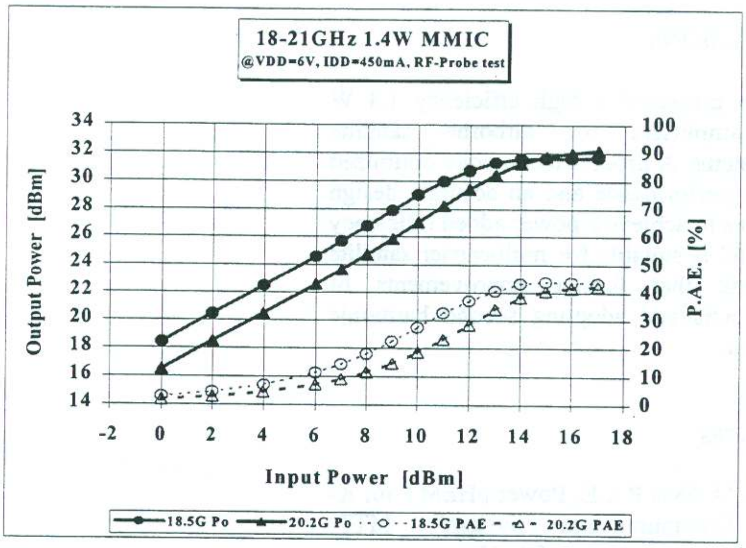

Fig.4 – 1.4W MMIC Performance

Linearity is an important specification for multicarrier satellite systems, therefore Noise Rower Ratio (NPR) [3] performance have been also tested at different bias conditions. The NPR test results at 20GHz, as a function of the bias current are reported in Fig.5. As shown, with the increase of the Ids current the NPR figure improves but at the expenses of the efficiency. When biased at Ids=50%Idss and Pout=27dBm the NPR is of the order of 17.5dBc.

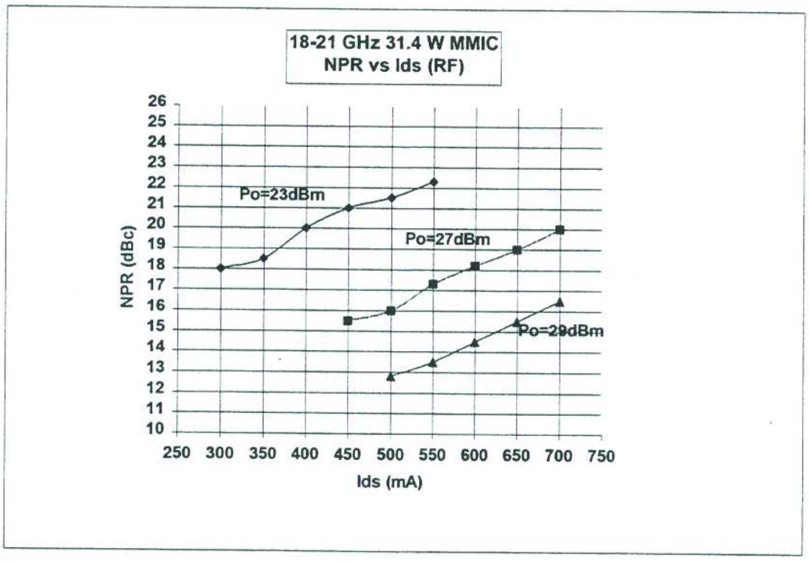

Fig.5 – 31.5 W MMIC NPR Performance

V. CONCLUSIONS

We have presented a high efficiency 1.4 W MMIC power amplifiers for airborne satellite communication systems. A process technology optimized for high efficiency performance and an accurate design technique allowed us to achieve a power added efficiency of 42%. This MMIC is suitable for multicarrier satellite systems. We think that further improvements of efficiency can be achieved adopting second harmonic matching techniques.

VI. REFERENCES

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