

Technologies for Telecom & Datacom Data Transmissions

And the winner is: Just plain Mesfets

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Abstract

This paper describes the system architecture and the critical components for transmission of wide-band serial data over fiber or cable. Technology tradeoffs and cost issues are discussed.

Introduction and background

About 10 years ago, the core of the world-wide telephone infrastructure was in the process of a major shift to an international digital standard for transmission: SONET/SDH. The more recent explosive growth of internet traffic is causing a transition of the network from voice-centric to data centric, and a seemingly insatiable demand for ever greater bandwidth in the transmission networks.

These developments have huge implications for technologies that are adaptable to transmission of wide-band data. As the business potential grows, more competitive technologies emerge as candidates to implement the critical components for this application. In this paper, we seek to highlight the performance requirements and compare the relative attributes of semiconductor technologies as they apply to these systems.

Generic Transmission Architecture

Compelling technical and economic considerations point to architectures which employ aggregation of the data into high rate serial binary streams. This holds true for long haul SONET/SDH transmission over fiber as well as for short haul datacommunication links such as fibre-channel or Gigabit Ethernet, over fiber or cable.

Fig (1) shows the essential functions of a system which provisions data for transmission over a serial medium. The categories: data grooming, data transport service, and transport means are generic, but here the specific example is the use of SONET or SDH transport.

The critical components of a telecom transmission set (or equivalently a datacom network switch) are shown in fig. (2). The transition between serial and parallel data occurs in the multiplexer/demultiplexer, and the width of the parallel word is adjusted for optimum system partition between different technologies. Generally, the processor VLSI function is implemented in CMOS and the word width is chosen to result in a signaling rate, which can be accommodated in the CMOS VLSI.

The aggregate switching bandwidth is ever increasing. Commercial state of the art today is more than 300 Gbit/sec. At these bandwidths, the switching problem is quite complex and the parallel data is often reserialized for efficient routing within the switch.

This is essentially the environment, which determines the operational requirements placed on the critical components. Referring back to fig. (2), the system basically divides itself into 3 sections:

the receive electronics, the transmit electronics and the switch. A useful overall performance figure of merit for such a transmission system is the bit-error-rate (BER). This is a measure of the integrity of the signal as it is transmitted through the fiber, received and processed into binary logic levels. Often times the system OEMs are required to guarantee a BER to their customers (The service providers) who, in turn, are required to guarantee a level of performance (QOS, COS) to their customers, the end user. The critical components in the transmission system are "critical" in so far as they effect the BER.

Fig. (3) shows a typical "good" eye diagram (i.e. low BER) at OC-48 (2.488 Gb/sec), and is produced by a NRZ random sequence of '1's and '0's. The Salient features include low amplitude of noise in the logic '1' and logic '0' state, sharp rise and fall times, as well as low duration of jitter during the transitions. These factors lead to a relatively large open "window" for sampling the data. The characteristics of the eye-pattern are strongly influenced by the performance attributes of the technology used for the "critical components". For comparison, a "bad" eye diagram with high BER is shown in fig. (4).

System Components

On the receive side, the optical to electrical conversion in the photo-diode results, in a photo current as low as a few micro-amps. This photo current is converted to a voltage signal in the trans-impedance amplifier. This component is a wide-band low-noise device and produces a peak-to-peak signal of a few millivolts. This signal is further amplified in a post-amplifier or limiting amplifier to usable logic levels. The post- amplifier is required to have sufficient gain-bandwidth product (GBW) to achieve fast slew-rates at its output. Fast slew-rates minimize transition times and thus the duration of ambiguity which would lead to jitter and increased BER.

The transmitted data format is non-return-to-zero (NRZ) binary with embedded clock. The spectrum of NRZ data contains no power at the fundamental clock frequency. Second-order non-linear processing is required (usually in a PLL) to recover the clock to properly sample the data. The specification for jitter is quite stringent (typically 1% of the bit period RMS) and must accommodate the conflicting requirements of tolerance to input jitter as well as minimizing jitter transfer. On the transmit side, the clock multiplier PLL must minimize jitter generation.

The multiplexer, demultiplexer and the switch fabric require high speed and low power logic. High bandwidth logic elements minimize transition times and thereby jitter.

Technology Candidates & Tradeoffs

In the typical application, the required data-rate is fixed. For telecom transmission applications, the standard data rates are determined by the SONET/SDH standard. The higher standard rates are:

SDH/SONET			Successful
<u>Designation</u>	<u>Data-rate</u>	<u>Status</u>	<u>Candidate Technologies</u>
STM4/OC-12	~622Mb/sec	deployed	GaAs, Si Bipolar, CMOS
STM16/OC-48	~2.5Gb/sec	deployed	GaAs, Si Bipolar
STM-64/OC-192	~10Gb/sec	Early deployment	GaAs, Si-Ge
STM-256/OC-768	~40Gb/sec	development	not yet determined

Assuming a candidate technology has the bandwidth, edge-rate, and noise capability for a given application, then the tradeoffs are power dissipation and cost.

Strategies to reduce power dissipation depend on the technology type. For the dominant semiconductor technology, CMOS, the strategy is scaling. Reducing feature sizes improves density. The minimum size transistor may control less current than the previous generation, but the switched current charges disproportionately smaller interconnect capacitance, so the same speed is achieved with less power, or higher speed with the same power compared to the previous generation. This strategy applies to other VLSI Fet technologies, namely H-GaAs. Scaling is the key to reducing power dissipation in succeeding generations of Fet technologies. The technique to minimize power dissipation in bipolar technologies is typically to use a circuit topology which make use of stacking logical functions vertically so that a unit of current drawn from the power supply operates multiple logic functions. This technique does not scale with succeeding generations and infact as system power supply voltages are reduced, the number of stacked logic functions must also be reduced. This CML (Current mode logic) circuit topology does not benefit directly from technology scaling. Furthermore as fig (5) shows, bipolar transistors have a more complex structure compared to Fets, and in general are larger. Bipolar technology, however, benefits from relatively greater transconductance compared with Fets. This is particularly useful in the design of the analog functions.

Component Cost

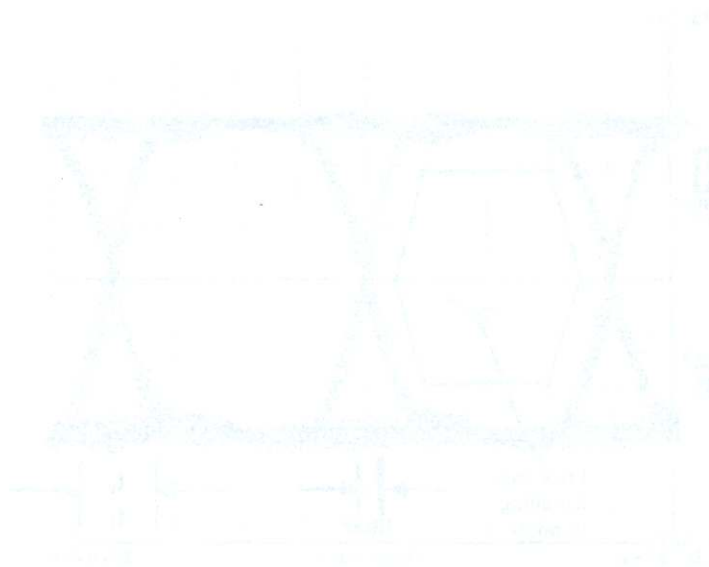
At the current state of the art, GaAs and bipolar Si-Ge are candidates at OC-192 (10 Gb/sec) and higher, while CMOS at 0.18 μ m design rules will encroach at OC-48 (2.5 Gb/sec) and lower data rates. As the demand for bandwidth grows, so do the volumes of products comprising the "critical chip-set". As is inevitable in the semiconductor industry, greater volume drives down the price and so cost must follow. Even if all other things are equal (performance, power), ultimately the lowest cost product dominates the application. The perception that "if its CMOS its cheap" is usually true. The generalization: "if its silicon its cheap" is definitely not necessarily true. The cost of a semiconductor product is really determined by manufacturing volume and by process complexity. It is typically (erroneously) assumed that since the cost of GaAs starting material is higher, it follows that GaAs based products are necessarily more costly. The factors, which contribute to the overall cost of a finished product, are the following:

- Number of masking levels
- Wafer size
- Wafer cost
- Number of chips per wafer
- Fab. Capitalization/capacity utilization

The cost to produce a semiconductor product is linearly dependent on the process complexity (number of masking levels), as well as on the number of functional die per wafer. The latter is, in turn technology dependent – being higher for technologies that can pack a given function into a smaller area such as CMOS and VLSI GaAs (H-GaAs). Using these assumptions as well as the reasonable assumption of depreciation based on a manufacturing facility with \$80M capitalization and capable of 1400 wafer starts per week, we can make a quantitative comparison of cost associated with different technologies producing the same product. This comparison is illustrated in the table below. In this table we include technologies which are the prevalent commercial competitors for the target application. The important parameter, number of masking levels, assumes a reasonably complex chip with 4 layers of interconnect metalization. 8" (200mm) CMOS is included for reference but this technology currently really does not apply above OC-48 (2.5 GB/sec).

Due to its remarkable simplicity, high yield manufacturability, and low power, H-GaAs technology dominates the OC-48 chip-set market and is emerging as the lowest cost alternative at OC-192. As an example, a SONET/SDH compatible OC-192 16:1 multiplexer, demultiplexer chip set is at least 5 times lower cost in H-GaAs technology compared to the equivalent function in any other technology.

In summary, customers buy products – not technology. When there is a volume market, prices will be reduced and so cost must be reduced, and that technology capable of producing the lowest cost product will dominate the market.



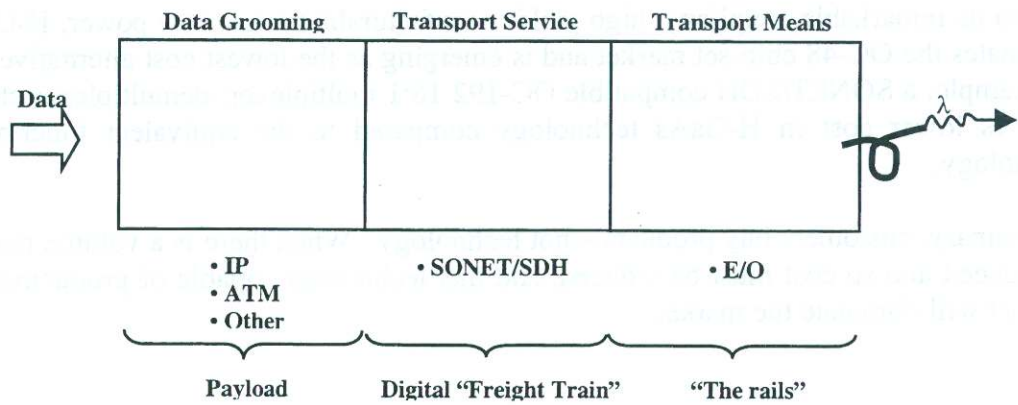


Fig. 1

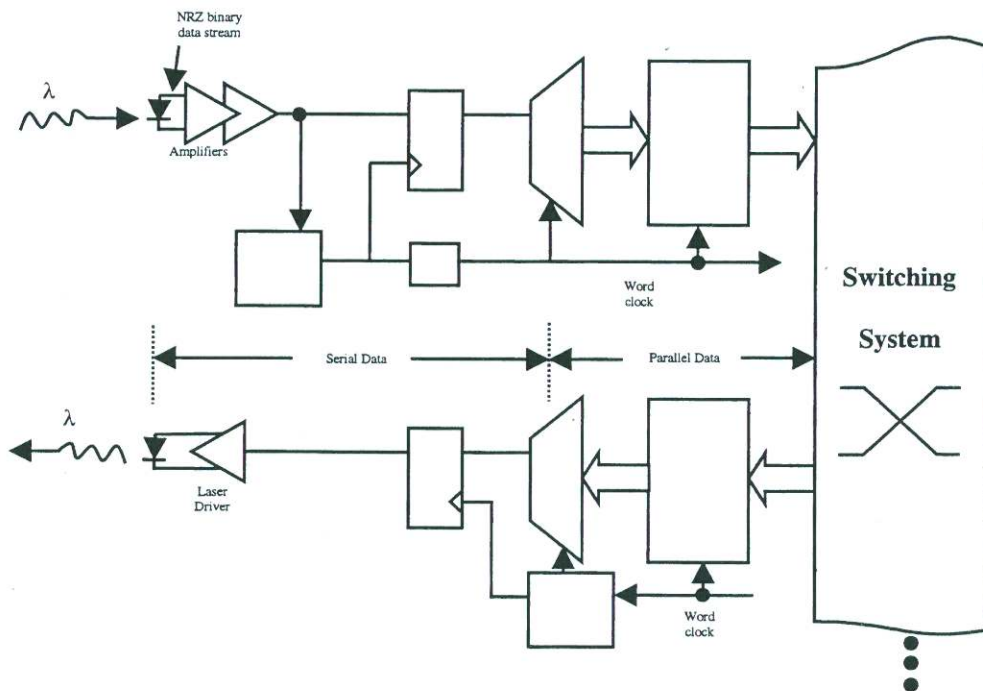


Fig. 2

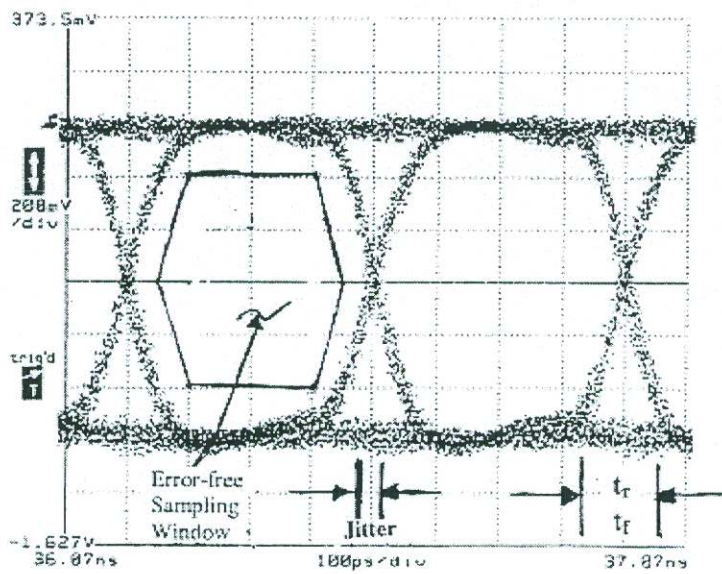


Fig. 3

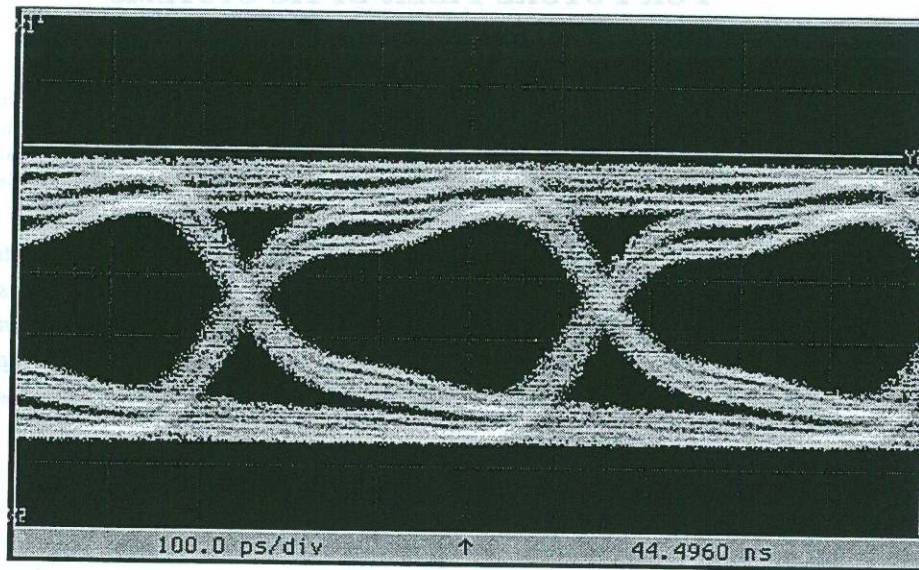
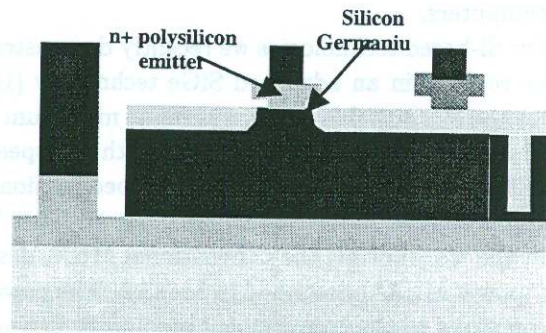


Fig. 4



MESFET Cross-section



Bipolar Cross-section

Fig. 5

Cost Factor	8"CMOS	6" H-GaAs	4"bipolar	6" bipolar	8"Si-Ge	Fab-less 8" Si-Ge
Mask Levles	~14	14	28	28	28	4 layer Metal
Depreciation	\$220	\$220	\$440	\$440	(>440)	
Raw Wafer	\$40	\$380	\$50	\$75	\$200	
Labor/Chemicals/Occupancy	\$280	\$280	\$560	\$560	*	
Total Cost	\$540	\$880	\$1050	\$1075	\$3000*	\$5000
Cost per sq. mm	\$0.017	\$0.050	\$0.134	\$0.061	\$0.1	\$0.16
Ckt density factor	0.7	1	1-1.5	1-1.5	1-1.5	1-1.5
Effective Cost	\$0.12	\$0.50	\$1.134-\$0.201	\$0.061-\$0.91	\$1-\$0.15	\$0.16-\$0.24
Relative Cost 0.25	0.25	1	2.7 - 4	1.2 - 1.8	2-3	3-4.8

Table 1.