DUAL-FUNCTION MMIC FOR MICROWAVE DIGITAL RADIO

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***ABSTRACT* - This paper describes the design and measured results of a dual-function power amplifier MMIC, which is intended to replace the existing hybrid solution in the microwave digital link applications. This circuit achieves at least 26dBm saturated output power from 12GHz to 16GHz and more than 40dB dynamic range by adjusting the bias voltage without any oscillation observed.**

I. INTRODUCTION

Commercial wireless communication systems have extended the frequency range to microwave and millimeter wave for broader bandwidth in order to accommodate the increasing voice and data traffics [1]-[2]. Figure 1 illustrates the current architecture of the RF front-end for microwave digital link system. Hybrid solution is used for the power amplifier, which consists of three discrete devices. The output power of high dynamic range is achieved by using a mechanical attenuator. To reduce the cost and size of the RF front-end, a broadband, variable-gain power amplifier MMIC is preferred, which will replace both the power amplifier and attenuator. In this paper, such dual-function, broadband power amplifier MMIC will be presented, which was designed to cover the frequency range from 12GHz to 16GHz.

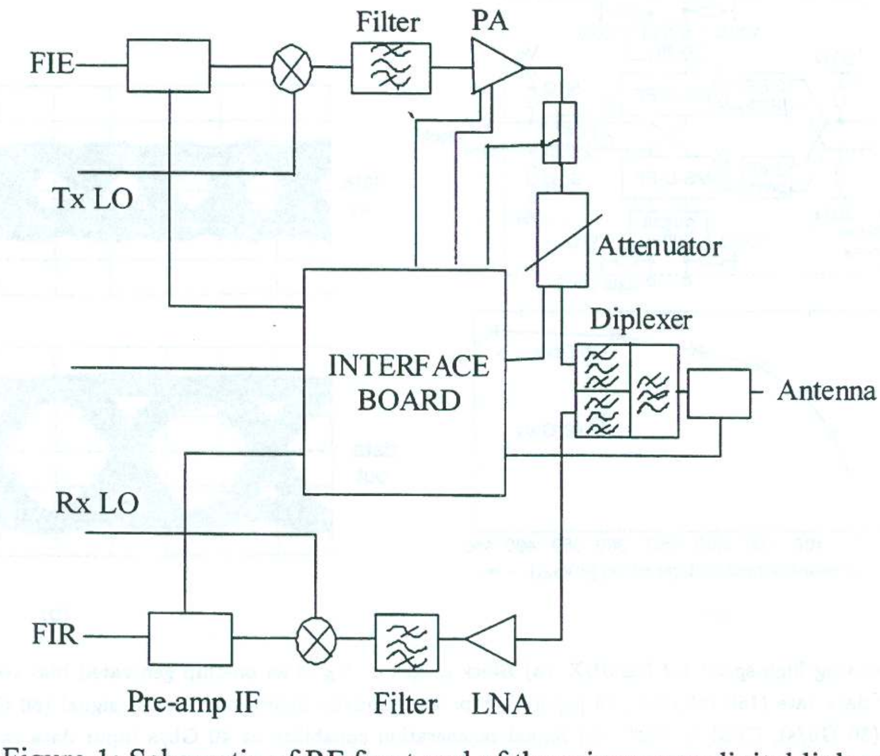

Figure 1: Schematic of RF front-end of the microwave digital link system.

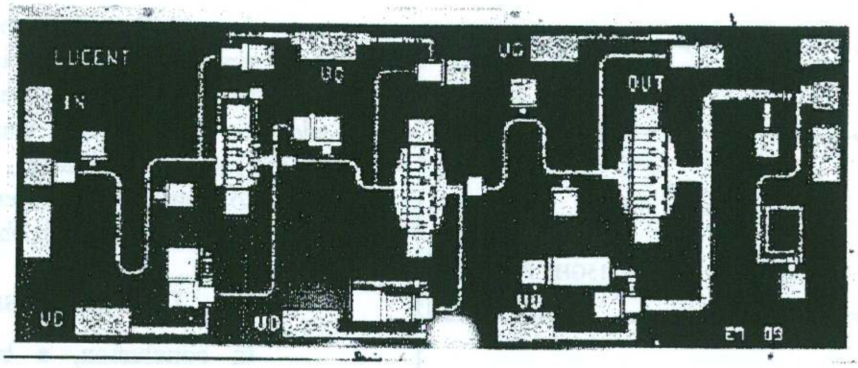

Figure 2: Photograph of the power amplifier MMIC. The chip size is 3mm x 1.2mm.

II. Circuit Topology

Filtronic Solid State's 0.25μm Double Heterojunction GaAs PHEMT process was chosen for this design. The typical cutoff frequency, f_t, of this process is 50GHz with the guaranteed minimum of 40GHz. Because there is no accurate non-linear device models available for this process, only measured S-parameter data and DC IV curves of various devices with different gate widths were used for the design. Thin film TaN resistor (50Ω/square) and MIM capacitor (0.6fF/μm) are available for matching networks. The wafer is thinned down to 100μm with via hole for backside ground contact. The design goal is to achieve 20dB minimum gain with flat frequency response, and 26dBm saturated output power (P_{sat}) from 12GHz to 16GHz. Figure 2 shows the photograph of the final chip layout. It consists of three stages with the resistive feedback topology as the first stage (400μm device) to obtain good input return loss. The second and third stages consist of a 600μm and 840μm devices, respectively. Shunt MIM capacitors are used extensively for matching networks. The real part of the optimal load of each device was determined from the DC IV curve and the imaginary part was determined from the measured S-parameter data with proper input matching. The interstage matching networks were optimized to obtain flat gain response across the band of interest. At every drain bias pad, there is a parallel path, consisting of 50Ω resistor in series with a capacitor to ground for stability consideration. Each gate bias is provided through a 300Ω resistor and there are two gate bias pads available to adjust the input matching and output power, if needed. This MMIC is operated at 5V and the final chip size is 3mm x 1.2mm.

III. Measured Results

Because of power consumption of this MMIC (2.5W), this chip was first mounted on a circuit board, which provides the DC biasing as well as the heat-sinking purpose. Then the on-wafer measurement for small-signal S-parameter was performed and the result is shown in Figure 3. It achieves minimum 20dB gain from 12GHz to 16GHz with good input matching. However, the

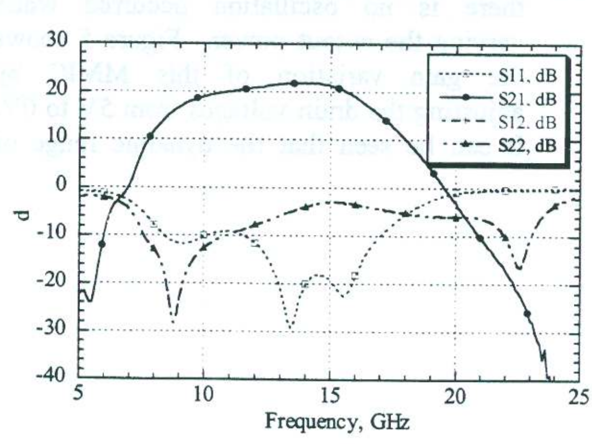

Figure 3: On-wafer measured small-signal frequency

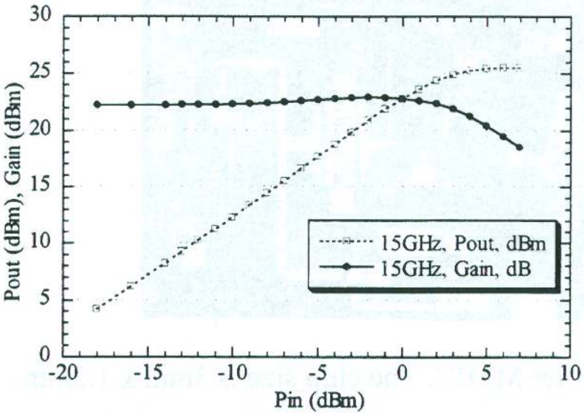

Figure 4: Power performance of this MMIC. Note that the losses of the SMA connector and the 50Ω line on the fixture are included.

could be fixed by using an isolator in the system. For power measurement, this chip was mounted on a test fixture with 50Ω lines and SMA connectors. Figure 4 shows the power response curve at 15GHz. Note that this result includes the losses of 50Ω line and the SMA connector, which is estimated to be between 0.25dB to 0.5dB. It is clear that this circuit meets the requirements of 20dB gain and 26dBm P_{sat}. Another important specification is the output power dynamic range. In this test, the input power is set to be 5dBm, which will be the power level in the actual system. The output power is then varied by changing bias voltage. It is extremely important that there is no oscillation occurred while varying the output power. Figure 5 shows the gain variation of this MMIC by adjusting the drain voltages from 5V to 0V. It can be seen that the dynamic range of more than 40dB is achieved with relatively flat response and there is no oscillation observed during the measurement. In addition, The same test was also performed at different temperatures, from –20°C to 70°C, to emulate outdoor environments, and similar results have been obtained.

IV. Conclusions

In conclusion, a broadband, dual-function power amplifier MMIC has been developed for microwave digital link applications. This power amplifier achieves 20dB gain and 26dBm P_{sat} from 12GHz to 16GHz with output power dynamic range of 40dB from –20°C to 70°C. This circuit is suitable to replace the discrete power amplifier and the mechanical attenuator in the current system, which will reduce the cost and size of the RF front-end significantly.

V. References

[1] J.L. Langstin, “Local Multipoint Distribution Services (LMDS) System Concepts and Implementation,” *IEEE MTT-S Topical Symposium on Technologies for Wireless Applications Digest*, pp. 12-15, Feb. 1997.

[2] Siddiqui MK, Sharma AK, Callejo LG, and Lai R, “A high-power and high-efficiency monolithic power amplifier at 28 GHz for LMDS applications,” *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 2226-2232, Dec. 1998.

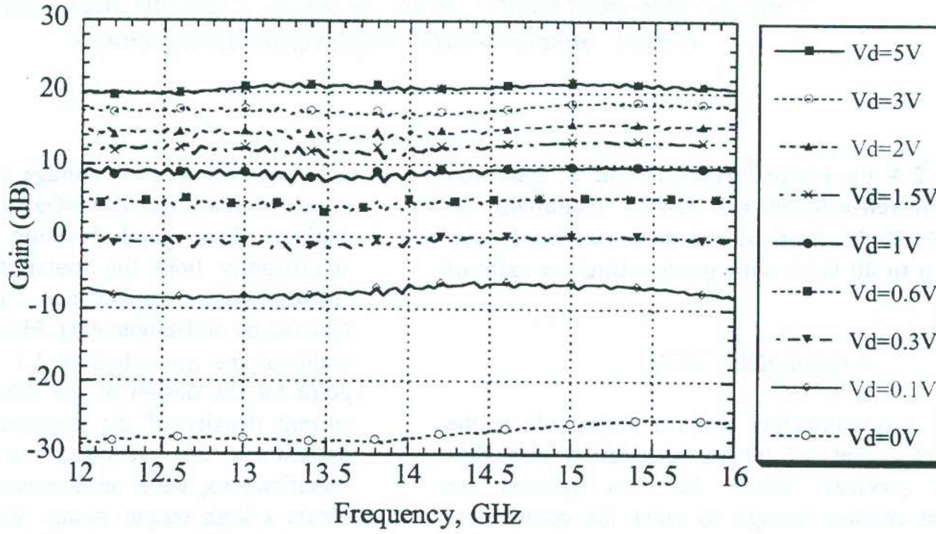

Figure 5: Gain variation of the amplifier by adjusting drain voltage with input power of 5dBm.