RF TRANSMISSION LINES ON SILICON SUBSTRATES

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***Abstract*- A review of RF transmission lines on silicon substrates is presented. Through measurements and calculated results, it is shown that attenuation is dominated by conductor loss if silicon substrates with a resistivity greater than 2500 Ω-cm are used. Si passivation layers affect the transmission line attenuation; however, measured results demonstrate that passivation layers do not necessarily increase attenuation. If standard, low resistivity Si wafers must be used, alternative transmission lines such as thin film microstrip and CPW on thick polyimide layers must be used. Measured results presented here show that low loss per unit length is achievable with these transmission lines.**

I. INTRODUCTION

The market for mobile voice and pager communication systems, especially at 2 GHz, has grown tremendously over the past several years. Now, demand is growing for higher frequency systems at 20 and 30 GHz for high data rate video and digital communications. Since these are commercial markets, it is imperative that system designers achieve the required performance at the lowest cost.

For the RF circuit designer, there are several methods that can be used to lower the cost. First, the Radio Frequency Integrated Circuits (RFICs) or Monolithic Microwave Integrated Circuits (MMICs) that perform RF amplification and frequency translation may be made using the lowest cost technology. Second, more functions can be incorporated onto a single circuit to minimize interconnect and wire bonding expenses while improving reliability. Third, thermal management and wafer breakage expenses can be reduced.

To meet these challenges, Si RFICs have emerged as a strong challenger to the traditional GaAs MMIC [1-5]. This has been made possible by the development of SiGe heterojunction bipolar transistors (HBTs) by IBM [5] and DaimlerChrysler [6]. In fact, by using aggressive bandgap engineering, HBTs with a maximum frequency of oscillation, f_{max}, of 160 GHz have been demonstrated. While commercial circuits based on this HBT are not available; Si RFICs operating into the millimeter-wave spectrum are currently available. Since Si wafers cost less than GaAs wafers and there is a larger worldwide Si processing infrastructure, it may be expected that Si RFICs will cost less than GaAs MMICs will. Because these circuits may be monolithically integrated with BJT and CMOS data processing and memory circuits, it is possible to build single chip communication systems. Furthermore, since sensors and MEMs devices are usually built on Si substrates, single chip systems are possible. Thus, the packaging and interconnect costs are significantly lowered.

However, the development of millimeter-wave HBTs only solves half of the problem with Si as a microwave substrate. Unlike digital ICs, interconnects in RFICs are required for impedance matching, filtering, and signal distribution. In fact, most of the circuit area in RFICs is comprised of transmission lines. Microwave transmission lines are characterized by their propagation constant $\gamma=\alpha+j\beta$ where β is the phase constant and α is the attenuation constant. Attenuation may be separated into the attenuation due to losses in the dielectric, α_d, and the conductor, α_c. While α_c is primarily dependent on the conductivity and geometry of the metal lines, α_d is primarily dependent on the substrate and determined by [7]:

$$\alpha_d = \frac{\pi}{\lambda_0}\frac{\varepsilon_r}{\varepsilon_r - 1}\frac{\varepsilon_{eff}(f)-1}{\sqrt{\varepsilon_{eff}(f)}}\tan\delta \quad \text{(Np/cm)} \qquad (1)$$

where ε_r is the relative dielectric constant (ε_r=11.68 for Si [8]), λ_0 is the free space wavelength, and ε_{eff} (f) is the effective permittivity of the transmission line. The loss tangent,

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} + \frac{1}{\omega\varepsilon'\rho} \qquad (2)$$

is dependent on the complex permittivity, $\varepsilon=\varepsilon'-j\varepsilon''$ (where $\varepsilon''/\varepsilon'$=0.0018 for Si [8]), and the resistivity of the substrate, ρ.

After inserting the associated values for Si into Equ. 1, the dielectric attenuation is given by:

$$\alpha_d = \frac{\varepsilon_{eff}(f)-1}{\sqrt{\varepsilon_{eff}(f)}}\left\{1.7905\cdot 10^{-3} f + \frac{153.09}{\rho}\right\} \text{(dB/cm)} \qquad (3)$$

where f is the frequency in GHz and ρ is in Ω-cm. Ideally, ρ is infinite and α_d is only dependent on losses associated with the polarization of the atoms in the material. In practice, the second term may be neglected if $\rho > 8.55*10^5/f$. Traditionally, digital Si ICs are fabricated on wafers with a bulk substrate resistivity of 1 to 10 Ω-cm. Thus, the second term dominates and $\alpha_d \cong 32$ dB/cm over the entire microwave and millimeter-wave frequency spectrum for microstrip and coplanar waveguide (CPW) as shown in Fig. 1. Obviously, this is a prohibitively high attenuation. Even if Si substrates with a resistivity of 10000 Ω-cm, which is the highest resistivity wafers commonly available, are used, the second term dominates α_d through 50 GHz; however, the dielectric loss is less than 0.1 dB/cm at 1 GHz for microstrip lines on 10000 Ω-cm Si which is a very acceptable attenuation.

While it may seem obvious to use Si wafers with the highest resistivity available and ignore the dielectric losses, this decision is not always up to the circuit designer. The two foundries offering SiGe HBT processing, IBM in the US and Temic Semiconductor in

Germany, use CMOS grade Si. Therefore, RF circuit designers must be able to layout circuits on either type of substrate. In the rest of this paper, low loss transmission lines on both types of Si wafer will be presented.

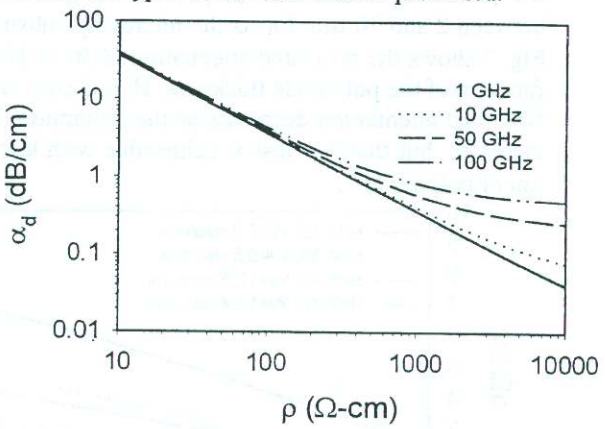

Fig. 1: Calculated dielectric attenuation of 50 Ω microstrip line on 100 μm thick Si and a line width of 80 μm.

II. TRANSMISSION LINES ON HIGH RESISTIVITY SILICON

While Equ. 3 clearly shows that dielectric attenuation decreases as the substrate resistivity increases, it is reasonable to ask how high the resistivity should be before the incremental benefit of lower α_d is too small to affect circuit performance. This question arises because substrate cost increases as the resistivity increases. Fig. 2 shows the calculated conductor and dielectric loss of 50 Ω microstrip lines as a function of the Si resistivity and thickness, and Fig. 3 shows the calculated conductor and dielectric loss of 50 Ω CPW lines as a function of the CPW geometry and Si resistivity. As shown in Fig. 2, the dielectric attenuation for microstrip lines may not be neglected even when the resistivity is 10000 Ω-cm. For CPW lines of the commonly used center strip and slot widths, S and W respectively, a resistivity of 2000 Ω-cm is required for $\alpha_c > 10\alpha_d$. These results are due to slightly higher α_d for microstrip lines and significantly higher α_c for narrow CPW lines. Fig. 4 shows measured attenuation of narrow and wide CPW lines on 400 and 2500 Ω-cm Si and GaAs. As predicted by Fig. 3, the attenuation of CPW on HRS and GaAs is similar; while on 400 Ω-cm Si, CPW has significantly higher loss. Note that lower conductor loss is achievable with CPW lines by increasing S and W, which would increase the influence of α_d. However, for commonly used CPW and microstrip dimensions, a resistivity of 2500 Ω-cm and 10000 Ω-cm is required respectively if α_d is to be ignored.

Besides low loss, HRS offers another major advantage to Si circuit designers. Most circuit element models developed over the past twenty years are based on measurements and modeling of GaAs circuits. Since ε_r of Si and GaAs differ by only 9 percent, Si circuit designers may use the same models. Fig. 5 shows the measured characteristics of a CPW short circuit terminated series stub on HRS and GaAs. Except for a frequency shift due to the lower dielectric constant of Si, the characteristics are the same. Other components behave similarly.

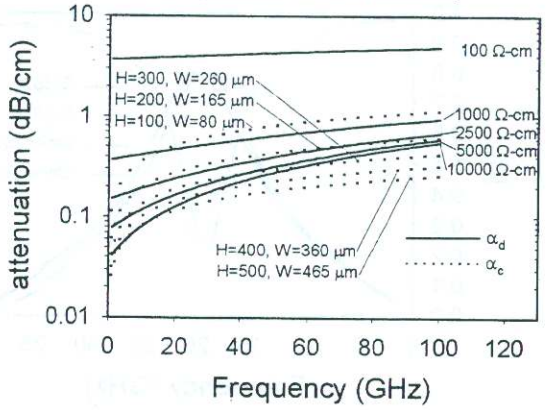

Fig. 2: Calculated attenuation of 50 Ω microstrip line as a function of Si thickness (H), strip width (W), and Si resistivity (metal thickness = 2 μm).

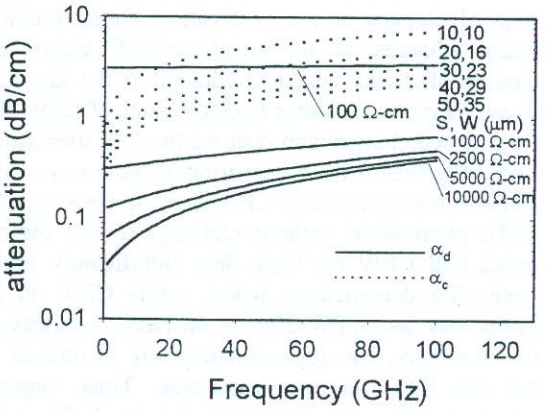

Fig. 3: Calculated attenuation of 50 Ω CPW as a function of strip width (S), slot width (W), and Si resistivity (metal thickness = 2 μm).

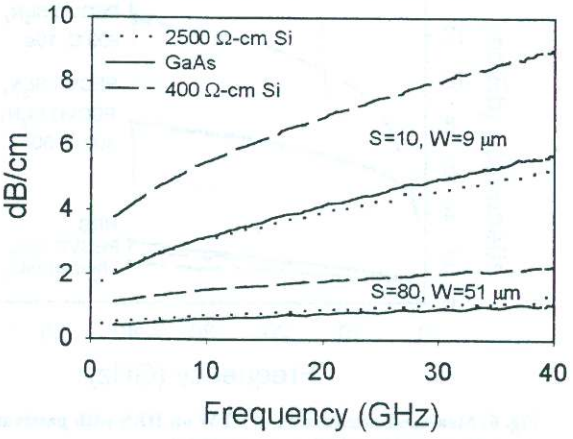

Fig. 4: Measured attenuation of CPW on Si and GaAs as a function of frequency and line geometry, metal thickness =1.5 μm.

There are potential difficulties with HRS though. CPW placed directly on HRS, as was done for Figs. 4 and 5, has bias dependent propagation characteristics, and even worse, leakage current between the center conductor and ground planes is large enough to alter the bias of diodes and other active components [9]. To mitigate this problem, HRS must be passivated with SiO_2 or Si_3N_4. However, several authors have noted a substantial increase in attenuation when a passivation layer is used and have

recommended removing the insulator from the exposed surface: only leave the insulator under the metal lines [10].

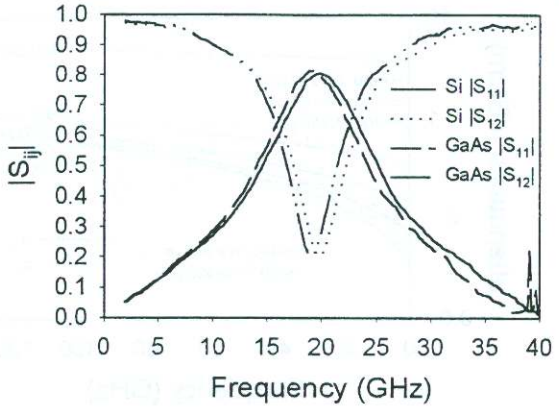

Fig. 5: Measured CPW short circuit series stub on GaAs and HRS, S=W=50 μm.

The increased attenuation is believed to be due to trapped charges in the passivation material that induces image charges at the insulator/HRS interface. These charges short the center conductor to the ground planes. Removal of the insulator from the slots of CPW eliminates the induced charges and restores the low attenuation of the line. However, this observation is not universal. Fig. 6 shows the attenuation of CPW lines on HRS with SiO_2 and Si_3N_4 passivation without etching the slot regions. It is noted that CPW on Si_3N_4 has significantly higher loss, even after densification bakes, while CPW on SiO_2 has lower loss than CPW directly on HRS. Analysis indicates that the Si_3N_4 has approximately 2% Si ions in the film, but the SiO_2 has no impurities. Thus, impurity free passivation layers eliminates the need for passivation removal.

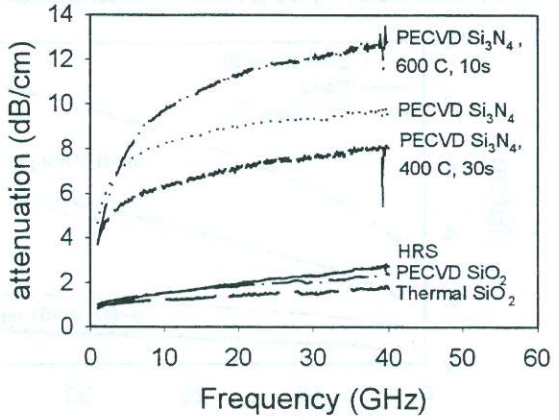

Fig. 6: Measured attenuation of CPW on HRS with passivation layer, S and W equal 50 and 35 μm respectively.

III. TRANSMISSION LINES ON LOW RESISTIVITY SILICON

Because low resistivity Si introduces significant attenuation as shown in Fig. 1, microstrip, CPW, and other transmission lines cannot be placed directly on it. Instead, methods must be used that either shield or minimize the electromagnetic field interaction with the Si. This is usually accomplished by using the polyimide that Si IC manufactures use for wafer planarization.

Thin film microstrip (TFMS) is formed by depositing a metal ground plane on the top surface of the Si, depositing polyimide on top of that, and then the microstrip on top of the polyimide. Thus, the polyimide, which is typically between 2 and 10 μm, forms the microstrip substrate [11]. Fig. 7 shows the measured attenuation of 50 Ω TFMS as a function of the polyimide thickness, H, and strip width, W. Note that attenuation decreases as the polyimide thickness increases, but that low loss is achievable with less than 10 μm of polyimide.

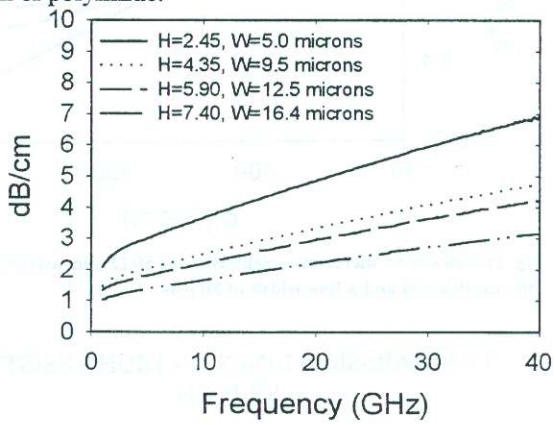

Figure 7: Measured attenuation of 50 Ω TFMS as a function of polyimide thickness.

With CPW, ground planes either above or below the substrate are not desired since they introduce the potential for exciting parasitic microstrip or parallel plate waveguide modes. This possibility increases when the polyimide is less than three times S+2W. Since a very thick polyimide would be required to maintain a good CPW TEM mode, it is not possible to shield the Si from the CPW with a ground plane as was done for the TFMS.

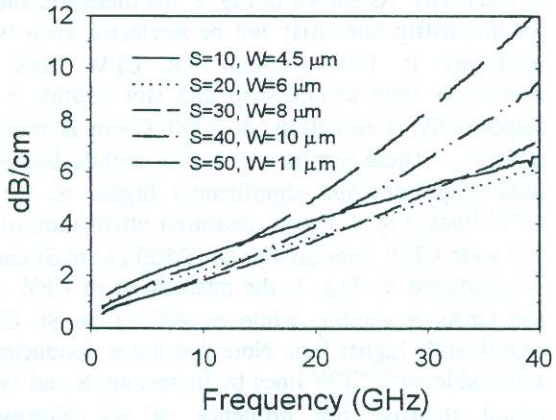

Figure 8: Measured attenuation of CPW lines on 14.59 μm polyimide on 2-10 Ω-cm Si.

Instead, polyimide is used to elevate the CPW above the Si to minimize the field interaction with the Si [12]. Polyimide is deposited directly on the Si wafer and the CPW is then defined on top of the polyimide. Fig. 8 shows the measured attenuation of five CPW lines on 14.59 μm thick polyimide, which is on low resistivity Si. When S+2W is small, the attenuation is conductor loss dominated (varies as $f^{0.5}$); however, the frequency dependence and attenuation increases as S+2W increases. This is the opposite of CPW lines on HRS or other insulators. Furthermore, ε_{eff} and the characteristic

impedance are also dependent on S+2W relative to the polyimide thickness. Thus, while each of the CPW lines in Fig. 8 is 35 Ω on HRS, their impedance varies from 42 to 52 Ω on polyimide.

Micromachining CPW on HRS to remove the substrate from the slots has been shown to reduce attenuation. This may be done with CPW on polyimide also as is shown in Fig. 9. Fig. 10 shows measured loss of micromachined CPW on low resistivity Si. There is a 28 percent reduction in attenuation after etching for the CPW line on thinner polyimide and a 35 percent reduction in attenuation on the thickest polyimide at 40 GHz. Etching the polyimide from the slots also lowers ε_{eff}: ε_{eff} for a CPW line with S and W of 10 and 9 μm respectively and a polyimide thickness of 20.15 μm is only 1.3.

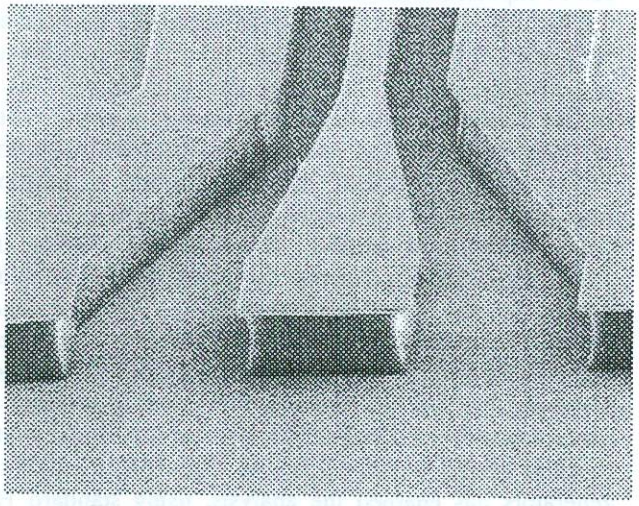

Figure 9: CPW on low resistivity Si with a polyimide interface layer that has been removed from the slots.

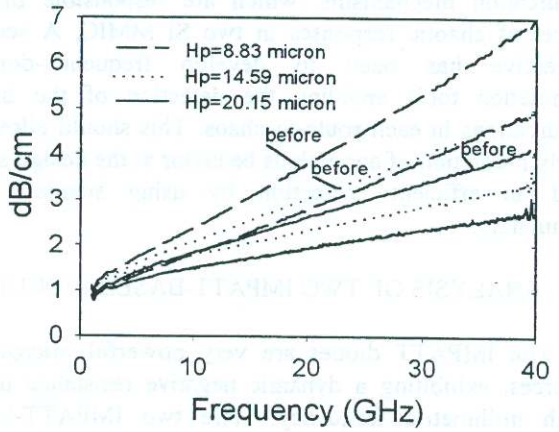

Figure 10: Measured attenuation of CPW lines on polyimide before and after etching polyimide from slots, S=10, W=9 μm.

IV. CONCLUSIONS

A review of transmission lines suitable for Si RFICs has been presented. It has been shown that CPW lines on Si with a resistivity greater than 2500 Ω-cm have approximately the same attenuation as CPW on GaAs. Furthermore, passivation layers on HRS do not necessarily increases attenuation if they are grown with low impurity concentrations. When low resistivity Si must be used, thin film microstrip with a polyimide thickness of only 7.4 μm yields the same attenuation as similarly sized CPW lines on HRS. CPW lines on polyimide have higher attenuation or require thicker polyimide than TFMS, but if the polyimide is etched from the slots, the attenuation is comparable to that of TFMS and CPW on HRS. Transmission lines on polyimide have a significantly lower ε_{eff} than CPW or microstrip on HRS, which increases circuit speed.

V. REFERENCES

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