Can Silicon Catch the Millimeter Wave?

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Abstract — **Transceiver designs implemented in silicon technology are most competitive in design cycle-time and performance versus cost when compared to other technologies. Scaling is driving silicon technology towards gain-bandwidths of 300GHz, enabling circuits operating deep into mm-wave frequency bands (i.e., well above 30 GHz). However, innovations in on-chip passive design and construction currently being pioneered in mixed-signal silicon technologies may be the real technology enablers at these frequencies. Relevant examples are presented from the author's own work and the recent literature.**

Index terms — **millimeter wave, radio frequency, wireless communication transceivers, integrated circuits, silicon technology.**

I. Introduction

Silicon systems on a chip (SoC) or systems-in-a-package (SiP) are supporting the drive towards low-cost portable wireless devices with full multimedia capabilities. Broadband systems are the next logical step in the evolution of wireless networks, and their economic viability depends upon inexpensive SoC/SiP realizations with rapid time to market. This favors silicon technology, provided that reproducible RF performance can be achieved.

While far from being the perfect platform for microwave frequency circuit development, the past 10 years of RF IC evolution has shown that silicon plays a lead role in portable wireless circuits because of its inherent economies of scale. It will continue to dominate RF IC technology in the 1-10GHz range for the foreseeable future.

However, demand for wider bandwidth services will quickly stress the capabilities of today's low-GHz systems, and faster circuit technologies can provide a relatively simple route to the greater bandwidth available in higher frequency bands. Many gigahertz of frequency spectrum for back-haul links, point-to-multipoint distribution, and personal area networking may be opened-up by new circuit developments aimed at the millimeter-wave, or mm-wave band (i.e., $\lambda < 10$mm or $f > 30$GHz in air).

Technology scaling and developments like SOI-CMOS and SiGe-BiCMOS continue to improve device speed, but is this sufficient to address challenges posed by applications beyond 10GHz? Almost all silicon technologies have elements in common, such as a moderate to highly conductive substrate, barriers to transistor scaling on the horizon, and relatively thin planes of wiring used for interconnecting on-chip components. Some of the strengths and weaknesses of the technology for mm-wave circuit development currently faced by designers attempting to extend the reach of circuits towards mm-wave frequencies will be outlined in this paper. Examples are drawn from the author's own work as well as from the recent literature.

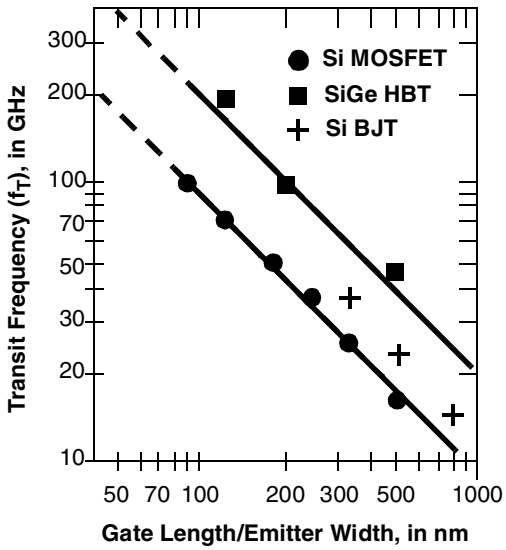

Fig. 1: Transistor f_T in various RF IC technologies.

II. On-chip interconnect - when is a wire is no longer a wire?

The progressive improvement in unity-gain (i.e., f_T) of silicon active devices is predicted to exceed 300GHz in production within a decade, as shown in Fig. 1. Are transistor developments alone sufficient to solve the challenges posed by new wireless applications, such as integration of a 60GHz broadband transceiver?

Unfortunately, improvements in CAD models, interconnect performance, and packaging continue to lag behind scaling. The average interconnect wire length is not shrinking as quickly as transistor dimensions, and above 10GHz "time-of-flight" delays begin to have an important effect on circuit behavior. Wires no longer can be modelled as a simple lumped resistor-capacitor filter, but begin to behave like lossy transmission lines that can impair circuit performance.

For traditional metal-insulator-silicon (MIS) wiring on-chip, the attenuation increases with the square of frequency between 1 and 15GHz (see Fig. 2). The attenuation is lowest for the 20µm line below 1GHz, but rises rapidly and reaches a plateau of 0.2Np/mm or 1.7dB/mm (2 µm thick aluminum) as the frequency increases and more energy is coupled into the substrate. Consequently, the 5µm wide conductor has lower attenuation than either the 10 or 20µm line above about

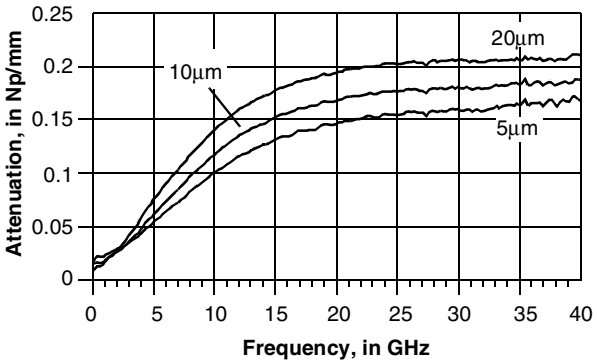

Fig. 2: Measured attenuation constant for MIS lines.

3.5 GHz.

One way of reducing these losses is through shielding. However, simple shielding adds unwanted parasitic capacitance that reduces operating bandwidth. The slow-wave coplanar waveguide (S-CPW, [1]) of Fig. 3 uses substrate shielding to reduce losses, but has little effect on bandwidth (e.g., attenuation is 0.3dB/mm at 30GHz). Floating metal shield strips are placed beneath the top conductors to reduce the electric field entering the silicon substrate as shown in the figure. The strips are designed to minimize their effect on the magnetic field, resulting in a higher characteristic impedance compared to a top-metal/ first-metal (MIM) microstrip line with a solid ground shield. The MIM structure also has low attenuation, but characteristic impedance on-chip is restricted to less than 100Ohms for topmetal trace widths greater than approximately 8µm. The S-CPW configuration allows the magnetic field to fill a larger volume, and therefore the designer can use a wider topmetal trace to realize very low attenuation per mm of length if desired (as seen in Fig. 3). The transmission line Q-factor is improved by 2x over most of the frequency range for the S-CPW compared to the MIM test lines well into the mm-wave range [1]. This improvement in Q arises from the combination of lower attenuation and wavelength reduction (i.e., > phase shift/unit length) with S-CPW.

Monolithic inductors and transformers designed from transmission lines and fabricated on silicon perform best in balanced circuits, because the substrate parasitics have less effect on the self-resonant frequency and Q-factor. A differential substrate shield for an inductor [2] uses a mesh of shielding strips that span the inductor dimensions. Voltage induced onto a shield strip along one side of the coil, is compensated by an equal but opposite voltage induced at the other end when the inductor is driven differentially. The net electric potential induced on the shielding strips is therefore zero, so an explicit ground connection is not required. Induced current is inhibited by placing the first and second metal shielding strips orthogonal to the topmetal inductor winding.

Measured Q-factors for shielded and unshielded symmetric inductors are compared in Fig. 4. The inductance is ~7.4nH. Differential shielding lower the self-resonant frequency by < 3%, and there is < 2%

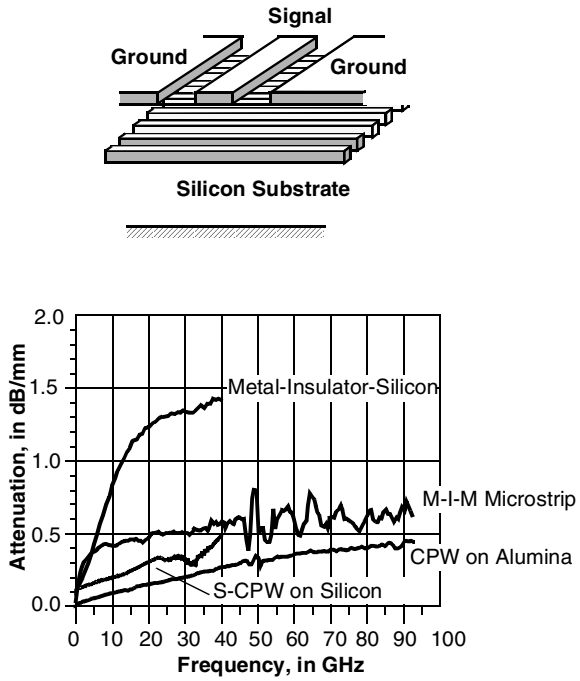

Fig. 3: Structure of shielded CPW (S-CPW) and measured attenuation constants for various transmission lines.

change in inductance between shielded and unshielded inductors, so current induced in the shielding strips is small. Thus, a differential shield does not diminish the useful frequency range or inductance, and improves the Q-factor by 35%.

On-chip transformers (like inductors) rely upon mutual magnetic coupling, but between two or more windings. Each transformer winding (ideally) has negligible dc voltage drop, which enables low voltage circuits as supply headroom is preserved. The losses in an on-chip transformer also benefit from the shielding techniques demonstrated for inductors.

Transformer-coupling between RF stages is used to implement the Hartley image-reject front-end shown in Fig. 5. This eliminates a passive (off-chip) filter connected between the preamplifier (LNA) and the mixer needed to reject spurious signals at the "image" of the desired signal band in a heterodyne radio, or in a

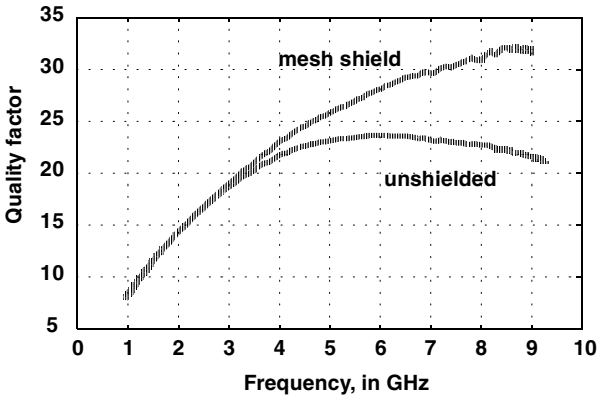

Fig. 4: Q-factor comparison of inductors on silicon.

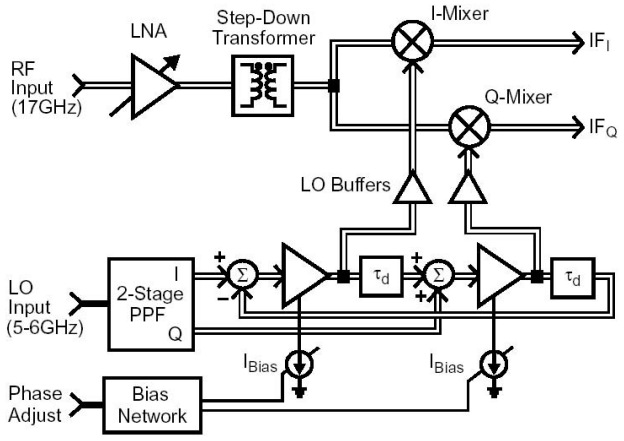

Fig. 5: Transformer-coupled RF receiver front-end.

homodyne (direct conversion) receiver.

The 17GHz image-reject receiver test IC includes a low-noise amplifier (LNA) and 2 mixers coupled by the step-down transformer [3]. A quadrature local oscillator (LO) generator allows the image rejection of the downconverter to be optimized by adjusting the phase of the LOs generated by a subharmonically injection-locked oscillator incorporating on-chip passive delay lines. Over 75dB of image-rejection at 70MHz IF was demonstrated in a production 100GHz-f_T SiGe-BiCMOS technology. The testchip (see Fig. 6) consumes a total of 62.5mW from a 2.2V supply.

A step-down transformer with tight magnetic coupling was developed for a 17GHz integrated downconverter. The primary winding is symmetric for use in a fully-differential circuit. The secondary winding is also symmetric, but each turn is equal in (unwound) length. All 3 turns are then connected in parallel to realize a step-down transformation. This results in balanced inductance and resistance among all turns and an accompanying increase in primary to secondary coupling (k_m=0.78). The electrical turns-ratio is 1:0.27 or 3.71:1.

Broadband wireless networks in the 24GHz ISM band will reduce congestion in lower frequency bands and supports data services up to hundreds of Mb/s, enabling 4G wireless access and connectivity. A linear integrated 21-26GHz power amplifier (PA) with 125mW (+21dBm)

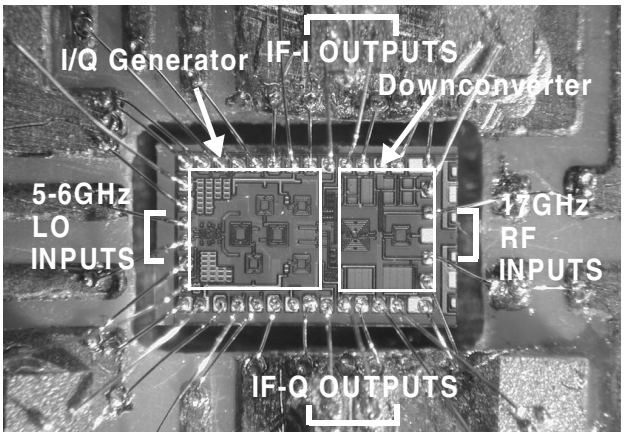

Fig. 6: 17GHz image-reject receiver testchip (0.18µm SiGe).

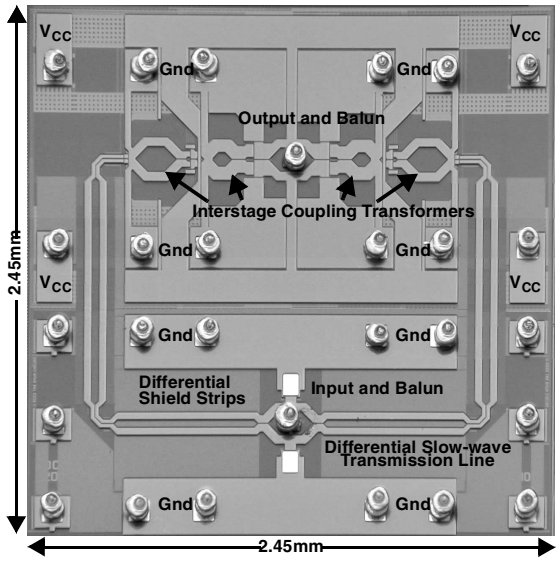

Fig. 7: SiGe 21-26GHz power amplifier chip micrograph.

output power using 1.8V breakdown (V_{CEO}), 100GHz f_T SiGe bipolar transistors is described in [4]. Interstage step-down transformers and on-chip input/output baluns optimize the gain in each stage and preserve signal swing, with minimal energy loss to the medium resistivity (10-15Ω-cm) substrate. A chip micrograph is shown in Fig. 7.

Three stages of amplification (approximately 6dB small-signal gain/stage) provide 15dB gain at 1dB gain compression per stage (i.e., large signal). The amplifier produces full power with a 6dBm RF input. An interstage step-down transformer (2:1 as drawn turns ratio) is used to maximize power transfer. The low-voltage secondary coil (emitter side) of the coupling transformer forms a self-shielding structure around the higher-voltage primary coil (collector side) to minimize substrate loss and skin effect (see Fig. 8).

The input and output baluns are identical. At the input, a shielded differential transmission line connects the input balun to the first gain stage. As the output balun must handle up to 400mA, multiple metal layers are used with an effective width of 90µm and 5µm thickness. A plot of the measured and simulated responses of the power combining (i.e., output) balun is shown in Fig. 9, where excellent agreement is seen [5]. A back-to-back test simplifies characterization of the balun, as the

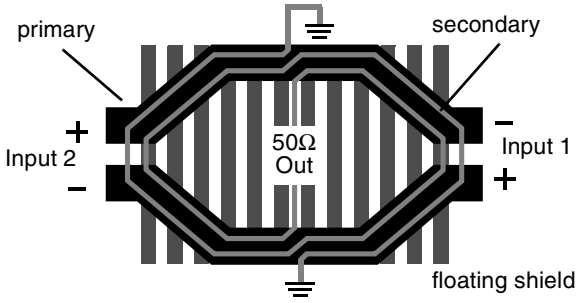

Fig. 8: Self-shielded balun with 2 diff. inputs and 50Ω output.

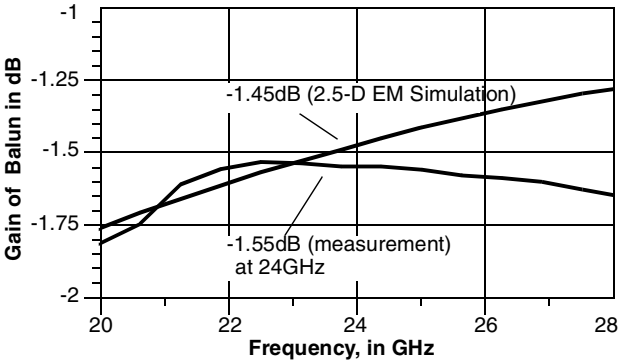

Fig. 9: Measured and simulated response of the 4:1 balun.

measurement equipment is single-ended. The loss of a single balun is one-half of the measured value from a back-to-back test from Fig. 9 (i.e., 3.1dB/2, or 1.55dB at 24GHz).

The measured performance of the 0.2µm SiGe PA is competitive with other technologies (e.g., GaAs pHEMT). Maximum power-added efficiency (PAE) is 19.7% at 22GHz, while PAE at 24GHz is 13%. Peak output power of 23dBm is achieved at 22GHz, and over 20.8dBm output power is available between 20 and 25GHz.

These circuits demonstrate that operation into the mm-wave range of frequencies is possible through passive-active co-design, where on-chip passives optimized for minimum losses are designed in conjunction with the active circuits. This approach realizes high efficiency (e.g., low power consumption or high PAE) while preserving competitive RF performance in a production technology.

III. Applications at 60GHz and Beyond

Many GHz of frequency spectrum for collision avoidance radar (first at 24GHz, migrating to 77/79GHz), and wireless personal networking at 60GHz (59-62GHz in Europe, U.S. and Japan) could be unlocked by new mm-wave circuit developments.

Table 1: Summary of recently reported results at 60GHz.

RF, GHz	Gain, dB	NF, dB	IIP_3, dBm	P_D, mW	Notes
61.5	17	4.2	-8.5	10.8	LNA [6]
60	12	8.8	0*	54	LNA [7]
62	9	13	-	19.2	Mix. [8]
61.5	18.6	13.3	-7	149	Rx F.E. [6]

* inferred from P-1dB measurement.

A brief summary of results reported in the recent literature for basic 60GHz-band receiver building blocks are summarized in Table 1. The first and last 2 entries in the table are an LNA, single-balanced mixer, and a complete downconverter (LNA, quadrature mixers and 3x LO multiplier) designed in 0.13 µm SiGe-BiCMOS technology. The reported power consumption for the downconverter excludes the output buffers used for testing and characterization, which may not be used in a more integrated receiver design. The second entry is for a 0.13µm CMOS LNA. Power consumed by the CMOS LNA is relatively high compared to its SiGe counterpart, but it can benefit from technology scaling in future. While it is clear that this area is still in its infancy, the results are encouraging further development. The relatively low power consumption and high level of integration demonstrated by the SiGe test circuits, for example, is useful for emerging wireless personal-area networking applications. However, other problems such as packaging cost and antenna directivity must be solved before a commercially viable solution is realized.

IV. Conclusions

Successful demonstration of SiGe and CMOS implementations at mm-wave frequencies is opening-up new avenues for product development, such as wireless personal-area networking. Recent development of 100-200 GHz technologies bring high-performance mm-wave applications within reach, but improved passive component designs, device models and circuit design techniques are still needed before commercial exploitation is possible.

Acknowledgements

The author would like to acknowledge the contributions of former graduate students and co-workers. Thanks to David Harame of IBM Microelectronics, Burlington VT, for fabrication support. Technical support for packaging and testing was provided by Wil Straver and Ruud Klerks at TU Delft.

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