CMOS devices and circuits for microwave and millimetre wave applications

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***Abstract* — We present several building blocks for RF front ends at micro and mm-wave frequencies using 90 nm CMOS. The designs are 20 GHz single- and 40 GHz double stage amplifiers with 5.6 and 7.3 dB gain respectively, a 20 GHz resistive mixer with CL = 7.9 dB and IIP3 = 17.5 dBm plus frequency doublers to 40 and 60 GHz with CL = 15.8 and 15.3 dB respectively. All circuits have been designed using distributed elements. Both using a 5 metal layer BEOL process and a 3 metal layer BEOL with post processing.**

I. Introduction

With the downscaling of CMOS very high transit frequencies with f_{max} exceeding 200 GHz have been achieved. This facilitates the implementation of micro and millimeter wave circuits in an advanced CMOS process. Several example of this can be found in [1-4]. This makes CMOS a realistic competitor to III-V materials like GaAs pHEMT for some applications.

In this paper we present several building blocks for an RF front end to study the possibility of integrating micro and millimeter receivers in CMOS. The presented designs are 20 and 40 GHz amplifiers, a 20 GHz resistive mixer as well as 40 and 60 GHz frequency doublers.

II. Technology

A. The 90 nm RF CMOS, front end

The circuits have been fabricated in IMEC's 90 nm RF CMOS process on p-type 20 Ωcm Si substrate. The devices have an f_{max} above 200 GHz and f_T of 170 GHz. Minimum physical gate lengths is 70 nm with an effective oxide thickness of 1.5 nm.

The transistor models used have been developed in-house, both a small signal model with HF noise included [5] used for the amplifier and a large signal model [6] used for the frequency doubler and mixer but also later verified against the amplifier.

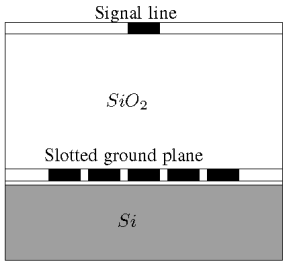
B. Passives, the back end

Two process flows have been used. The first was a standard 5 metal layer BEOL in which the amplifier and frequency doubler have been implemented. The second flow consists of 3 metal layers BEOL with two post-processed thick metal layers with BCB [7].

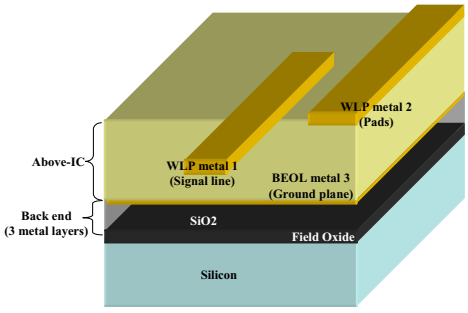
In both process flows high quality MIM capacitors with a capacitance of 1 fF/μm^2 were available in the back end part. These have been modeled in-house using 3D EM simulations. Also multilayer capacitances, there the capacitance between the metal layers are used, have been designed, modeled and used in the designs.

III. A microwave approach to CMOS design

We have in the designs used a distributed approach with microstrip transmission lines using, in the first process flow, bottom metal 1 of the back end as ground plan, top metal 5 as signal line and the SiO_2 as dielectric, see Fig. 1a. The ground plane is slotted to comply with design rules due to chemical mechanical polishing (CMP). This structure was also modeled using 3D EM simulation. In the second process flow with above-IC processing we have used the top BEOL metal (3) as ground plane and the first post processed metal layer as signal line, see Fig. 1b.



(a)



(b)

Fig. 1. Cross-section of the microstrip transmission lines, a) 5 metal layer BEOL and b) 3 metal layer BEOL and above-IC post processing.

These approaches have been successfully verified both on test structure in a TRL calibration kit and in the various circuits.

IV. 20 AND 35 GHZ AMPLIFIERS

Two amplifiers, one single stage at 20 GHz and one double stage at 35 GHz, with distributed matching networks have been designed using the 5 metal layer back end process. The matching networks consist of a transmission line and a shorted stub. The shorted stub also allows for easy biasing. See Fig. 2 for the schematic. The lines have also been meandered to reduce the chip size, see the chip photo in Fig. 3.

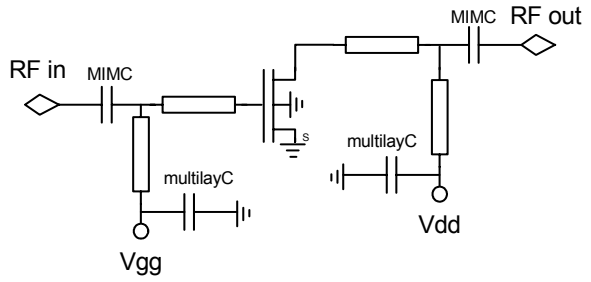


Fig. 2. Schematic of the amplifier.

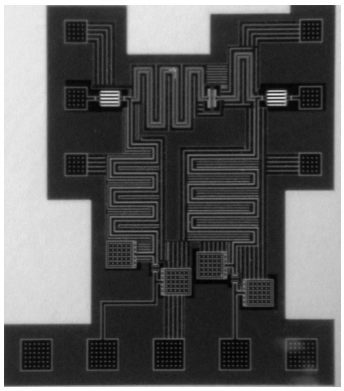


Fig. 3.Chip photo of the 20 GHz amplifier, 0.7 x 0.8 mm in size.

A. 20 GHz single stage amplifier

The gain is 5.6 dB with a return loss better than 10 dB with V_{gs}= 0.65 V and V_{dd} =1.5 V. The matching network was somewhat shifted in frequency. This is believed to be due to the meandering and coupling between adjacent meanders.

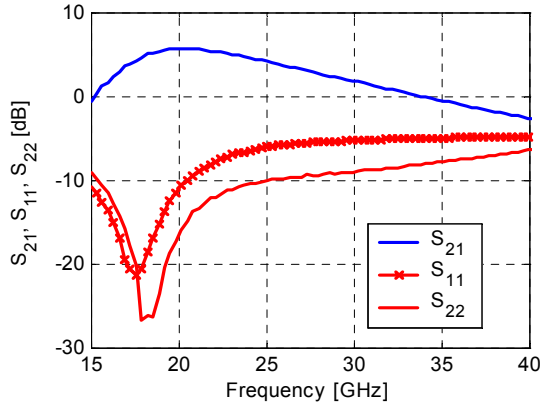


Fig. 4. Gain and return loss of the 20 GHz single stage amplifier.

Power consumption was 12 mW and the chip size 0.7 x 0.8 mm.

B. 35 GHz double stage amplifier

This amplifier have a gain maximum of 7.3 dB at 35 GHz with an input return loss better than 10 dB and output return loss better than 5 dB with V_{gs}= 0.35 V and V_{dd} =1.5 V.

Power consumption was 21 mW and the chip size 1 x 0.7 mm.

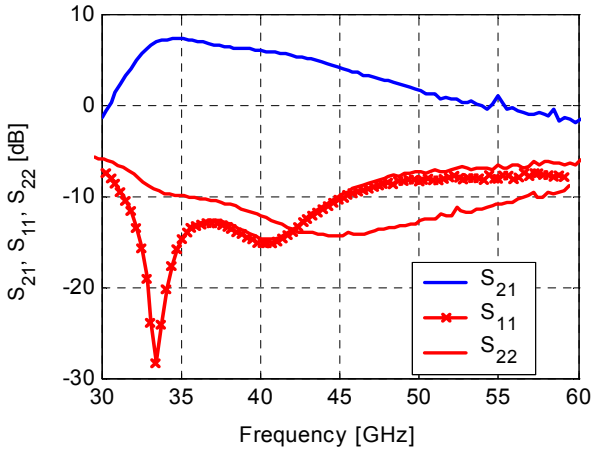


Fig. 5. Gain and return loss of the 35 GHz double stage amplifier.

V. RESISTIVE MIXER

A single ended resistive mixer was designed for a LO of 20 GHz, see Fig. 6 for schematic. The 3 metal layer back end with above-IC post processing was used. We have used a transmission line and a shorted stub for the LO matching network to the gate. The shorted stub also allows for easy gate bias. RF is then applied to the drain through a coupled line filter. The IF is extracted from the drain through lumped low pass filter. The drain can also be biased at the IF port.

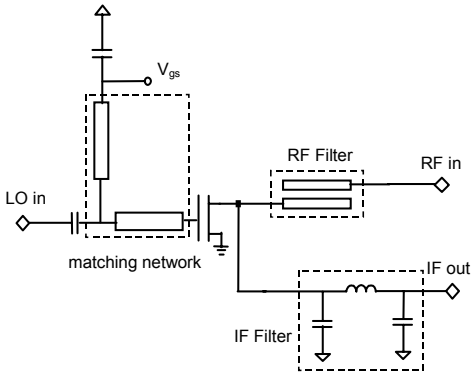


Fig. 6. Topology of the resistive mixer.

The mixer exhibits a 7.9 dB minimum conversion loss at 4 dBm LO power and V_{gs}= 0.5 V, V_{dd} =0 V. The 1 dB bandwidth is 18 to 23 GHz for the RF and 1 to 5 GHz for the IF.

The LO to RF isolation is better than 18 dB over the entire bandwidth and the 1 dB compression point 3 dBm. IIP3 was 17.5 dBm at 4 dBm LO power. This was, in

agreement with theory of [8], improved to 20 dBm with about 4 dB with a small drain bias.

Power consumption is virtually 0.

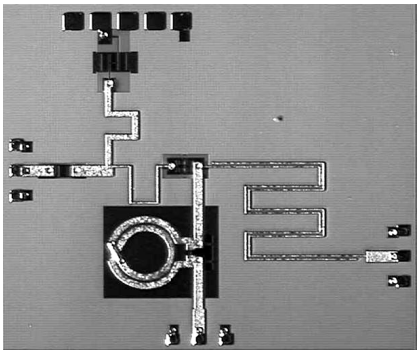


Fig. 7. Chip photo of the 20 GHz resistive mixer, 2.2 x 2.0 mm in size.

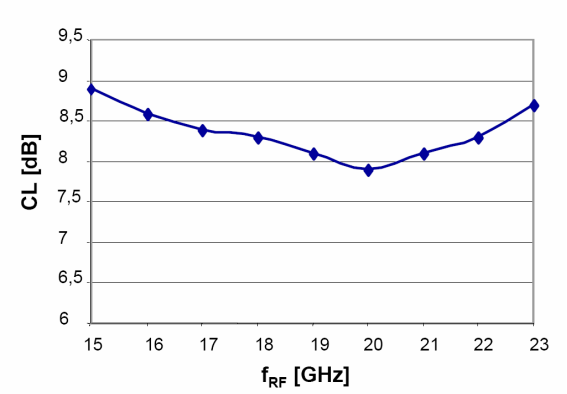


Fig. 8. Conversion loss versus RF frequency, 20 GHz 4 dBm LO.

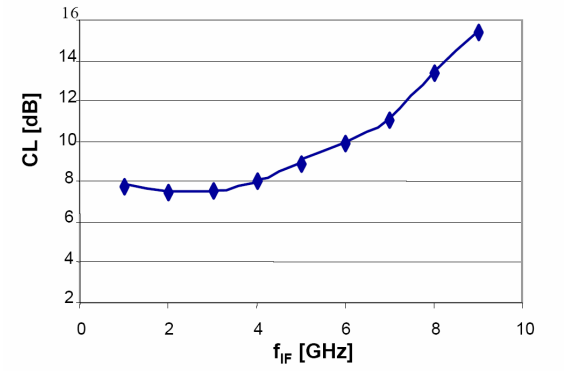


Fig. 9. Conversion loss versus IF frequency. f_{LO} = 20 GHz and P_{LO} = 4 dBm.

VI. Frequency Doublers

Two active frequency doubler, one 20 to 40 GHz and one 30 to 60 GHz, have been designed based on microstrip transmission line matching structures, see schematic in Fig. 10 and Fig. 11 for chip photo. They were realized in the 5 metal layers BEOL process. The task of the output filter was to suppress the fundamental component and match the 2nd harmonic. We used shorted stubs in both the input and output filter in order to facilitate biasing.

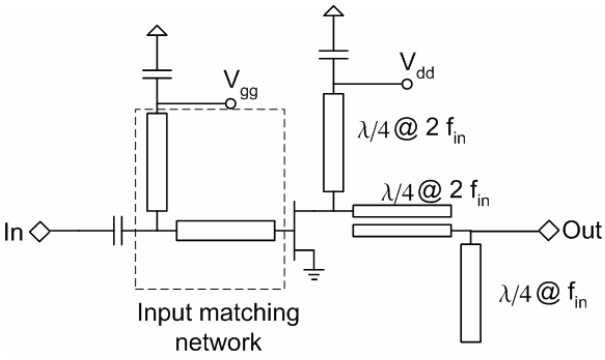


Fig. 10. Schematic of the frequency doubler.

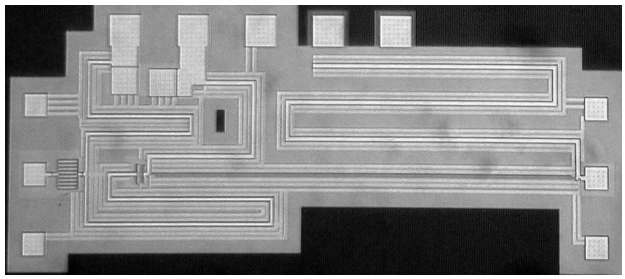


Fig. 11. Chip photo of the 20 to 40 GHz frequency doubler, 1.3 x 0.5 mm in size.

A. 20 to 40 GHz frequency doubler

A conversion loss minimum of 15.8 dB with better than 10 dB suppression of the fundamental was achieved with V_{gs}= 0.35 V, V_{dd} =1.5 V and an input power of 2 dBm, see Fig. 12. Well-positioned minimums was achieved for the input match with 7 dB and for the output better than 10 dB, see Fig. 13.

Power consumption was 4 mW.

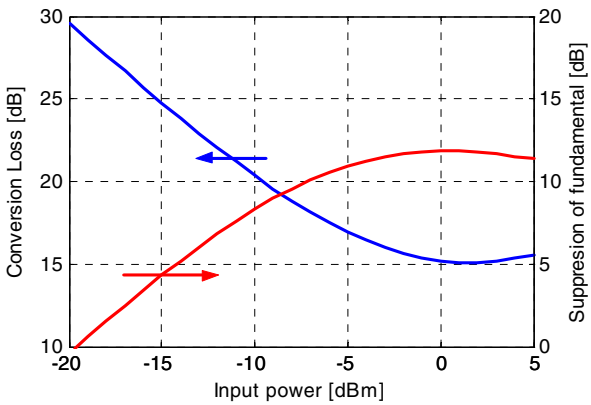


Fig. 12. 20 to 40 GHz frequency doubler: Conversion loss and suppression of fundamental with respect to 2nd harmonic versus input power.

B. 30 to 60 GHz frequency doubler

The 30 to 60 GHz frequency doubler have a conversion loss minimum of 15.3 dB and more than 25 dB suppression of fundamental with V_{gs}= 0.35 V and V_{dd} =1.5 V.

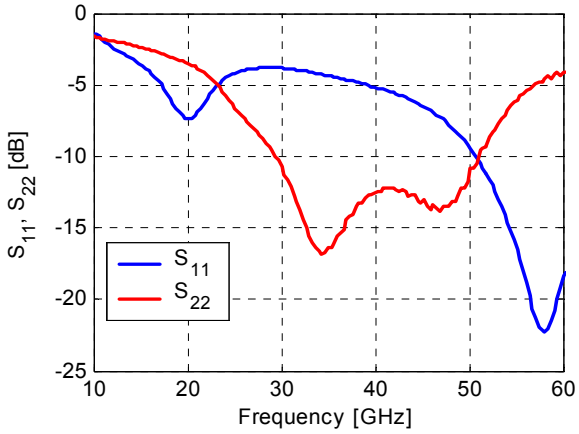


Fig. 13. Input (solid blue) and output (dashed red) matching of the 20 to 40 GHz frequency doubler.

The relatively better performance of this higher frequency doubler is due to the shorter lines and thus lower losses. This since a large part of the losses are ohmic and not frequency dependent, i.e. the frequency dependent losses do not increase with the same rate as the shortening of the lines at higher frequency. For these particular transmission lines and frequency range that is.

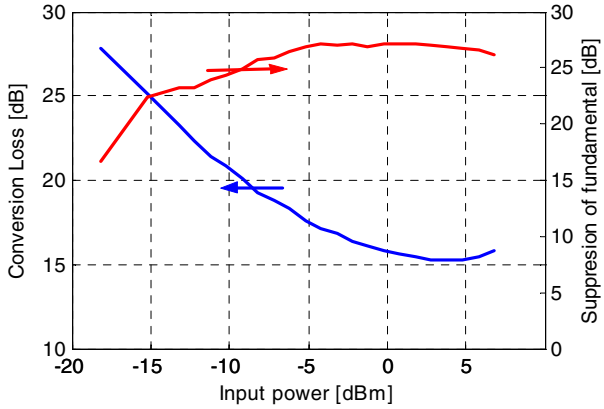


Fig. 14. 30 to 60 GHz frequency doubler: Conversion loss and suppression of fundamental with respect to 2nd harmonic versus input power.

Circuit	Description	FoMs
Amplifiers	20 GHz single stage	Gain = 5.6 dB S_{11}, S_{22} > 10 dB
	40 GHz double stage	Gain = 7.3 dB S_{11}, S_{22} > 10 dB
Mixer	20 GHz resistive mixer	CL = 7.9 dB IIP3 = 17.5 dBm
Frequency doublers	20 to 40 GHz	CL = 15.8 dB S_{11}>5dB,S_{22}>10 dB
	30 to 60 GHz	CL = 15.3 dB S_{11}, S_{22} > 10 dB

TABLE I
SUMMARY OF CIRCUITS AND THEIR FIGURE OF MERITS

This also shows that the bottle neck is really the back end with the passives and not the front end with the transistors.

The chip size was 1 x 0.5 mm and power consumption 4 mW.

VII. CONCLUSION

Amplifiers, Mixer and frequency doublers a RF front end in the 20 to 60 GHz range have been described. All have been designed using a microwave engineering approach with distributed elements for the RF parts.

See table 1 for a summary of the circuit performance.

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