# ESD Characteristics of GaAs versus Silicon Diode

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*Abstract* — **The ESD characteristics of GaAs diode are compared with those of Silicon diode. The ESD diodes are designed and implemented using GaAs HBT technology and 0.25 um CMOS technology. The differences of ESD characteristics between GaAs diode and Silicon diode are investigated, simulated and measured. Because the thermal characteristics of GaAs are different from those of Silicon, the ESD characteristics of GaAs device are different from those of Silicon device.**

## I. INTRODUCTION

The ESD protection method for RF integrated circuits becomes more important as operation frequencies increase. Especially, the compound semiconductors are used in the circuit with high operation frequency. But there are few works on the ESD device using compound semiconductor technology [1]. Because of the different thermal characteristics between GaAs and Silicon, the ESD characteristics of GaAs device are different from those of Silicon device.

Frequently, to reduce the parasitic capacitance induced by the ESD diode, the stacked diode is used. But, it is well known that ESD survival level of Silicon diode becomes low as the number of stacked diodes is increased. It is induced by the thermal characteristics of Silicon. The thermal characteristics of GaAs are different from Silicon. Therefore the ESD characteristics of stacked GaAs diode may be different from Silicon ESD diode.

To find the difference of the ESD characteristics between GaAs diode and Silicon diode, the device simulator, Silvaco is used. The peak temperatures of Silicon diode and GaAs diode are simulated during ESD event condition. The various ESD diodes using HBT technology and CMOS technology are designed and implemented to compare the ESD characteristics of GaAs diode with those of Silicon diode.

## II. THERMAL CHARACTERISTCS OF GAAS AND SI

The thermal characteristics of semiconductor material are very important parameters to the ESD sensitivity. Generally, because of high melting point and thermal conductivity of Silicon, the ESD device using Silicon process has higher ESD survival level than the ESD device using compound semiconductor technology. The melting point of GaAs and Silicon are 1238°C and 1415°C, respectively. The thermal conductivity is shown in Fig. 1.

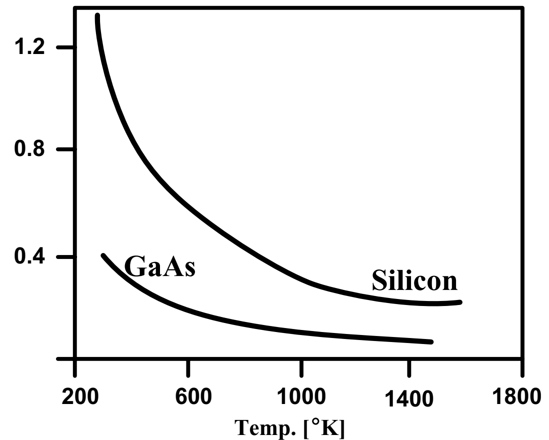



Fig.1.The thermal conductivities of various semiconductor. After [1].

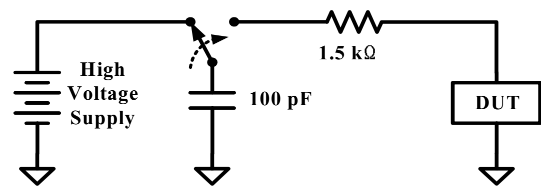



Fig.2. Human Body Model (HBM). [3].

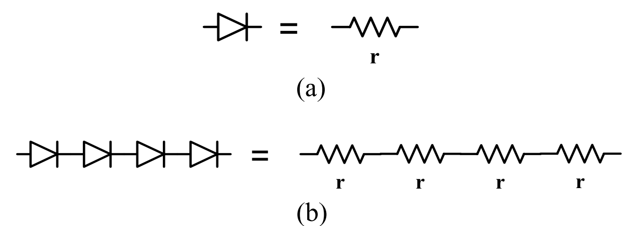



Fig.3.The simplified ESD diode model during ESD event (a) single diode (b) stacked diode.

The heat generated in Silicon ESD device is diffused faster than in GaAs one during the same ESD events. Generally, the heat is generated in pn junction of diode. For GaAs ESD device case, the heat generated in the pn junction may not have influence on the temperature of neighboring device due to its low thermal conductivity. Therefore the ESD survival level of GaAs ESD device can be estimated with Eq. (1) during HBM ESD event [2].

The Fig. 2 shows the Human Body Model of ESD. Where $R$ is the resistance of stacked diode and $r$ is the resistance of each diode of stacked diode. In this calculation, the HBM ESD event is assumed. If the $r$ is assumed to be 3 $\Omega$, the dissipated energies, as shown in Eq. (2) and Eq. (3), in the each diode during HBM ESD event are almost same. This means that the temperature during ESD event in the each diode is almost same. Therefore, the ESD survival levels of various stacked GaAs diodes are almost same.

$$I_{peak} = V_{HBM} /(1500 + R)\Omega$$
$$I(t) = I_{peak} \exp(\frac{-t}{(1500+R)\times 10^{-10}}) \quad (1)$$
$$E = \int_0^{150n\sec} I^2(t)\cdot R dt$$

*Case I : single diode*

$$Energy = V_{HBM}^2 \times 6.3\times 10^{-14} J \quad (2)$$

*Case II : four stacked diode*

$$Energy = V_{HBM}^2 \times 6.24\times 10^{-14} J \quad (3)$$

But, because of the higher thermal conductivity of silicon than that of GaAs, the heat generated in the pn junction may increase the temperature of the neighboring diode. Therefore, the ESD survival level becomes low as the number of stacked diodes is increased. The simple calculation as shown in Eq. (1), Eq. (2) and Eq. (3) can not be used for Silicon ESD device.

## III. Device Simulation Result

The thermal characteristics of GaAs diode and Silicon diode are simulated using Silvaco. The Fig. 4 shows the simulated structures of GaAs diode and Silicon diode. The pn-junction area of GaAs diode is the same with Silicon diode.

The current pulse is impressed into the ESD diode, and the peak temperature at the ESD diode is simulated, varying the width and the amplitude of current pulse. The waveform of impressed current pulse is shown in Fig. 5.

The peak temperatures of single diode and stacked diode are simulated. The number of stacked diode is two. In Fig. 6, the contour of equi-temperature is presented. As shown in Fig. 6 (a), the heat generated in first (or second) diode has no influence on the second (or first) diode. Therefore the peak temperatures of single diode and stacked diode are almost same. This means that the ESD survival levels of single and stacked diode are almost same for GaAs diode case.

But for Silicon diode case, the heat generated in some diode may have influence on the other diode of stacked diode as shown in Fig. 6 (b). Therefore the peak temperature of stacked silicon diode is higher than that of single silicon diode as shown in Fig. 8. This means that the ESD survival level of stacked silicon diode is lower than that of single silicon diode.

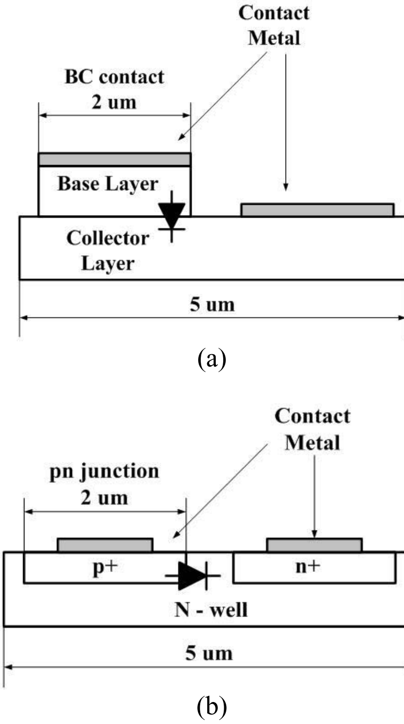



Fig.4.The structures of device simulation (a) GaAs diode (b) Si diode.

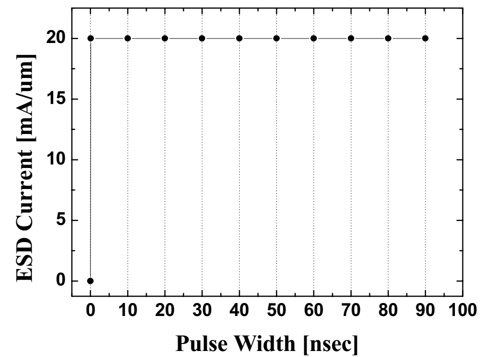
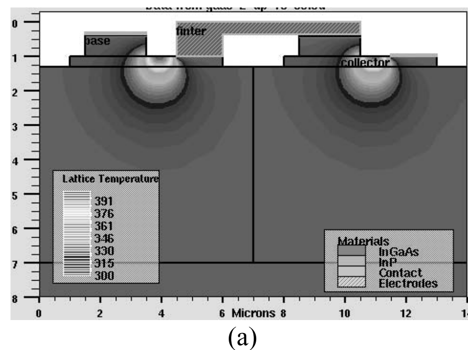
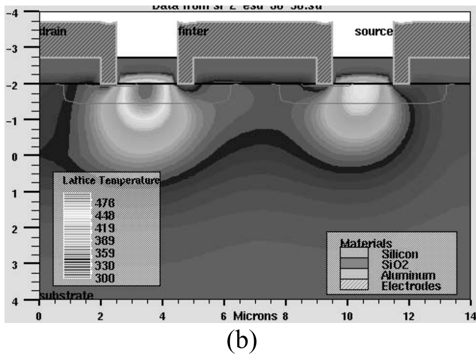



Fig.5. The waveform of impressed current.



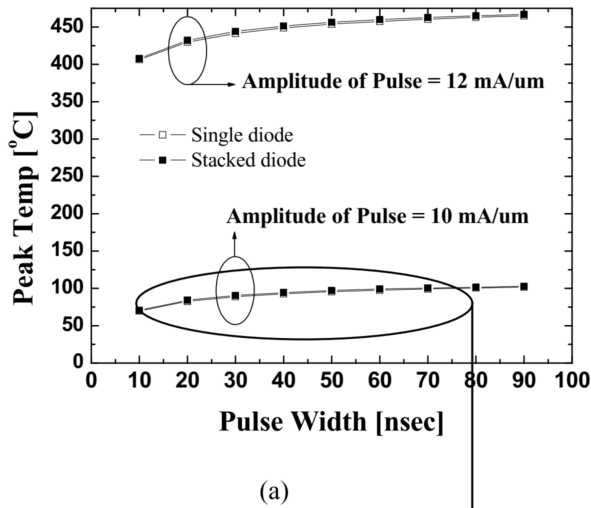

(a)



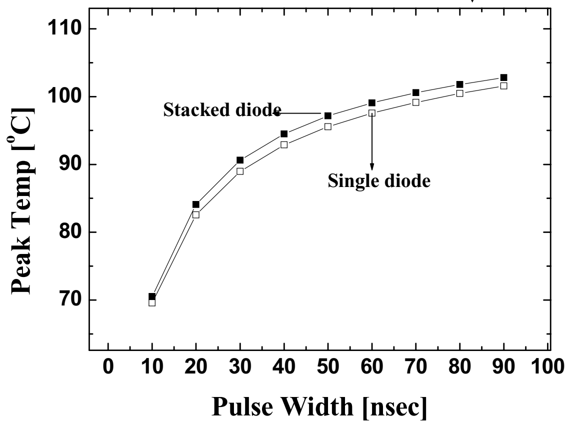

(b)

Fig.6. The temperature distribution of stacked diode (a) GaAs diode (b) Silicon diode.

Fig. 7 shows the simulation results of GaAs diode. The simulated peak temperatures at the GaAs single and two stacked diode are almost same. Therefore, as the results of calculations in the section II, the ESD survival levels of single and two stacked diode must be same. As the width of impressed current pulse is increased, the peak temperature is increased.



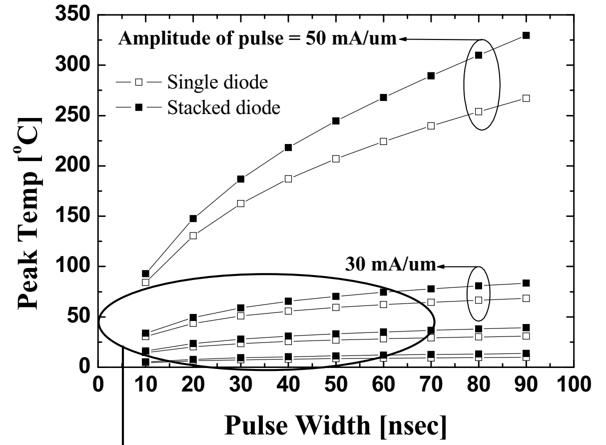

(a)



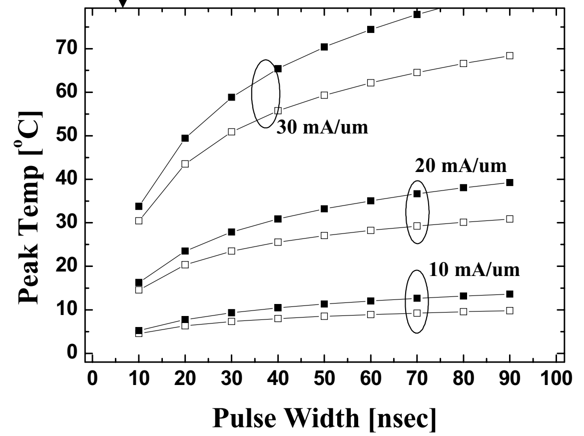

(b)

Fig.7. The simulated peak temperature of GaAs diode.

Fig. 8 shows the simulation results of Silicon diode. For the Silicon diode, the peak temperature of two stacked diode is higher than that of single diode under same impressed current pulse. This means that the ESD survival level of two stacked diode is lower than that of single diode.




(a)




(b)

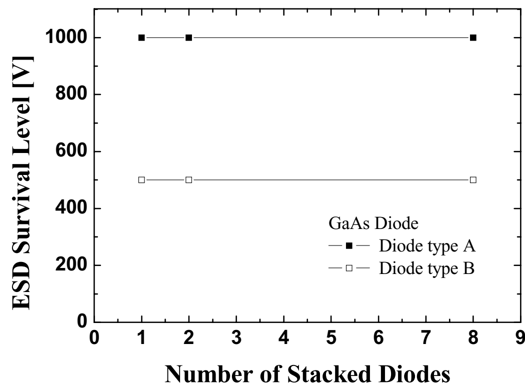
Fig.8. The simulated peak temperature of Silicon diode.

## IV. Measurement Results

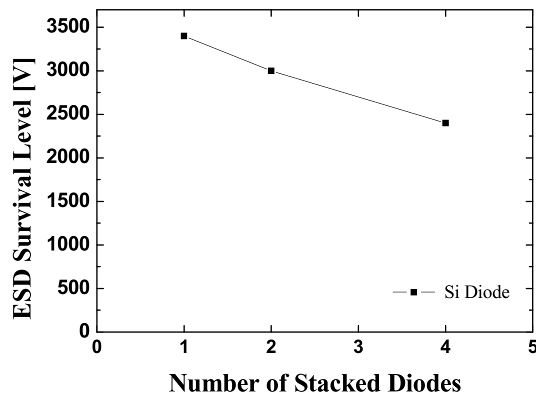
The single and stacked ESD diode using GaAs HBT technology and 0.25um CMOS technology are designed and implemented. The ESD test results of those diodes are shown in Fig. 9. The ESD model for ESD test is IEC61000-4-2 Electrical Model. The ESD is zapped into ESD protection device 10 times at a second interval per given ESD voltage.

As shown in device simulation results, the ESD survival levels of single and stacked diode using GaAs HBT technology is almost same. But in the silicon diode, the ESD survival level of stacked diode is lower than that of single diode.

Generally, to reduce the parasitic capacitance induced by ESD protection diode, the stacked ESD diode is used. For GaAs diode case, the ESD survival levels of single diode and stacked diode are almost same. Therefore, the parasitic capacitance induced by the ESD protection diode can be reduced without sacrificing the ESD survival level of ESD protection diode for the ESD protection diode implemented using GaAs technology. On the other hand, the ESD survival level must be sacrificed to reduce the parasitic capacitance of stacked Silicon diode.




(a)




(b)

Fig.9. ESD test results (a) GaAs diode (b) Silicon diode.

## VI. CONCLUSION

The thermal characteristics of the ESD protection diodes using GaAs HBT technology and CMOS technology are investigated. Using the device simulator, the peak temperatures of various diodes during high current conditions are simulated. Because of the low thermal conductivity of GaAs, the ESD diode can be used as stacked form to reduce the parasitic capacitance induced by the ESD protection elements without sacrificing the ESD survival level.

## ACKNOWLEDGEMENT

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