# PARAMETER EXTRACTION PROCEDURE FOR MICROWAVE AND MILLIMETRE-WAVE MONOLITHIC FET-TYPE DEVICES BASED ON A SCALABLE DISTRIBUTED MODEL

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## ABSTRACT

*A new parameter extraction procedure that uses a FET distributed model in conjunction with a standard optimization routine is presented. The model extraction is carried out by simultaneously fitting the S-parameters of various devices with different gate widths. This procedure has shown to be very robust and yields a very reliable identification of the model elements, both parasitic and intrinsic.*

## INTRODUCTION

Parameter extraction of equivalent circuit based models for microwave and millimetre-wave monolithic FET-type devices has traditionally been a well studied area, especially as far as lumped element equivalent circuits are concerned, and various approaches have been proposed over the years regarding the extraction of parasitic elements [1-2]. However, there are still several shortcomings which constitute an important source of errors in MMIC designs. The cause for these errors lies not only in the parameter extraction technique, but also in using an inappropriate model which does not take into account all the effects present in the device [3,4].

It has been shown in previous works [3-5] that the three-dimensional nature of the device cannot be ignored, and transverse propagation phenomena must be taken into account by using a distributed model, especially if the device is going to be employed at high frequencies. In addition, if the model is to be useful for monolithic circuit applications, it is quite desirable for it to have proper scaling features which offer the designer the ability to predict the performance of devices with different gate width dimensions without repeating the measurement. Lumped element models have shown to be inappropriate when scalability is required [5], so distributed models arise as the best choice to develop a scalable tool suitable for the design of monolithic circuits.

In this contribution a new parameter extraction procedure based on a scalable distributed model for monolithic FET type devices is presented. This parameter extraction technique has been successfully applied to extract the distributed model which simulates the small-signal performance of four monolithic MESFET devices, which only differ in the gate width (50, 100, 250 and 500 μm), at a wide variety of bias conditions, in the 1 to 40 GHz frequency band. An excellent agreement between simulation and measurements is achieved with the distributed model for all the devices and for all bias points. Extrapolation of the model parameters to a 1 mm gate width device is also carried out and compared with the measured S-parameters in order to verify the scaling performance of the model and the suitability of the extraction technique.

The devices used in this study have been manufactured on purpose to analyse the scaling features of the distributed model. They have only one finger and the access to the intrinsic FET is identical for all the devices, so that parasitic effects are the same for all of them. The results obtained for this family of devices (50, 100, 250, 500 and 1000 μm) are shown for the first time in this paper.

## PARAMETER EXTRACTION PROCEDURE

The parameter extraction procedure proposed here is based on a FET distributed model, together with a standard optimization routine. The model takes into account the propagation effects along the

gate and drain electrodes, it is capable of describing the intrinsic FET more accurately than lumped element models do, and it is a more physical model [4]. Fig. 1 shows the equivalent circuit per unit gate width of the distributed model. The elements of the admittance matrix have been defined in accordance with the conclusions drawn from a previous study based on a simple lumped element equivalent circuit used to match the S-parameters of each device at zero drain bias conditions. This previous study is similar to that presented in [5] for a different family of devices. As an example of the results obtained in this first stage with the lumped element equivalent circuit, Fig. 2 shows the total gate resistance as a function of $V_{GS}$, with the gate width as a parameter. Notice that this element is clearly dependent on the gate width and on the bias point. From the gate width dependence of this figure it is clear that there are three different contributions to the total gate resistance: (i) one part is constant and corresponds to the parasitic gate resistance, $R_g$, (ii) another part scales proportionally to the gate width and corresponds to the gate line resistance, $R_{tg}$, (iii) and there is also a part that scales proportionally to the inverse of the gate width, and means that there are parallel losses in the devices. This is the reason why $R_i$ and $R_f$ must be included in the model. These two elements are therefore incorporated for the sake of scalability.

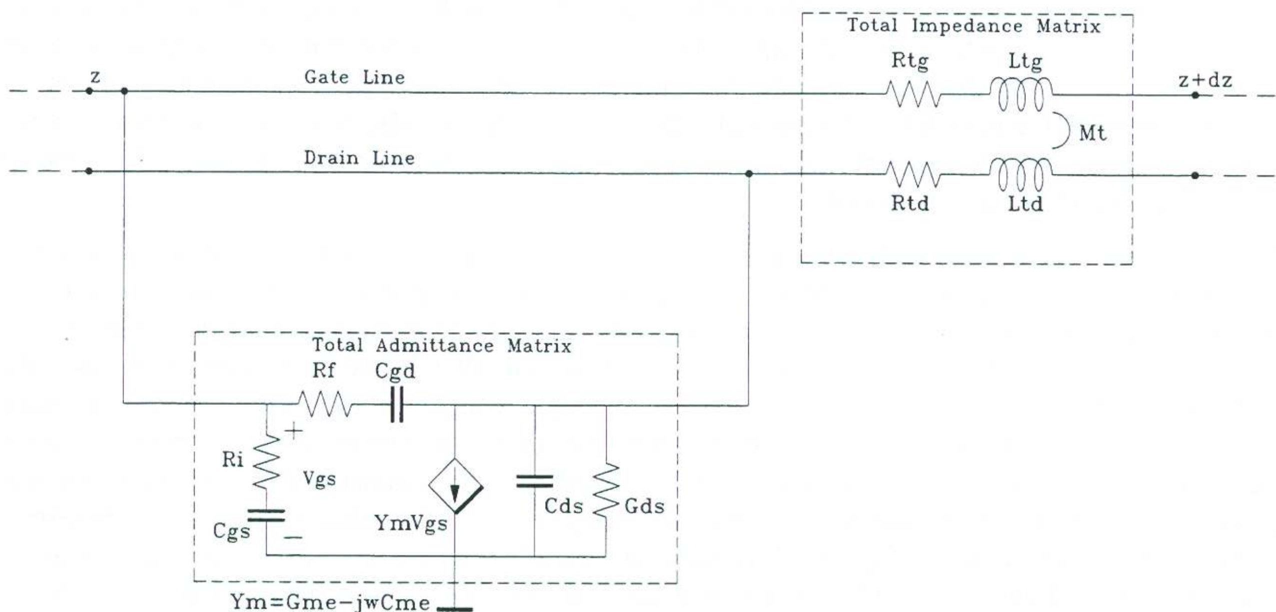


Fig.1. Equivalent circuit per unit gate width of the distributed model.

The parameter extraction technique is based on the scalability of the distributed model, which is straightforward since the model elements are defined per unit gate width [5]. Therefore there are not scaling rules in the strict sense, because scalability is simply inherent in the model definition.

The model extraction is carried out by using a optimization strategy which fits the S-parameters of all the devices with different gate widths simultaneously, forcing the fulfilment of the scaling pattern in the optimization process. This way the per unit gate width model which best simultaneously fits the measurements of all devices is obtained, and series and parallel intrinsic effects can be clearly differentiated from extrinsic effects. This extraction technique has shown to be very robust and reliable, and it is almost independent of the initial values of the model parameters.

Since various devices are involved in the process, this model extraction procedure somehow takes into account the dispersion existing among devices, which are never exactly identical. The technique ensures to a large extent that the obtained values produce the best average fitting of the measurements, and it can be used with confidence by MMIC designers for a wide range of devices.

## RESULTS

This parameter extraction procedure has been successfully applied to extract the distributed model which simulates the small-signal performance of four monolithic MESFET devices, which only differ in the gate width (50, 100, 250 and 500 μm), at a wide variety of bias conditions, in the 1 to 40 GHz frequency band.

Parasitic elements should be constant for all bias points and for all the devices, since they are related to non-active parts of the device. In a first step and to confirm the previous point, parasitic elements have been set free in the optimization process, i.e., the optimization routine has allowed parasitic elements to depend on the bias conditions. Fig. 3 shows the values obtained for parasitic inductances and capacitances as a function of $V_{GS}$ with $V_{DS}$ as a parameter. As expected, they are fairly constant, so that they can be kept constant in the optimization process (see Table I). This fact confirms the suitability of the model for representing the main aspects of the device behaviour, and proves that the parameter extraction procedure yields the correct values for the model elements.

Some of the results obtained when parasitic elements are considered bias independent are presented in Fig. 4 as a function of $V_{GS}$ with $V_{DS}$ as a parameter. $V_{DS}$ varies from 0 to 4.2 V, with a step of 0.2 V. The figures show the results for the shortest gate width device. The model for the other devices can be obtained by multiplying each equivalent circuit element by the corresponding scale factor (i.e., 2, 5 and 10 for the 100, 250 and 500 μm device, respectively). The excellent agreement between measured S-parameters and model predictions up to 40 GHz over all bias points, in the pinch-off, linear and saturation regions (see Fig. 5), again confirms the validity both of the model and the parameter extraction procedure.

The proposed extraction technique assumes that the involved devices are exactly scalable. Unfortunately, due to unavoidable differences in the manufacturing process, small deviations in the device dimensions or small changes in the channel material properties, are to be expected. An independent optimization of each device has revealed that there are two elements, the transconductance ($G_{me}$) and the output conductance ($G_{ds}$), which are especially sensitive to these differences, and consequently do not properly scale from one device to another. The main deviation from the scaling pattern occurs around $V_{GS}$=-1V. These scaling inconsistencies can be taken into account in the proposed extraction procedure by independently obtaining the values of these two elements for each device. Fig. 6 illustrates the ratio between the value of $G_{me}$ obtained independently and the value of $G_{me}$ scaled from the other devices. Notice that this parameter takes a value different from 1 only around $V_{GS}$=-1V, excluding the region near $V_{GS}$=-2V, where $G_{me}$ is close to zero and therefore the values of this ratio are not significant (do not make sense). The optimization error shows a dramatic fall in the $V_{GS}$ region affected by this new parameter as can be seen in Fig. 7.

To assess the capability of the distributed model to be scalable and the suitability of the parameter extraction procedure, the results obtained when applying the extraction technique to the 50, 100, 250 and 500 μm devices have been extrapolated to predict the performance of a 1 mm gate width device, and the S-parameters obtained in this way have been compared with the measurements. This fifth device has not been included in the optimization routine because it is not exactly scalable, as can be observed in Fig. 8, where the DC current $I_{DS}$ is represented as a function of $V_{GS}$ (at $V_{DS}$ = 4 V), for the five devices. It can be noted that the 1 mm gate width device has a different pinch-off voltage. Therefore, to extrapolate the results, it has been necessary to previously shift the gate voltage, so that the DC current $I_{DS}$ for the 1 mm gate width device can be scaled from the current of the other four devices as illustrated in Fig. 9. A comparison between extrapolated and measured S-parameters for the 1 mm gate width device is shown in Fig. 10. The excellent agreement confirms the good scaling performance of the distributed model when predicting the behaviour of different size devices.

## CONCLUSION

Although excellent fitting of the S-parameters of FET devices for a single device and a single bias point can be easily achieved by using any standard lumped-element equivalent circuit, if scalability is required only distributed models can provide a good simulation for any device regardless its gate width. The results obtained by using a distributed model to fit simultaneously the S-parameters of several devices with different gate widths corroborate this point. The results also show that this optimisation approach provides a robust and reliable extraction procedure for extracting the parameters, both intrinsic and parasitic, of the distributed model. Extrapolation of the model parameters to a larger device verifies the good scaling performance of the distributed model and the suitability of the extraction technique.

## ACKNOWLEDGEMENT

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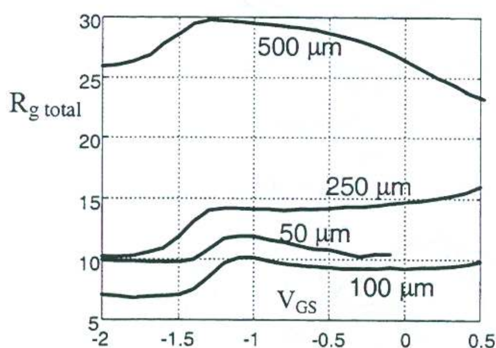


Fig. 2. Extrinsic gate resistance versus gate voltage at $V_{DS}$=0, when using a lumped element model.

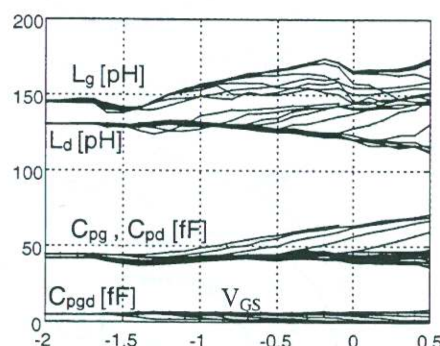


Fig. 3. Some parasitic elements as a function of $V_{GS}$ with $V_{DS}$ as a parameter.

| $R_g$ | $R_d$ | $L_g$ | $L_d$ | $C_{pg}$ | $C_{pd}$ | $C_{pgd}$ |
|---|---|---|---|---|---|---|
| 0.8 Ω | 1.3 Ω | 144 pH | 130 pH | 42 fF | 44 fF | 5 fF |

Table I. Parasitic element values.

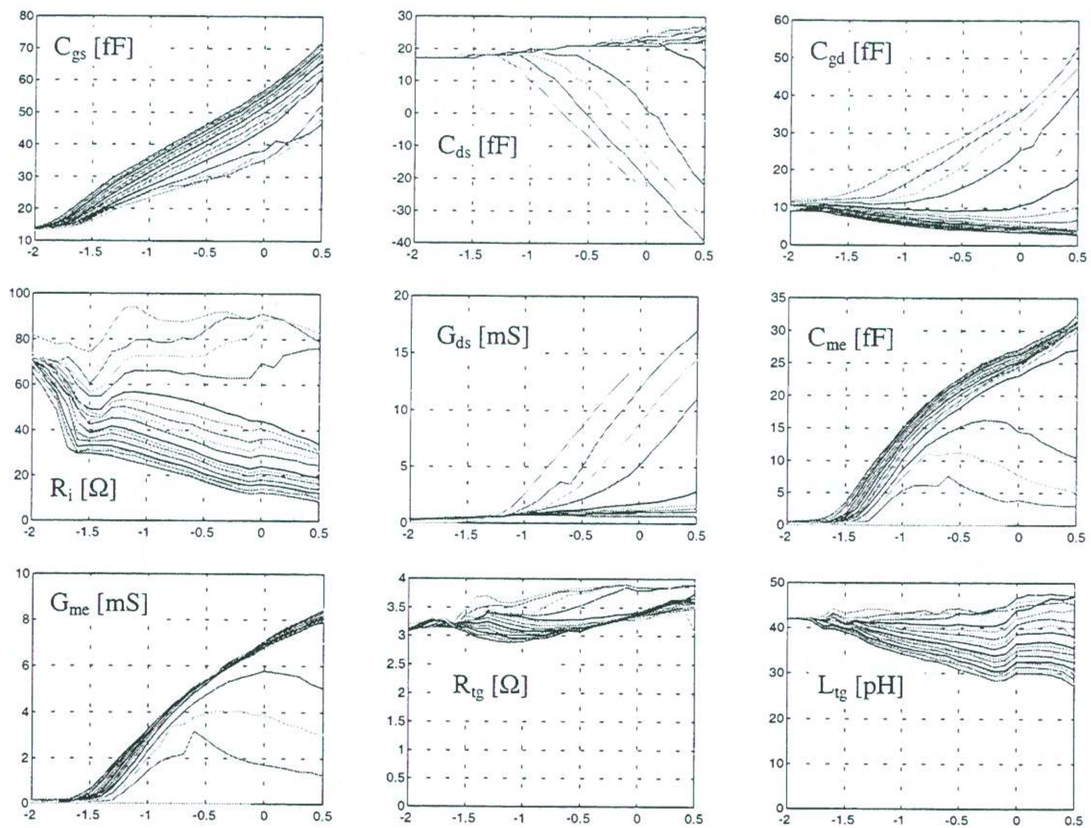


Fig. 4. Some intrinsic elements as a function of $V_{GS}$ with $V_{DS}$ as a parameter.

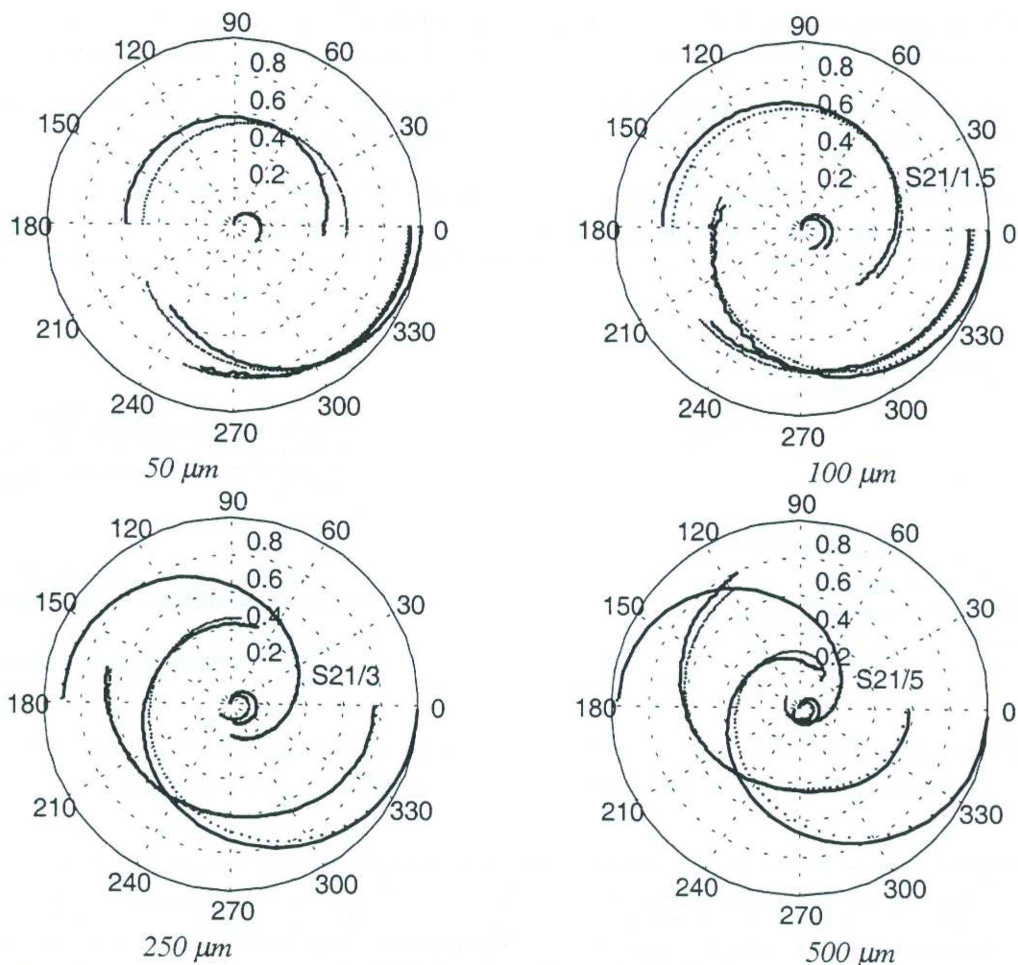


Fig. 5. Comparison between measured (*continuous lines*) and simulated (*dotted lines*) S-parameters for four devices (50, 100, 250, 500 μm) at $V_{GS}$= -0.6V and $V_{DS}$= 4V.

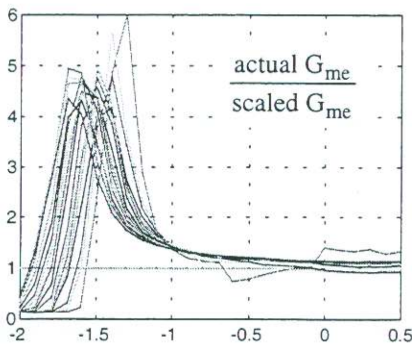


Fig. 6. Ratio between the actual value of $G_{me}$ and the scaled value of $G_{me}$ as a function of $V_{GS}$ with $V_{DS}$ as a parameter, for the 250 μm gate width device.

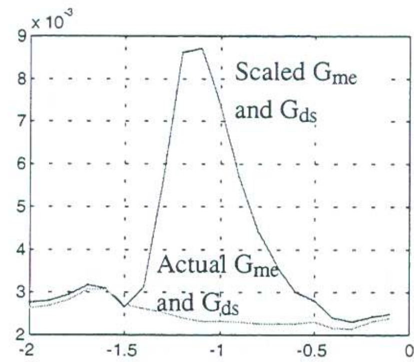


Fig. 7. Optimization error versus $V_{GS}$ at $V_{DS}$=0 (scaled and actual $G_{me}$ and $G_{ds}$).

$$Error = \frac{1}{M} \sum_{i=1}^{M} \sum_{j=1}^{4} \left| S_{ij}^{measured} - S_{ij}^{simulated} \right|^2$$

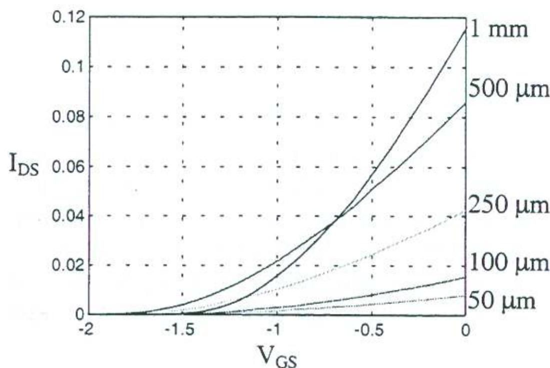


Fig. 8. $I_{DS}$ as a function of $V_{GS}$ at $V_{DS}$ = 4 V for the five devices. Notice that $I_{DS\,(1\,mm)}$ is not $2 \times I_{DS\,(500\,\mu m)}$.

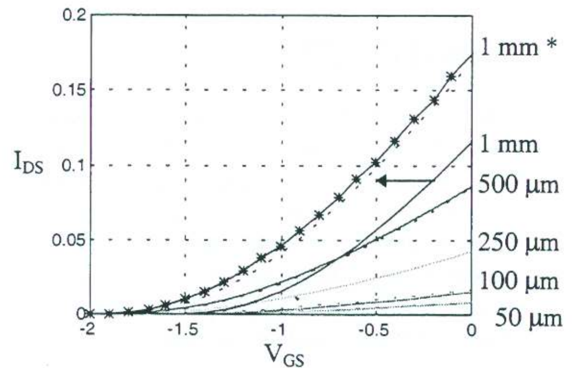


Fig. 9. $I_{DS}$ as a function of $V_{GS}$ at $V_{DS}$ = 4 V for the five devices (--- $4 \times I_{DS\,(250\,\mu m)}$ ; * after shifting $I_{DS\,(1\,mm)}$ towards the left to make it scalable).

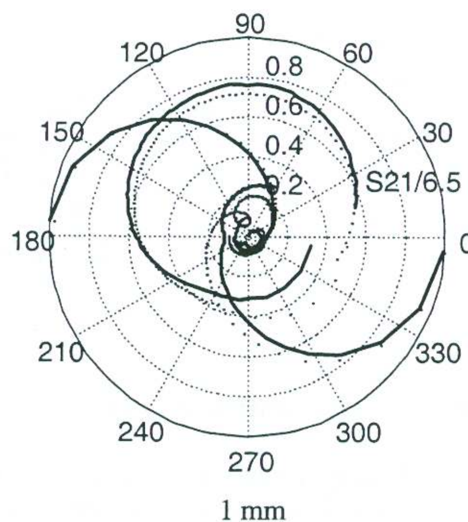


Fig. 10. Comparison between measured (*continuous lines*) and extrapolated (*dotted lines*) S-parameters for the 1 mm gate width device at $V_{GS}$= -0.6V and $V_{DS}$= 4V. The extrapolation has been carried out from the results obtained for the other four devices at $V_{GS}$= -1V, $V_{DS}$= 4V.