40 Gb/s ICs Using a Production PHEMT Technology

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Abstract

This contribution presents a new set of digital ICs dedicated to optical fibre links, realised using a qualified GaAs P-HEMT technology with 0.25 µm gate length. The ICs include 2:1 selectors, 1:2 DEMUXes, D-flip-flops, dividers by 2, operating at bit-rates up to 40 Gb/s. Applications include high speed optical fibre systems. These circuits may also be considered as basic building blocks for future higher complexity digital functions.

1. Introduction

Due to the increasing need for high capacity transmission systems, high bit-rate data processing is needed for 20 to 40 Gb/s optical links. Reliable industrial devices are needed, and therefore components using stabilised and fully released technologies will be preferred. To date, MUX and DEMUX ICs operating up to 40 Gb/s have been reported, using bipolar technologies or in development FET technologies (InP or GaAs), but there is almost no published results at 40 Gb/s using production FET technology. We report a set of basic digital building blocks including 44 Gb/s selector and 40 Gb/s demultiplexor, 20 Gb/s D-flip-flop, and 20 GHz static divider by 2 ICs. These ICs are using one of Philips standard technologies.

2. Technology and Architecture

The circuits were fabricated using Philips production-line ED02AH technology. This technology uses 0.25 µm gate-length Enhancement and Depletion P-HEMTs and is under space qualification. Average transition frequency (F_T) is 64 GHz. Figure 1 shows the technology road map of Philips Microwave Limeil.

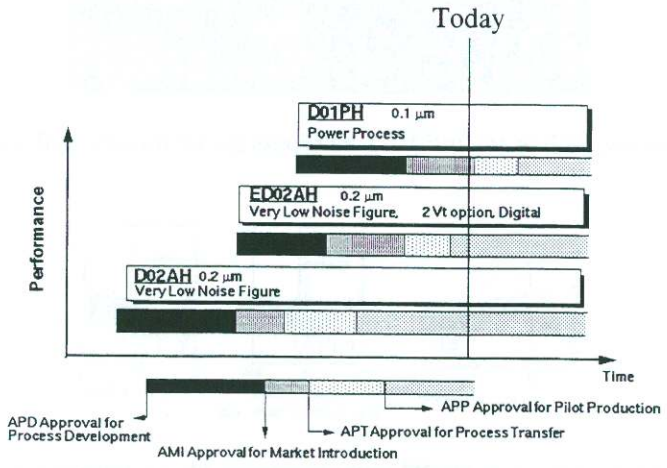

Fig. 1 : Philips Microwave Limeil millimetre-wave technology road map

For all the circuits described here, the design is based on SCFL logic. All the data and clock inputs are single-ended. Compared to a fully differential design, this approach gives slightly reduced bandwidth but brings significant facility for practical application in a system. At the outputs, two-stage output buffer ensures both signal regeneration and 50 Ω output matching.

The key of a high-speed design is the choice of the optimal compromise between speed and functionality. At the basic SCFL inverter gate level, the balance is done between propagation delay and small-signal gain for a given technology. The optimal case being a gain a little higher than 1, in order to ensure signal reshaping, while keeping the propagation delay as small as possible. In order to point out the best compromise, a set of 16-stage SCFL ring-oscillator circuits with various gain/load ratios was realised and tested. Results show that the minimum propagation time is as low as 7 ps (value which has, to our knowledge, never been reported so far), while a propagation time of 8.5 ps was demonstrated to be reachable under reliable and reproducible conditions. A dependence of the propagation time over supply voltage was also recorded.

2. A 44 Gb/s selector

2:1 selector ICs were designed, realised and measured (A photography of the circuit is shown on figure 2). The selector core is the most critical part, for which a minimum value R-C product was chosen. Furthermore the input source-followers of the selector core were placed very close to the switching transistors in order to supply transient currents to the gate of these transistors. A two-stage output buffer ensures both signal regeneration and 50 Ω output matching. The chip size is 1.5 x 1.5 mm². Power consumption is lower than 1 W.

The measurement set-up includes a 12.5 Gb/s Pseudo-Random Bit Sequence generator supplying two data-streams with 2^{23}-1 word length, which are multiplexed by a commercial 20 Gb/s selector unit (output eye-diagram of this commercial selector is shown on top of figure 5). The two output data are then input into our selector IC with a large delay against each other so that the patterns are nearly uncorrelated.

Eye-diagram measurements were done up to 44 Gb/s (see eye-diagram at 40 Gb/s on figure 3). At these bit-rates, degradations are already introduced by the test set-up, and especially by the commercial selector unit, by probes and by phase noise of the clock source, so the real eye-diagram should be even better than what is shown in fig. 3. The Clock Phase Margin (C.P.M.) was measured at several bit-rates. Recorded values are 230 ° at 20 Gb/s, 115 ° at 40 Gb/s and 80 ° at 44 Gb/s. these values are high enough to ensure reliable operation (this compares favourably to state-of-the-art results like [1, 2, 3]). Furthermore, it appears that the relation between the C.P.M. and the bit-rate is very linear up to the 44 Gb/s limit of our test-set-up (see fig. 4), which shows that the circuit may be operated at bit-rates above 44 Gb/s.

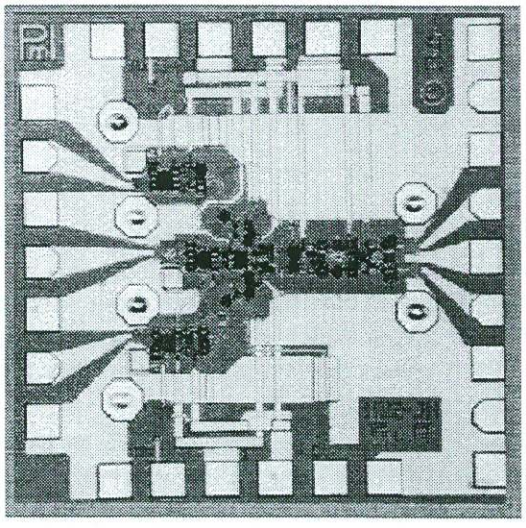

Fig. 2 : Photography of the selector IC (1.5x1.5mm²)

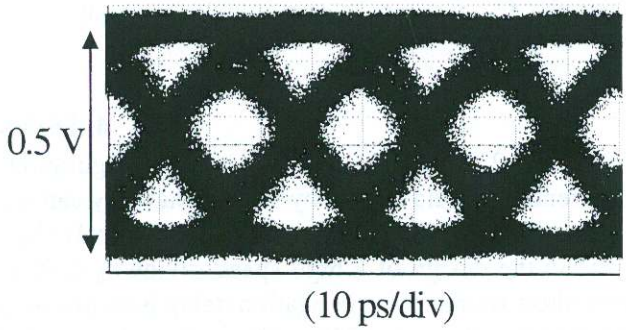

Fig. 3 : Output eye-diagram of the selector IC at 40 Gb/s (obtained using non-ideal test set-up described in section 2)

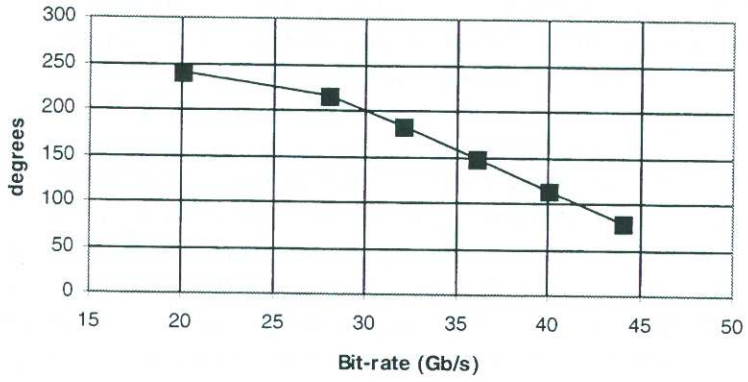

Fig. 4 : Recorded Clock Phase Margin of the selector IC versus output bit-rate

3. Demultiplexing at 40 Gb/s

1:2 DEMUX ICs were designed and realised. The critical design issues were investigated. DEMUX operating up to 40 Gb/s was demonstrated. The output eye diagrams are particularly clear and well opened with very short rise and fall times (about 20 ps). The DEMUX ICs are also functional at lower bit-rate (fig. 5 shows the input and output eye-diagrams at 20 Gb/s input data-rate). These circuits may thus be cascaded as shown on fig. 6, in order to realise a 1:4 DEMUX. This may be done either using a hybrid approach or a monolithic design.

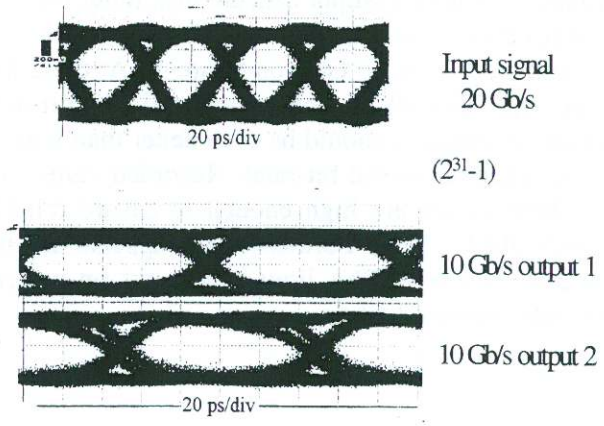

Fig. 5 : DEMUX output eye-diagrams at 10Gb/s and 20Gb/s input eye-diagram from the test set-up

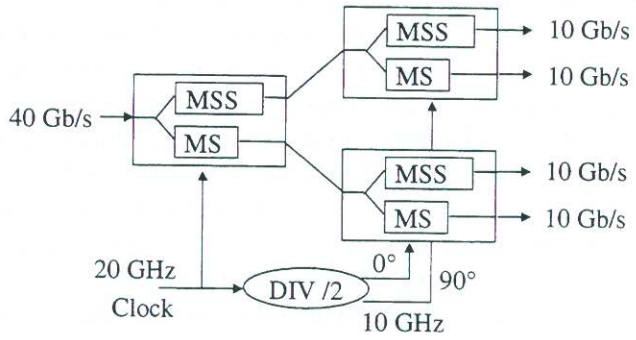

Fig. 6 : Block diagram of a 1:4 DEMUX

4. Divide-by-2 IC

Divide-by-2 circuits based on a static configuration were designed and tested. These dividers supply two differential signals shifted by 90°, so that they can easily be used in a 40 Gb/s 1:4 DEMUX.

Static divide-by-2 circuit uses a master-slave D-flip-flop which output is connected to the input. A critical issue in the design of a high speed divide-by-2 IC is to achieve a layout which keeps this interconnection very short so that the propagation delay is as low as possible. Fig. 7 shows the layout of the circuit, with the small D-flip-flop core (250 x 300 μm^2), and, around of it, the input and output buffers.

Measurement shows that the circuit is functionnal inside an input frequency ranging from 7 GHz to 23 GHz. For 10 to 20 GHz input frequency range, the output amplitude on each of the 4 outputs is equal or greater to the input amplitude (see fig. 9). Fig. 8 shows the output waveforms when the IC is driven by a 20 GHz sinus-wave signal. The maximum sensitivity (29 mV) is reached for an input frequency of 17 GHz. Noise measurement was done, and it appears that the output noise is lower than –100 dB/Hz at 100 KHz from the carrier for an input frequency of 20 GHz. This value is very low, compared to the noise of the source (-64.5 dB/Hz), which has a lot of amplitude noise.

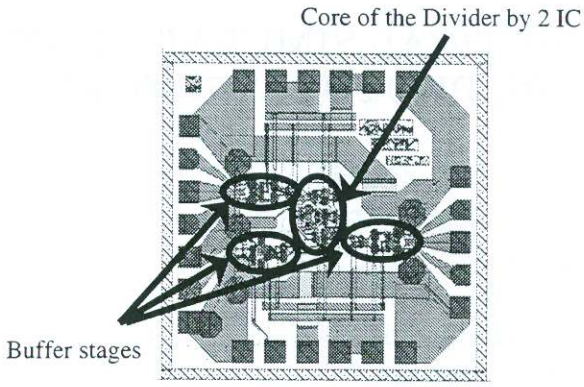

Fig. 7 : Layout of the Divide-by-2 circuit

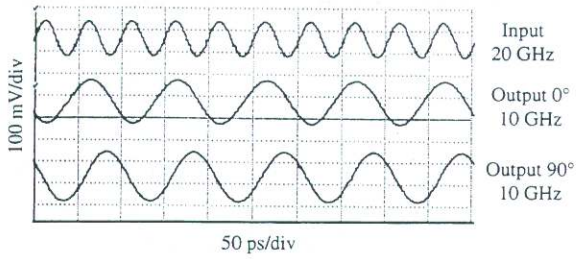

Fig. 8 : Divider by 2 output signals measured at 20 GHz input frequency (shown on the top)

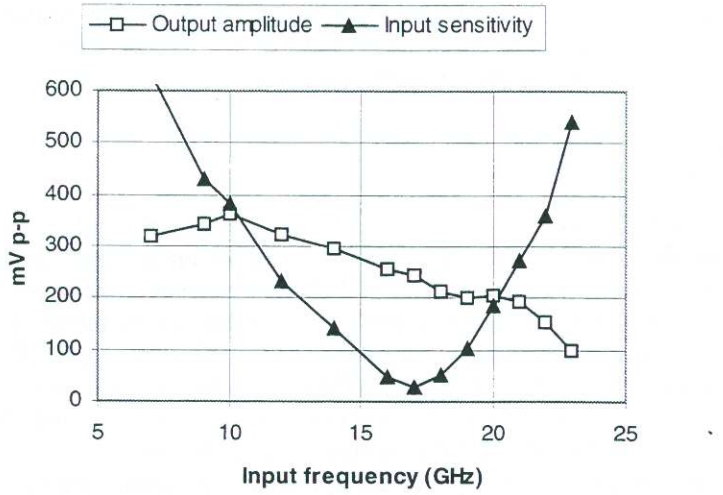

Fig. 9 : Measured input sensitivity of the divide-by-2 IC and corresponding output amplitude.

5. Conclusion

Results on digital processing ICs operating up to 40 Gb/s are presented. Prototypes using the ED02AH fully released 0.25 µm gate length GaAs P-HEMT technology with transition frequency of 64 GHz exhibit performance compatible with 40 Gb/s operation at lower cost price than InP-based processes. This result is explained by the high Bit-rate/F_T ratio achieved by this chip-set. Our results also show that 40 to 50 Gb/s is the limit for ED02AH technology. Higher bit-rate operation (60 to 80 Gb/s) requires a shorter gate length P-HEMT technology.

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