# K-BAND CHIPSET FOR FULLY INTEGRATED POINT TO MULTIPOINT MICROWAVE MODULES USING 0.25 MICRON PHEMT MMIC TECHNOLOGY

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## ABSTRACT

The high volume point to multipoint market demands lowest cost components for all building blocks of the system, particularly for the microwave circuits. Different types of MMICs, including frequency generating block, were developed using TriQuint's 0.25 micron power pHEMT MMIC technology to realize highly integrated transceiver units. Measured results for LNA (low noise amplifier), medium and high power amplifier, mixer and oscillator circuits are presented.

## 1. INTRODUCTION

Two major issues have been the initiators to start MMIC chipset developments for point to multipoint applications in Ku through K-band:

1. None commercial available MMIC's fulfilling requested specifications.
2. If available (although lack in specification compliance) MMIC's price is much more expensive than justifiable for mass production quantities.

A carefully study of the processes available on the market led to the result that TriQuint's 0.25 micron power pHEMT process was the best choice to achieve the requested specifications for the variety of circuits to be developed. The process offers 0.25 micron AlGaAs / InGaAs pHEMTs with an undoped InGaAs channel surrounded by two low-doped AlGaAs layers. A narrow and a wide recess are etched into the GaAs and AlGaAs layers respectively to ensure best compromise between both, $f_t$ (cut-off frequency) and $V_B$ (breakdown voltage). Typ. values achieved for a 600 micron pHEMT are $f_t$ = 33 GHz and $f_{max}$ = 78 GHz. All circuits are realized on 100 micron substrates using conventional microstrip technique. Two different chipsets were developed in parallel. One for the 15 to 20 GHz frequency range and the second for 20 to 26 GHz. Each chipset includes a LNA, a medium and a high power amplifier, mixer as well as a fundamental oscillator.

The results for the chipset for the 20 to 26 GHz range are presented. As far as not different noted, all shown results are 2nd pass results achieved by using sophisticated tuning capabilities implemented in the 1st pass layouts.

## 2. LNA (Low Noise Amplifier)

A different approach as compared to the classical way of designing LNAs was chosen. Instead of designing for outstanding noise figure data performance, a trade-off between noise figure, gain and output power respectively had to be found to meet the required system specifications. This is due to the multi-carrier point to multipoint application which requires LNAs with excellent linearity. To achieve the requested output power of $P_{1dB} > 15$ dBm a 400 micron total gatewidth FET cell was chosen for the first as well as for the second amplifier stage. Using this stage topology outstanding performance for the output power combined with good noise figure data was achieved. One major issue during the design process of the amplifier was to control stability. Using the S-Probe technique [1], stability of the design was controlled not only in the operating band, but from lowest frequencies up to the maximum frequency where the single FET device is able to oscillate. All process variations were taken into account to avoid stability problems during mass production of the MMIC.

The input and output networks of the 2 stage LNA, as shown in Fig. 1 ($1^{st}$ pass design), are designed for lowest transmission losses to ensure low noise figure and high output power. The interstage matching network guarantees mainly in-band stability and flattens the gain response.

The final measured results for the LNA are shown in Fig. 3 presenting small signal gain, input as well as output reflection loss and noise figure versus frequency. The amplifier demonstrates a small signal gain of $16 \pm 1$ dB, an excellent output matching better than 15 dB and a input matching around 5 dB from 21 to 28 GHz. The noise figure data were taken from 20 to 26 GHz and show values from 2.5 to 3 dB. The bias conditions were set for optimum output power respectively linearity and are $V_{DS} = 3.5$ V and $I_{DS} = 20 / 30$ mA ($1^{st}$ / $2^{nd}$ stage).

## 3. POWER AMPLIFIERS

Higher state modulation schemes, as 16 QAM or 8 QPSK, create high demands on linearity (intermodulation) and phase distortion versus RF-drive respectively, of the amplifiers applied in the transmit chains. Several published power amplifier MMICs in K-band through Ka-band [2], [3], [4], [5] show similar FET topologies. All referenced amplifier MMICs are designed using a smaller sized (gatewidth) FET as the driver stage and a bigger sized FET in the final stage. This topology yields high efficient amplifiers (PAE > 30% for power drive) but does not provide an adequate result for gain expansion as well as for linearity. To fulfill the system requirements both stages of a two stage amplifier use the same size of gatewidth for driver, as well as for the final stage.

The output matching network was designed with regard to optimum output power combined with good intermodulation behavior and output matching. Base for the design were load-pull large signal measurement data, performed with a commercial load-pull system, supported by the foundry. The interstage matching network was designed for optimum power match of the driver stage, too. In addition slight correction to the gain slope were included. Finally the input matching network provides an adequate input matching performance and flattens gain slope as good as possible.

As already described for the LNA, a rigorous stability analysis using the S-Probe technique [1] was performed. Low frequency as well as high frequency instabilities were carefully analyzed and eliminated. For combined amplifier stages, gates and drains were connected together to avoid high frequency "ring-oscillations".

To realize transmit amplifier chains, a medium power amplifier and a high power amplifier were developed. The photographs of the first design iterations are shown in Fig. 2 and Fig. 6, respectively.

The medium power amplifier uses two 600 micron FET structures. Biasing the MMIC with $V_{DS}$ = 6.5 V and $I_{DS}$ = 2 x 80 mA leads to the response curves as presented in Fig. 4 and Fig. 5. In Fig. 4 a small signal gain from around 16 dB, together with a moderate input / output matching are shown from 20 to 29 GHz. In addition the 1 dB gain compressed output power of $P_{1dB}$ > 25 dBm was observed in the operating band. Fig. 5 shows the output power, gain expansion as well as the phase variation for $S_{21}$ versus input power drive of the amplifier for 24 GHz.

The high power amplifier combines four 600 micron FET structures, for the final as well as for the first stage, for the MMIC's total gatewidth of 4.8 mm. The amplifier is typical biased with $V_{DS}$ = 6.5 V and $I_{DS}$ = 2 x 320 mA. Measured response curves, equivalent to the medium power amplifier, are shown for the high power amplifier in Fig. 7 and Fig. 8.

## 4. MIXER

To decrease the number of mixer designs for Ku through K-band a broadband double balanced mixer topology, comparable to reference [6] was chosen. Instead using modified Marchand baluns a new type of balun is introduced. The presented mixer consists of two novel baluns (RF & LO) and a ring diode quad together with a transmission line choke for the intermediate frequency port. The LO and RF are fed at the unbalanced balun ports, and IF is tapped out at IF port as shown in Fig. 9. The mixer is suitable for both, down and up-conversion.

The used pHEMT-diode, 0.25 x 75 micron in size, shows series resistance about 10 Ω and a zero bias junction capacitance about 95 fF, which corresponds to a cut-off frequency of 167 GHz. The influence of the small diode junction capacitance on conversion loss at high LO drive level is negligible. The dynamic range of the mixer is further improved by using the ring diode quad to realize a double balanced mixer.

The introduced new type of balun consists of a coupled microstrip line and coupled line structure similar to a Lange coupler. This structure was chosen to achieve tight coupling. The exact dimensions of the planar structure of the balun were determined by using a field simulator [7].In addition, the RF and LO baluns are partially used to match the RF and LO ports of the ring diode quad. The IF choke consists of approximate quarter wave coupled lines which are grounded at the IF port through a resistor / capacitor series combination.

First pass measured results for conversion loss and two tone intermodulation are shown in Fig. 10. A conversion loss of typical 7 dB and outpout-$IMD_3$ values of around 55 dB are shown from 20 to 28 GHz.

## 5. OSCILLATOR

The oscillator MMIC, see Fig. 11, is a three stage circuit working in a fundamental mode. Hence no frequency multiplier is needed. The MMIC consists of one oscillator stage and two buffer stages. It is designed to perform in a thin-film network (TFN) environment with three bond-wires at the input and at the output interconnect, respectively.

The oscillator stage, providing the negative resistance to the frequency defining resonant circuit, is designed in a common drain configuration. The two buffer-amplifier stages are reducing the load-pulling on the oscillator stage due to their isolation. The small signal gain of the buffer stages is typically 16 dB.

To obtain a high oscillation margin over the frequency band good matching for $S_{11}$ is required. As shown in Fig. 12 the $S_{11}$ for the oscillator circuit amount approximately 10 dB from 20 to 27 GHz. Due to the two buffer stages the MMIC has the capability to deliver a saturated output power of 26.5 dBm with a 1 dB gain compression point at 24.5 dBm, typically.

Combining the MMIC with an external dielectric resonator, free-running phase noise data of typical - 40 dBc / Hz @1 kHz and - 98 dBc / Hz @100 kHz frequency offset were achieved.

## 6. CONCLUSIONS

A complete chip set for highly integrated transceiver front-ends in K-band was presented. Due to the variety of developed circuits demonstrated, a playground for setting up different transceivers for a variety of application is given. Some MMIC's, in the meantime, are used in classical point to point radio link systems, as well as in point to multipoint applications.

High linear amplifiers for applications in transmitter chains, as well as for high linear receiver line-ups were introduced. For low noise applications noise figure data around 3 dB together with $P_{1dB}$>15 dBm were demonstrated in K-band. Two amplifiers for applications in transmit chains (medium and a high power amplifier) show $P_{1dB}$ data greater than 25 and 30 dBm over bandwidths more than 35%.

A double balanced mixer circuit using a novel type of RF & LO-balun was presented. Measured results show a typical conversion loss around 7 dB in the operating band.

A challenging fundamental oscillator design, consisting of an oscillator plus two buffer stages, shows $|S_{11}|$>9 dB combined with a bias depending output power of greater 25 dBm from 20 to 27 GHz.

All shown results, except for the mixer circuit, were achieved by tuning the first pass layout. All tuning steps were then built into the 2nd pass layout by only changing the masks for the metal levels.

## 7. ACKNOWLEDGEMENTS

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## REFERENCES

[1] Ken Wang, Marty Jones and Steve Nelson. *"The S-Probe. A New, Cost-Effective, 4-Gamma Method for Evaluating Multi-Stage Amplifier Stability"*, IEEE MTT-S Digest (1992), pp.829-832

[2] Simon, K.M. *et al. "K through Ka-band driver and power amplifiers"*, IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1996, pp.29-32

[3] Yarborough, R. et al. *"Performance comparison of 1 watt Ka-band MMIC amplifiers using pseudomorphic HEMTs and ion-implanted MESFETS"*, IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1996, pp.21-24

[4] Wu, C.S. et al. *"Pseudomorphic HEMT manufacturing technology for multifunctional Ka-band MMIC applications"*, IEEE MTT, Feb. 1995, Vol. 43, pp.257-266

[5] Bill T. Agar Jr. *et al. "The IRIDIUM® K-Band MMIC Chip Set"*, IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1995, pp.21-24

[6] Brinlee Wayne R. *et al. "A Novel Planar DOUBLE-Balanced 6-18GHz MMIC Mixer"*, IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1994, pp.139-142

[7] IE3D, Zealand Software Inc., Fremont, CA 94538

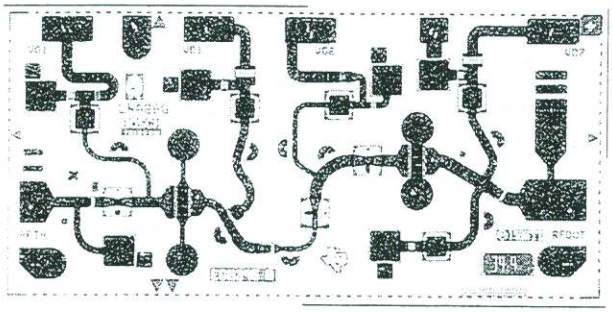

Fig. 1: Low Noise Amplifier (1.52 x 3.05 mm)

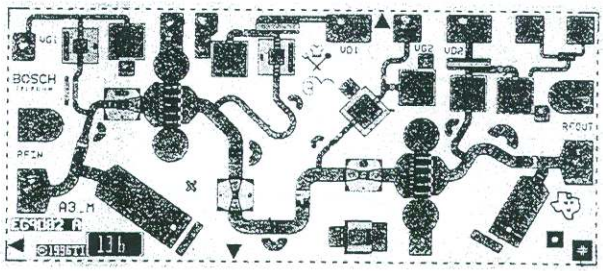

Fig. 2: Medium Power Amplifier (1.27 x 2.79 mm)

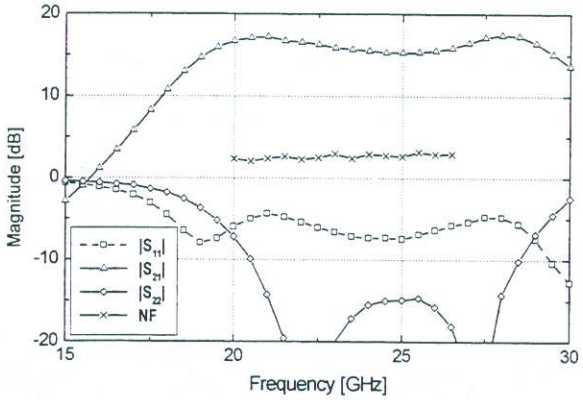


Fig. 3: Low Noise Amplifier: Small signal and noise figure curves for $V_{DS}$=3.5 V, $I_{DS}$=20/30 mA

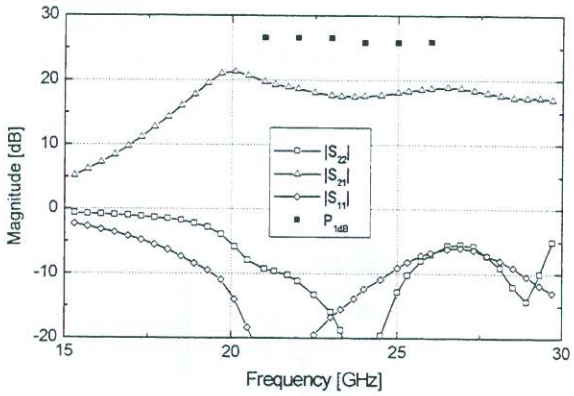


Fig. 4: Medium Power Amplifier: Small signal and 1 dB gain compressed response curves versus frequency for $V_{DS}$=6.5 V, $I_{DS}$=2 x 80 mA

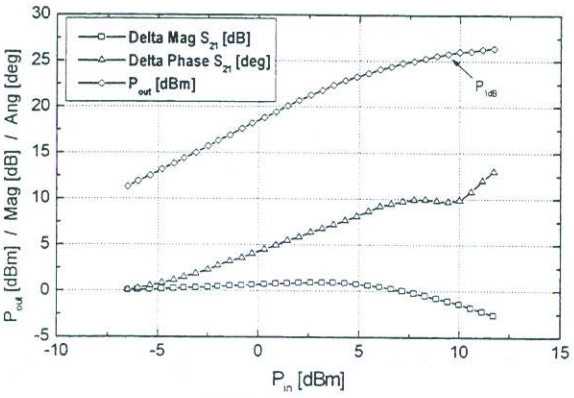


Fig. 5: Medium Power Amplifier: Output power and gain- / phase alteration versus input power drive for $V_{DS}$=6.5 V, $I_{DS}$=2 x 80 mA

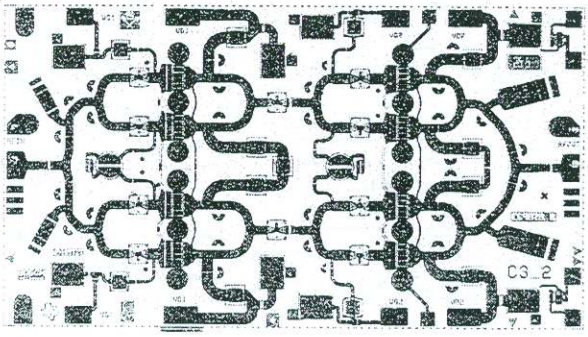

Fig. 6: High Power Amplifier (2.49 x 4.39 mm)

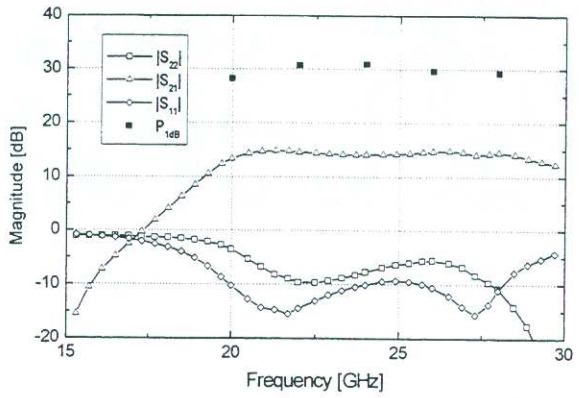


Fig. 7: High Power Amplifier: Small signal and 1dB gain compresses measured responses for $V_{DS}$=6.5 V, $I_{DS}$=2 x 320 mA

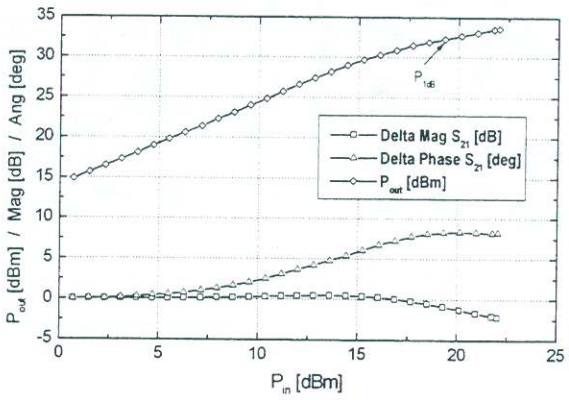


Fig. 8: High Power Amplifier: Output power and gain- / phase alteration versus input power drive for $V_{DS}$=6.5 V, $I_{DS}$=2 x 320 mA for f=23 GHz

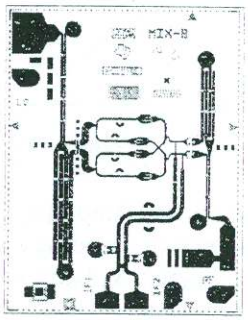

Fig. 9: Double Balanced Mixer (2.66 x 2.03 mm)

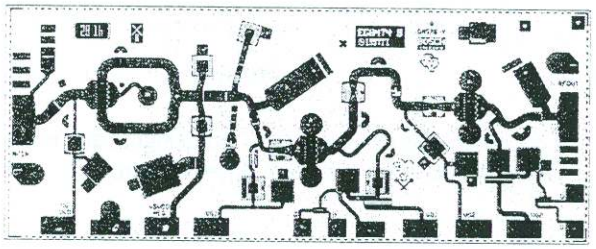

Fig. 11: Fundamental Oscillàtor (1.73 x 4.28 mm)

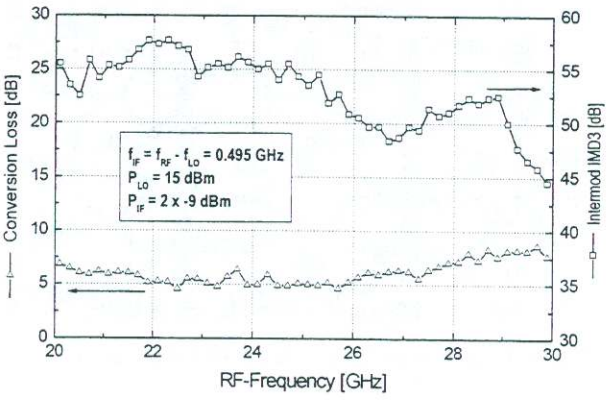


Fig. 10: Mixer: Conversion gain and output-$IMD_3$ versus frequency

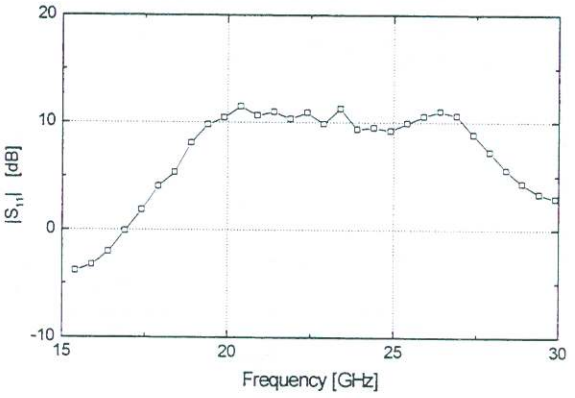


Fig. 12: Oscillator: Small signal input reflection loss versus frequency $V_{DS}$=±6.5 V, $I_{DS}$=3 x 80 mA