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Material Characterization and Device Performance of $In_{0.7}Al_{0.3}As/InAs/In_{0.8}Ga_{0.2}As$ HFET Structures Fabricated on GaAs

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Abstract

$In_{0.7}Al_{0.3}As/InAs/In_{0.8}Ga_{0.2}As$ modulation-doped heterostructures on GaAs were characterized and HFETs were fabricated. A linearly graded InAlAs buffer was used to transform the lattice constant from that of GaAs to $In_{0.8}Ga_{0.2}As$. Random surface morphology with scattered volcano-like deep holes was observed. The root-mean-square roughness value was 4-7 nm. Most dislocations were confined in the graded buffer and the maximum threading dislocation density in the HFET layers was estimated to be in the order of 10^6 cm^{-2}. An electron mobility of $1.37 \cdot 10^4$ cm^2/Vs with a carrier density of $1.88 \cdot 10^{12}$ cm^{-2} at 300 K was achieved. HFETs with a 0.1 µm gate length showed an extrinsic transconductance of 750 mS/mm, an extrinsic f_T of 90 GHz and an f_{max} of 225 GHz.

Introduction

Recently there has been a growing interest in fabrication of $InAlAs/In_xGa_{1-x}As$ ($x \geq 0.53$) heterostructure field effect transistors (HFETs) on GaAs substrates [1-4]. The motivations are on one hand the superior DC and RF performance of such devices fabricated on InP [5,6], and on the other hand the advantages of using GaAs rather than InP for its lower cost, mechanically less brittle and easier to manufacture and process in MMIC technology. We have previously reported the DC and RF performance of $In_{0.7}Al_{0.3}As/In_{0.8}Ga_{0.2}As$ HFETs fabricated on GaAs using a linearly graded In(AlGa)As buffer [3]. Here, we present material characterization of such HFET structures and device performance from a sample with a 4 nm thick InAs layer inserted in the $In_{0.8}Ga_{0.2}As$ channel.

Sample growth and device fabrication

All samples were grown by molecular beam epitaxy (MBE) under As-rich growth conditions. A typical structure is shown in Fig. 1. A 1 µm thick linearly graded $In_xAl_{1-x}As$ (x from 0.02 to 0.8) buffer and 100 nm $In_{0.8}Al_{0.2}As$ were grown at a thermocouple temperature, T_{tc}, of 400 °C. The use of a low growth temperature was intended to reduce dislocation density and minimize three-dimensional islands on the surface, while the use of InAlAs rather than InGaAs as graded buffer was to reduce the background impurity level. The HFET structure consisted of a 35 nm channel, a 5 nm $In_{0.7}Al_{0.3}As$ spacer, a 25 nm $In_{0.7}Al_{0.3}As$ Schottky layer and a 5 nm undoped $In_{0.8}Ga_{0.2}As$ cap. The channel was either $In_{0.8}Ga_{0.2}As$ (#600) or $In_{0.8}Ga_{0.2}As$ with an InAs layer inserted at (#599) or 3 nm from (#589, #590 and #598) the interface between the channel and the spacer. The thickness of InAs was 6 nm for #590 and #599, and 4 and 8 nm for #589 and #598, respectively. Silicon δ-doping was used with a nominal doping density of $4 \cdot 10^{12}$ cm^{-2}. The growth temperature was 480 °C as measured by a pyrometer, T_p, for the channel and the spacer, and was reduced to T_{tc}=400 °C for the rest of the structure to minimize Si diffusion toward the surface (except for #589). Both T_{tc}- and T_p-values are nominal values. The measured T_{tc}-value is in general higher than the T_p-value. Characterization techniques include atomic force microscopy (AFM), transmission electron microscopy (TEM), and Hall effect measurements.

HFETs were fabricated on #589 with standard photolithography for isolation and ohmic contact definition. The isolation was performed with wet etched mesas. The ohmic metallization was Au/Ge/Ni and the contacts were annealed by rapid thermal annealing. T-shaped gates were defined with electron beam lithography using a three-layer resist system. A selective citric acid based etch was used for recess etching. The gate metallization (Au/Pt/Ti) was electron beam evaporated. The gate length was approximately

0.1 μm. Finally a thick gold layer was evaporated on the bonding pads.

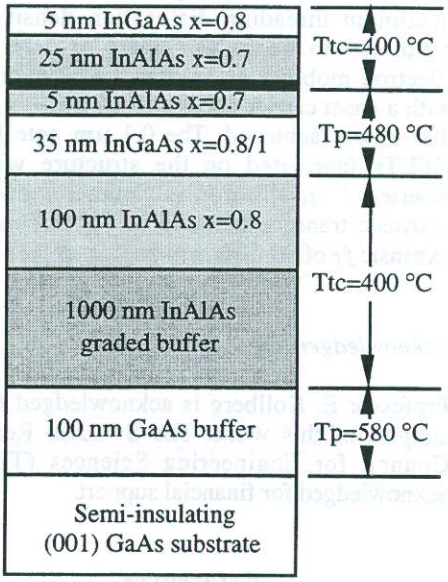

Figure 1. HFET structure configuration.

Results and discussions

Samples are mirror-like to the naked eye. Random surface morphology with deep holes was observed in AFM. Such deep holes were volcano-like with a broken rim of the crater. They were about 1 μm in diameter and could be as deep as 100 nm with a density in the order of 10^6 cm^{-2}. The root-mean-square (rms) surface roughness value was no less than 4-7 nm which might be due to the presence of the deep holes. Cross-sectional TEM revealed that most dislocations were confined in the graded buffer resulting in a small threading dislocation density in the HFET layers. A typical TEM image of HFET layers is shown in Fig. 2 from one of the previously grown structure with an $In_{0.8}Ga_{0.2}As$ channel and an InGaAs/InAlAs superlattice on the graded buffer [3]. The maximum density was estimated to be in the order of 10^6 cm^{-2}, which is several orders of magnitude smaller than the theoretical value of 10^{12} cm^{-2}. This demonstrates the effectiveness of using a graded buffer to reduce dislocation density in a semiconductor heterostructure with a lattice misfit of 5.7 %. Tersoff has proposed a model to explain this phenomenon [7]. According to his model the graded layer has a large residual strain near the surface which helps to push dislocations to the sample edges. Newly generated dislocations lie in a region free from previous dislocations. Thus the pinning effect which impedes the motion of threading dislocations is reduced. Furthermore, dislocation nucleation is inhibited deep inside the graded buffer where the strain is greatly reduced. This favours existing threading dislocations gliding to sample edges to relieve strain. All factors increase the gliding efficiency of threading dislocations. Thus the threading dislocation density can be significantly reduced.

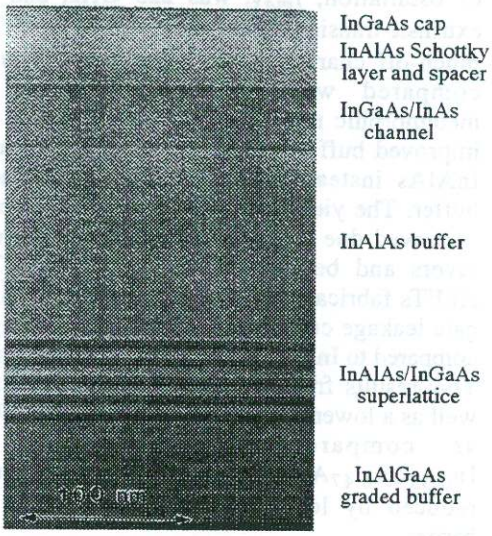

Figure 2. Cross-sectional TEM image of a HFET lstructure.

Results of electron mobility and sheet carrier density are summarized in Table I. As seen, all room-temperature mobilities exceed 10^4 cm^2/Vs indicating a good material quality. The lower carrier density in #589 as compared with the other samples results from Si diffusion to the surface at a relatively high growth temperature of 480 °C. The highest mobility is $1.37 \cdot 10^4$ cm^2/Vs with a sheet carrier density of $1.88 \cdot 10^{12}$ cm^{-2} from #599. The carrier density is similar to #590 but the mobility is 21 % higher. This implies that most electrons are confined within the 6 nm thick InAs quantum well between the spacer and the $In_{0.8}Ga_{0.2}As$ channel. The slightly smaller carrier density for #600 as compared with that of #590, #598 and #599 is due to the lower conduction band offset. These mobility values are higher than that from the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ lattice matched to InP [6] and are comparable to $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ HFETs on InP [5].

Table I. Summary of electron mobility, μ (in 10^4 cm^2/Vs), and sheet carrier density, n (in 10^{12} cm^{-2}).

Sample No.	300 K		77 K	
	μ	n	μ	n
#589	1.29	1.38	3.16	1.56
#590	1.13	1.83	2.30	2.00
#598	1.06	1.75	1.91	1.89
#599	1.37	1.88	3.46	2.01
#600	1.14	1.58	2.58	1.65

The devices were DC and RF characterized. An extrinsic transconductance, g_m, of 750 mS/mm was obtained for a 2x20 µm gate-width device (Fig. 3). S-parameters were measured on-wafer up to 50 GHz and an equivalent circuit was extracted. The extroplated maximum frequency of oscillation, f_{max}, was 225 GHz, and the extrinsic transit frequency, f_T, was 90 GHz. The pinch-off characteristics have been improved compared with earlier generations of metamorphic materials [3]. This is due to the improved buffer layers, and mainly the use of InAlAs instead of InGaAlAs in the graded buffer. The yield and uniformity has also been improved due to improved growth of the epi-layers and better surface morphology. The HFETs fabricated on this material show a high gate leakage current at high-gain bias voltages, compared to InP-based lattice matched materials. This results from a lower Schottky barrier as well as a lower conduction band offset (0.39 eV as compared with 0.53 eV for $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$), and can be reduced by lowering the In content in the barrier.

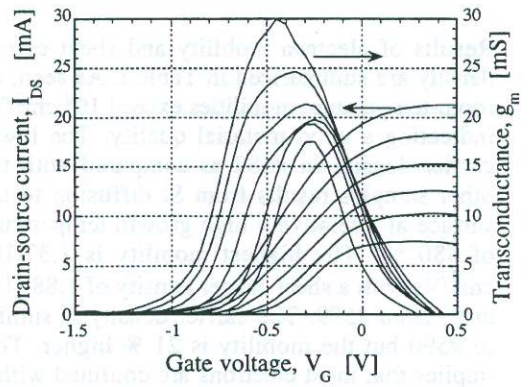

Figure 3. Drain-source current, I_{DS}, and extrinsic transconductance, g_m, for a 2x20 µm device on #589 (V_{DS}=0.25 - 1.5 V).

Summary

By using a linearly graded InAlAs buffer and a low growth temperature, high quality $In_{0.7}Al_{0.3}As/InAs/In_{0.8}Ga_{0.2}As$ modulation-doped heterostructures have been grown on GaAs by MBE. The minimum rms surface roughness value was 4-7 nm. Dislocations were mainly confined in the graded buffer and the maximum threading dislocation density was estimated to be in the order of 10^6 cm^{-2}. Electron mobility as high as $1.37 \cdot 10^4$ cm^2/Vs with a sheet carrier density of $1.88 \cdot 10^{12}$ cm^{-2} at 300 K was achieved. The 0.1 µm gate length HFETs fabricated on the structure with an inserted 4 nm thick InAs channel showed an extrinsic transconductance of 750 mS/mm, an extrinsic f_T of 90 GHz and an f_{max} of 225 GHz.

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