GaAs Application Specific MMICs for a HIPERLAN MCM

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Abstract

HIPERLAN (HIgh PErformance Radio Local Area Networks) is an emerging European standard for wireless local area networks with an in air data rate of 23.5 Mbits/sec. This paper details the design manufacture and measured performance of two application specific GaAs MMICs which form the majority of the 5.2 GHz RF front end. One MMIC is a power amplifier with level control and the other is an up/down-converter with on chip VCO. These are the first GaAs MMICs designed specifically for the HIPERLAN standard.

Introduction

Fig. 1 shows a block diagram of the RF to IF section of the HIPERLAN radio, of which the two GaAs MMICs form the main part. The MMICs will be incorporated into a Multi-Chip Module (MCM) designed and manufactured by GEC Plessey Semiconductors Ltd. The MCM silicon motherboard allows the compact integration of the various technologies employed in the radio onto a single substrate.

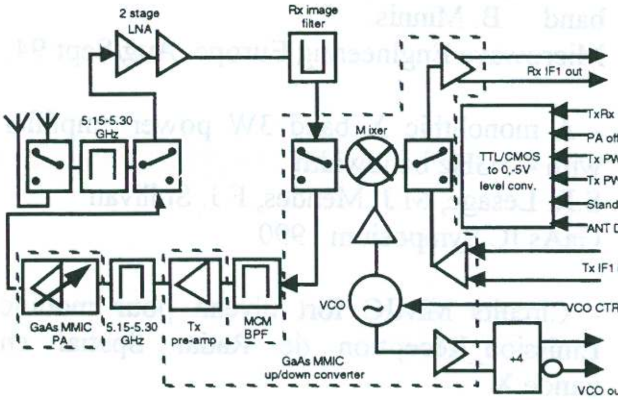

Fig. 1. HIPERLAN MCM Radio Block Diagram

The LNA utilises discrete HEMT die and MCM passive components to achieve a gain of 22 dB with a noise figure of 2 dB. This is used to buffer the noise figure of the down-converter. Standard product switches are used to realise the common port T/R switch and diversity antenna selection switch. Filters are also realised using MCM passive components.

The key parameters of the performance requirements of the two GaAs MMICs are given below.

Power Amplifier:		
Frequency	**5.15 to 5.3 GHz**	
Gain	**>16 dB**	
Return Losses	**>10 dB**	
1 dB CP	**>21 dBm**	
Psat	**23±2 dBm**	
Current	**<150 mA**	
Transceiver:		
LO	**5.80 to 6.05 GHz**	**1 - 4 V**
RF	**5.15 to 5.30 GHz**	
Rx Gain	**>-7 dB**	
Rx Noise Figure	**<22 dB**	
Rx Input IP3	**>10 dBm**	
Rx Current	**<50 mA**	
Tx Power Out	**>9 dBm**	**300 mV IF in**
Tx spurious	**<-63 dBc**	**4.88 - 5.55 GHz**
Tx current	**<200 mA**	

Both MMICs were fabricated using the standard GMMT F20 process, which utilises 0.5 μm gate length, depletion mode MESFETs. The simple 9 mask process is ideally suited to volume manufacture of MMICs.

Power Amplifier

Fig. 2 shows a photograph of the two stage power amplifier MMIC. The output stage is realised by two devices in parallel. A low gain / output power mode is available when an interstage attenuator is switched in. At the same time one of the two output stage FETs is pinched-off resulting in an output power reduction of around 10 dB with a 38% DC power consumption saving.

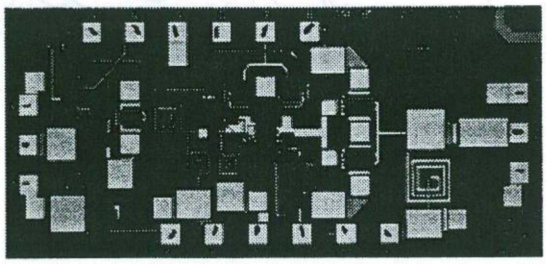

Fig. 2. Power Amplifier MMIC Photograph

The small signal S-parameters of a waferful of power amplifiers are plotted in Fig. 3. Gain is over 20 dB and both input and output return losses are greater than 17 dB. Fig. 4 shows the power transfer characteristics of a random sample of 24 amplifiers.

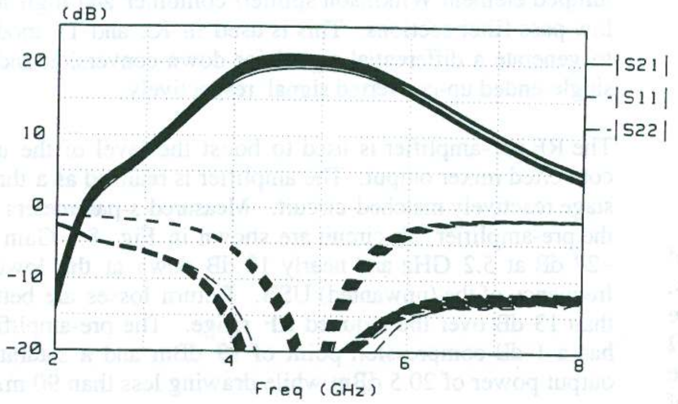

Fig. 3. Power Amplifier Measured S-parameters

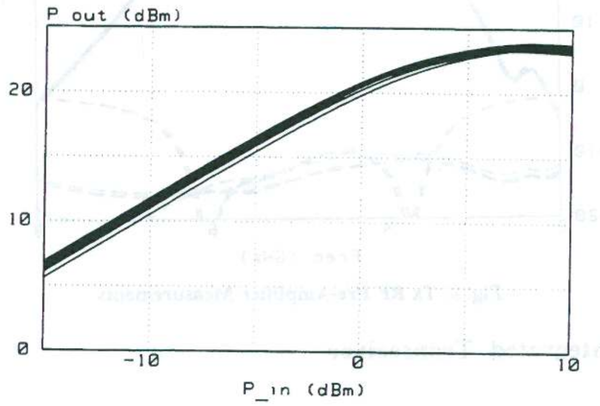

Fig. 4. Power Amplifier Power Transfer Characteristics

Transceiver Sub-circuits

As shown in Fig. 1, the transceiver MMIC comprises a VCO, buffer amplifier, mixer, RF balun, RF and IF Tx/Rx switches, Rx and Tx IF amplifiers and a Tx RF pre-amplifier. To minimise component count, the VCO, buffer, mixer and balun are used in both transmit and receive modes.

Following the MCM LNA and filter, the receive input signal is selected by the Tx/Rx switch and fed through the 180° splitter to the mixer. An IF amplifier provides the down-converted signal with gain and match to the high impedance external IF filter.

In transmit operation, an IF amplifier provides a high input impedance and gain prior to up-conversion using the same LO and mixer. The mixer RF output is converted to single-ended by the RF balun. The signal is then routed off chip for USB removal before returning to the pre-amplifier contained within the same chip.

Although the complete transceiver chip was fabricated in a single design pass, the majority of the sub-circuits were also manufactured on the same wafer by placement around the process control/ monitor (PCM) 5 site drop-in.

VCO / Buffer / Mixer

The on-chip Clapp-type VCO is fully self-contained and includes the resonator and tuning varactor. This push-pull device essentially comprises two separate oscillators connected and biased through virtual earths where a corresponding single-ended oscillator would have demanded RF grounding. The varactor tuning voltage is also applied at a virtual earth. The push-pull arrangement minimises on-chip RF decoupling requirements as well as providing the differential input to the double-balanced mixer. The tuning characteristics of several oscillators, covering the 5.5 GHz to 6.5 GHz frequency range, are shown in Fig. 5. Over the required 200 MHz bandwidth, the linearity of the VCO is better than 1.3:1. The VCO consumes approximately 25 mA.

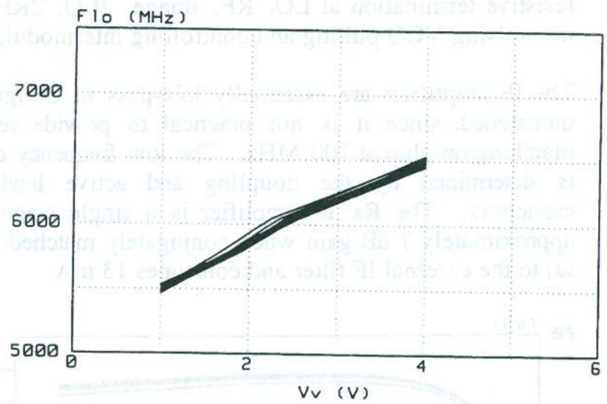

Fig. 5. VCO Tuning Characteristics

The buffer amplifier is required to provide a differential sample of the on-chip LO signal to allow external phase locking. It is required to isolate the VCO from the loading and possible pulling effects of the phase locked loop (PLL). Consisting of a long-tailed pair of small FETs, biased by a current source, no input matching is used in order that it presents a high input impedance to the VCO. Reactive matching is used at the output to provide a good match and thereby power gain. To allow a single-ended measurement of this differential amplifier, on-chip 50 Ω terminations were provided for the sub-circuit. The measured s-parameters of the buffer amplifier are shown in Fig. 6. With due allowance for the measurement arrangement, the recorded gain is ~0 dB but this is voltage gain, with very little load applied to the VCO. The current drawn by the buffer amplifier is ~7 mA.

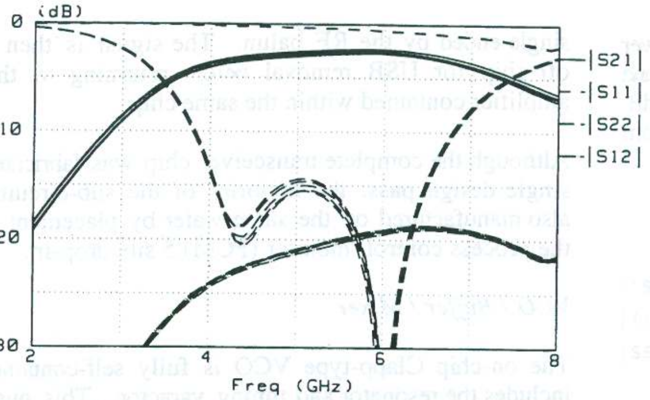

Fig. 6. VCO Buffer Amplifier Measurements

The double-balanced mixer is formed by a quad ring of FETs. With differential signals at RF, LO and IF ports, each port is a virtual earth of the other two. The gates are driven by the differential output of the VCO. A 200 Ω resistor across the LO input reduces the LO voltage available to the gates but reduces the pulling effect of Tx/Rx switching at the RF and IF ports.

Diplexer / IF Amplifiers

The IF side of the mixer is connected to the Tx/Rx switches by means of a diplexer filter. This assures a resistive termination at LO, RF, image, 2LO, 2RF etc., minimising VCO pulling and controlling intermodulation.

The IF amplifiers are essentially low-pass in design, i.e. unmatched, since it is not practical to provide reactive matching on-chip at 700 MHz. The low frequency cut-off is determined by the coupling and active load bias capacitors. The Rx IF amplifier is a single stage with approximately 7 dB gain when conjugately matched (~600 Ω) to the external IF filter and consumes 13 mA.

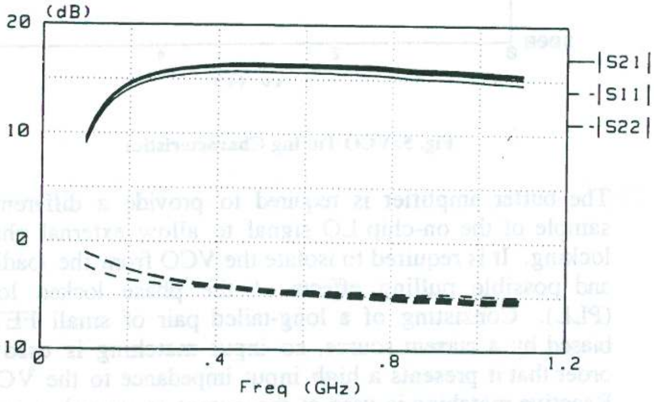

Fig. 7. Tx IF Amplifier Measurements

The Tx IFA is similar in design but has two stages with an inter-stage variable attenuator included to control the IF power into the mixer to ensure linearity. Differentially measured s-parameters of the Tx IF amplifiers are shown in Fig. 7. Allowing for the difference between the sub-circuit measurement system impedance and the amplifier input impedance, the IFA provides 18 dB gain; 13 dB of gain control is available by means of the voltage-variable attenuator. The Tx IF amplifier draws 63 mA and has a 1 dB compression point of just under 10 dBm.

RF Balun / Tx Pre-Amplifier

A 180° splitter/ combiner is formed by combination of a lumped element Wilkinson splitter/ combiner and high and low pass filter sections. This is used in Rx and Tx modes to generate a differential signal for down-conversion and a single-ended up-converted signal respectively.

The RF pre-amplifier is used to boost the level of the up-converted mixer output. The amplifier is realised as a three stage reactively matched circuit. Measured s-parameters of the pre-amplifier sub-circuit are shown in Fig. 8. Gain is ~27 dB at 5.2 GHz and nearly 10 dB down at the lowest frequency of the (unwanted) USB. Return losses are better than 13 dB over the required RF range. The pre-amplifier has a 1 dB compression point of 19 dBm and a saturated output power of 20.5 dBm while drawing less than 90 mA.

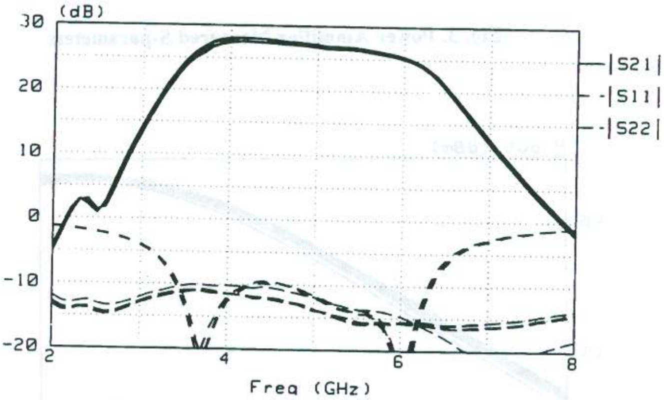

Fig. 8. Tx RF Pre-Amplifier Measurements

Integrated Transceiver

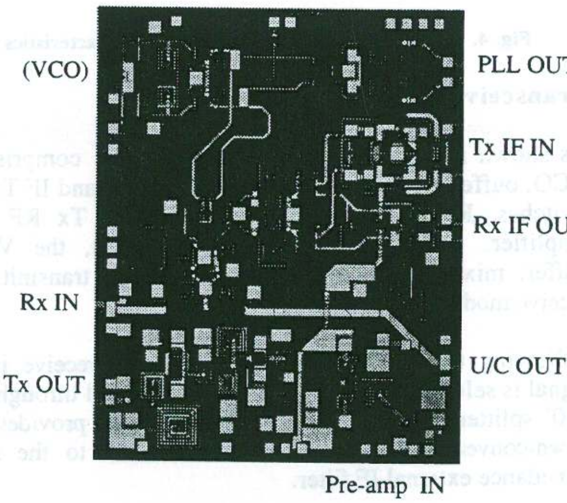

Fig. 9. Transceiver MMIC Photograph

The sub-circuits are interconnected into a single MMIC, Fig. 9. In addition to the RF sub-circuits described above, bias networks are included. These allow the Tx, Rx and common circuits to be independently enabled by means of single-ended 0/ -5 V controls at about 0.4 mA each when on. In the standby mode with all control inputs at -5 V, the total current drawn by the MMIC from the fixed +5 and -5 V supplies is < 1 mA and <0.2 mA respectively.

A consequence of the incorporation of the MMICs into MCMs is that full on-wafer RF measurement of the MMICs is necessary to select known good die. With the up/down-converter MMIC, a set of custom mixed RF and DC probes are used for this purpose. Differential probes are used to interface to the IF input and output. These are matched to a differential impedance of 200Ω. To reduce the number of separate measurements to be made, the up-converter output is connected to the pre-amplifier input by means of a track through the saw lane on the wafer. This track is severed at die separation, but allows the whole transmit chain to be checked with a single measurement at the wafer stage.

Figure 10 shows the buffered VCO output at the PLL port during operation of the transceiver MMIC. Phase noise was measured at -133 dBc/Hz at 10 MHz offset.

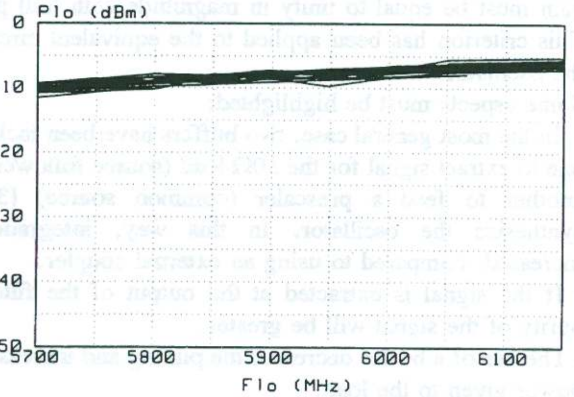

Fig. 10. Buffered VCO Output Power

The down-converter itself is designed to have conversion loss, Fig. 11 shows the conversion loss of 14 down-converters versus RF frequency, measured directly on wafer. Measured conversion loss is 8 dB, this improves to 6 dB when the IF outputs are conjugately matched, as will happen in practice.

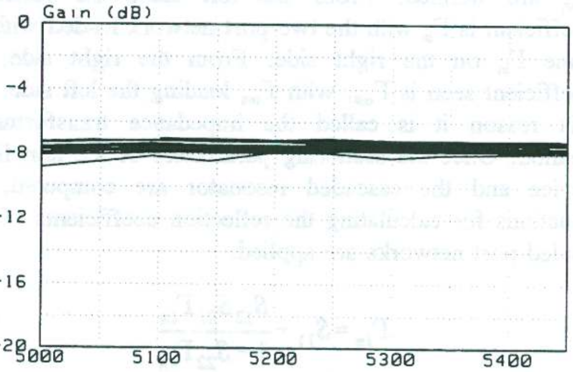

Fig. 11. Transceiver Rx Conversion Gain

In transmit mode, the up-converter has an output power of over 10 dBm for an input of -13 dBm. When integrated into the MCM, this output is filtered and is then used to drive the PA MMIC. After filtering there will still be sufficient power to drive the PA into saturation, providing +23 dBm of output power. Fig. 12 shows a typical output spectrum of the transceiver, without any additional filtering. All spurious signals are at least 20 dB below the wanted signal, with the LO at -28 dBc. This is a reflection of the excellent balance of the VCO and mixer. In band spurious signals are at -70 dBc which is due to both a good choice of IF frequency (resulting in only very high order spurs. falling in-band) and the IF amplifier operating sufficiently linearly so as not to generate large harmonic tones.

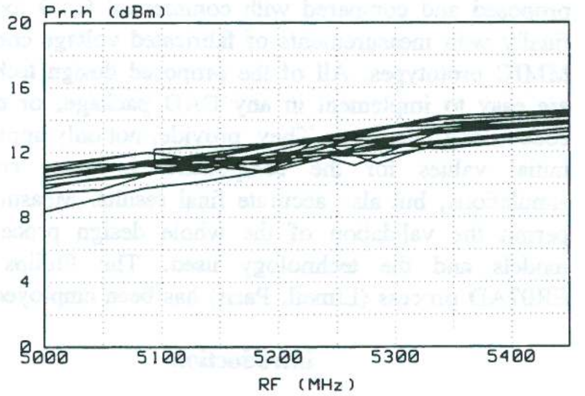

Fig. 12. Transceiver Tx Output Power

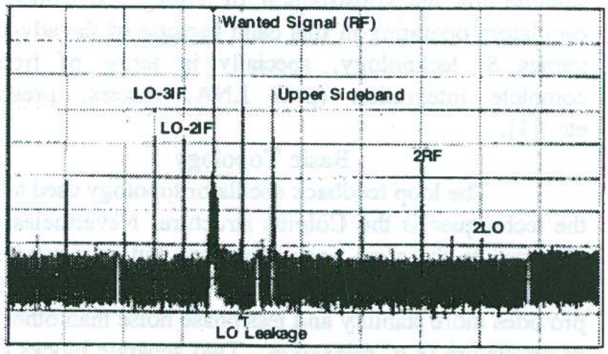

Fig. 13. Transceiver Output, 0 to 15 GHz

Conclusions

A power amplifier and highly integrated transceiver MMICs have been manufactured in a single design cycle. The functionality of the sub-circuits is very close to the target requirements with the result that the integrated transceiver operates to specification. On-wafer measurement of circuit RF functionality allows selection of known good die for incorporation into a Multi-Chip Module.

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