Correlation between permanent degradation of GaAs-based HEMT's and current DLTS spectra

Gaudenzio Meneghesso, Alessandro Paccagnella
Dipartimento di Elettronica e Informatica, Università di Padova
Via Gradenigo 6a, 35131 Padova, Italy

Youcef Haddab
Institut de Microsystems, Swiss Federal Institute of Technology, EPFL,
1015 Lausanne, Switzerland

Claudio Canali, Enrico Zanoni
Dipartimento di Scienze dell' Ingegneria, Università di Modena
Via Campi 213, 41100 Modena, Italy

I. ABSTRACT

In this paper we report on the hot-electrons induced degradation in AlGaAs/GaAs HEMT's and AlGaAs/InGaAs/GaAs PM-HEMT's, consisting in a decrease in the drain current. We have found that the amount of the degradation is correlated to to the impact-ionization in the channel, which is related to the electron energy. Creation of traps is the degradation mechanism which has been found to be responsible for the observed I_d degradation. Drain current DLTS (Deep Level Transient Spectroscopy) analyses and transconductance frequency dispersion measurements have been used to identify properties and localization of these traps. These techniques appear to be a powerful tool to study the reliability problems arising in HEMT structures due to defect created by hot electrons.

II. INTRODUCTION

Oxide and interface damage due to hot electrons and hot holes has been extensively studied in short-channel Si MOS transistors, where hot electron effects represent a crucial reliability problem despite the scaling of bias voltages, since channel lengths are projected in the $0.1\mu m$ range. Since III-V microwave FET's do not adopt a gate oxide, hot electron degradation has usually been considered negligible in these devices, and little attention has been devoted to the possible damage induced by hot carriers at passivation/semiconductor and semiconductor/semiconductor interfaces. Nevertheless, High Electron Mobility Transistors (HEMT's) currently adopted for power microwave amplifiers have channel lengths in the $0.15\mu m \div 0.3\mu m$ range, with drain-source voltages V_{ds} which can easily exceed 5 V. At these bias levels, extremely high electric fields are present in the gate-drain access region, and significant hot-electron phenomena have been observed, such as light emission [1] and increase in negative gate current I_g (due to holes, generated by impact-ionization and collected at the gate electrode) [2]. All these effects demonstrate the presence of highly energetic carriers which can eventually result in device breakdown or degradation.

This paper reports on the permanent degradation of the electrical characteristics of GaAs-based HEMT's and PM-HEMT's following to hot-electron stress. We demonstrate that the failure mechanism involved consists in the creation of deep levels either in the gate region or at the AlGaAs/GaAs interface in the access region between gate and drain. The nature of these deep levels has been analyzed by means of transconductance dispersion and drain current DLTS measurements. Transconductance and DLTS results are correlated here for the first time with hot-electron induced HEMT's degradation.

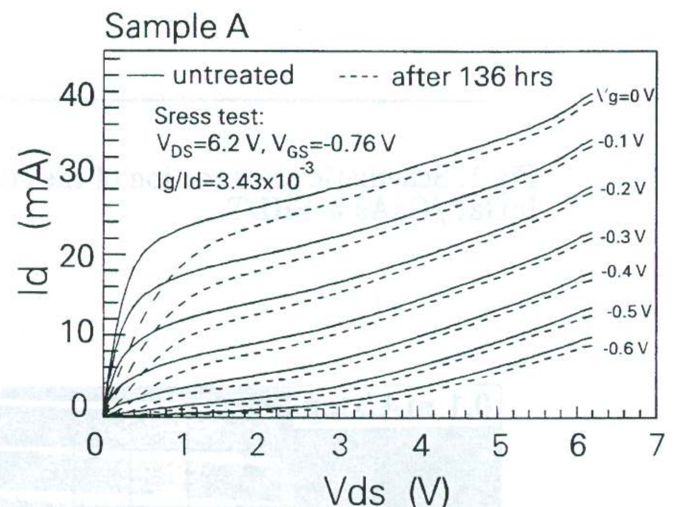

FIG. 1. I_d vs V_{ds} before and after 136 hrs. of stress at V_{DS} = 6.2 V and V_{GS} = −0.76 V for samples '**A**' devices.

III. DEVICES AND EXPERIMENTAL RESULTS

Tested devices are: i) commercially-available 0.3 μm AlGaAs/GaAs HEMT's, hereafter identified as samples '**A**', adopting an n-doped $Al_{0.3}Ga_{0.7}As$ layer, and an AlGaAs/GaAs superlattice buffer layer [3]; and ii) 0.25 μm $Al_{0.2}Ga_{0.8}As$/InGaAs double-heterojunction power pseudomorphic HEMT's with superlattice buffer layer, hereafter identified as samples '**F**'.

Devices have been submitted to various dc tests at room temperature, with V_{DS} exceeding 5 V. At these

recovered by annealing up to 250°C for 24 hours. The failure mechanism consists in the creation of deep levels under the gate, which act as electron traps at low gate-to-drain electric fields. At high V_{ds}, this negative charge can be either compensated by holes generated through impact-ionization, or removed by field-assisted detrapping or tunneling, thus causing the kink. These traps are located under the gate electrode and give rise to a shift in the device threshold voltage, Fig.6. This shift is consistent with the presence of additional negative charge trapped under the gate. In order to characterize these traps, low frequency ac measurements have ben carried out.

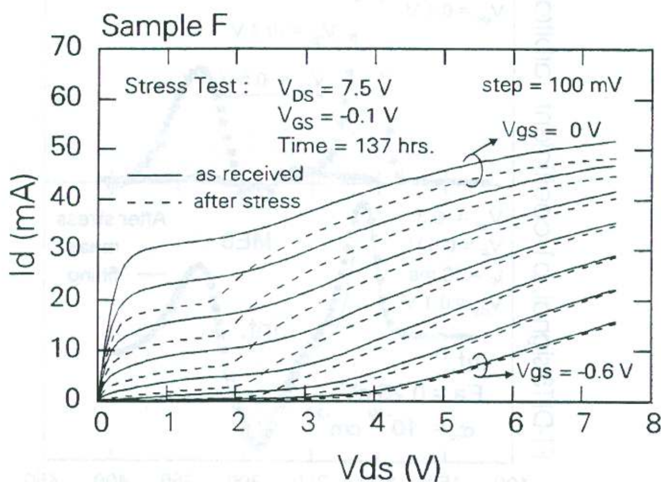

FIG. 5. I_d vs V_{ds} before and after 137 hrs. of stress at V_{DS} = 7.5 V, V_{GS}=-0.1 V for samples 'F devices.

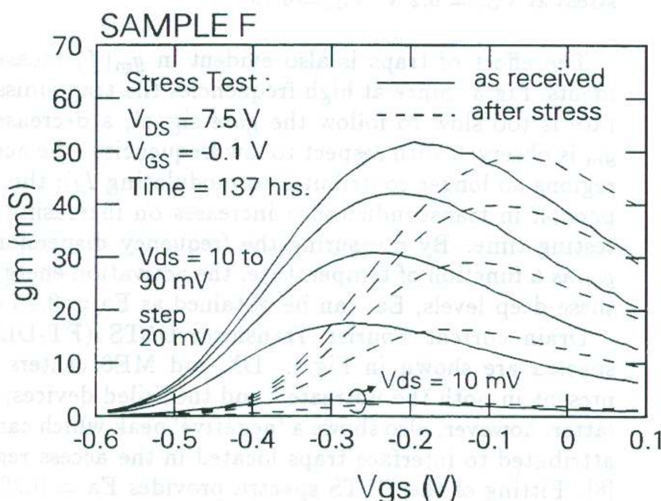

FIG. 6. g_m vs V_{gs} before and after 137 hrs. of stress at V_{DS} = 7.5 V, V_{GS}=-0.1 V for samples 'F devices.

Figure 7 represents the device transconductance, $g_m(f)$ measured at $V_{ds} = 2\ V$ (corresponding to the kink in the output characteristics) for devices submitted to different hot-electron tests. It can be seen that, on increasing V_{DS} in the hot-electron test, the frequency dispersion of g_m increases. This $g_m(f)$ behaviour suggests the creation of deep levels under the gate as a possible cause of the degradation itself; since the gate signal modulates both the charge in the channel and the charge trapped on these levels, the transconductance at low frequency is lower than the one measured at high frequency, when the traps can no longer follow the signal, see Fig.7 [9].

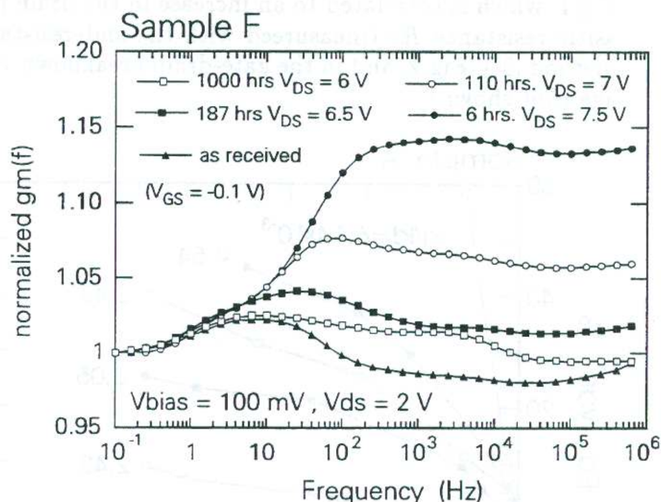

FIG. 7. Normalized $g_m(f)$ measured at V_{ds} = 2 V in a samples 'F' devices before and after various stress test.

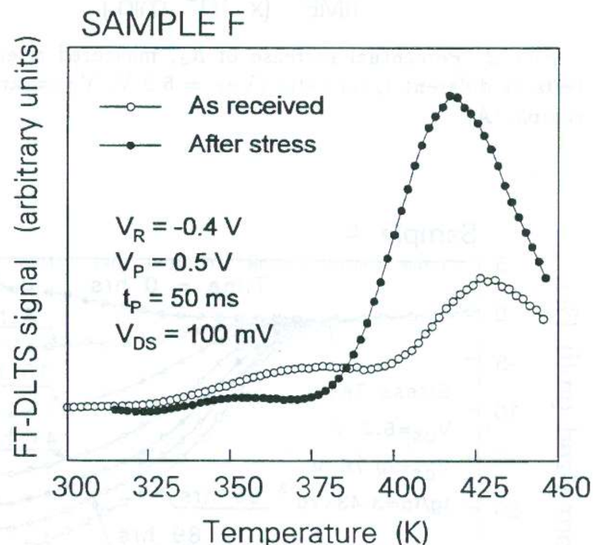

FIG. 8. Drain current FT-DLTS measurement, for samples 'F' devices, in an as-received device and in a device after the stress at V_{DS} = 7.5 V, V_{GS}=-0.1 V.

When negatively charged, these traps cause the observed shift in pinch-off voltage in linear region (see fig. 6) and the I_d decrease in the low V_{ds} part (see Fig.5) as above discussed. At high V_{ds}, three effects can contribute to detrap or compensate the trapped electrons: (i) hot electrons can impact-ionize traps, thus releasing the negative trapped charge [10]; (ii) the high electric field existing between the gate and the channel can directly detrap the electrons; (iii) holes, generated by impact-ionization, can be captured by hole traps or can neutralize trapped

V_{DS} values, hot-electron effects and impact-ionization take place. Generated holes are collected by the gate electrode, giving rise to a negative gate current I_g [4]. After hot-electron tests devices exhibit a rapid degradation, which is not observed during high temperature storage tests (275°C) without bias.

For samples '**A**' the degradation consists in a decrease of I_d both in the linear and in the saturation region, Fig.1, which is correlated to an increase in the drain parasitic resistance R_d (measureed with the end–resistance method [5]), Fig.2, and in the gate-drain breakdown voltage (not shown).

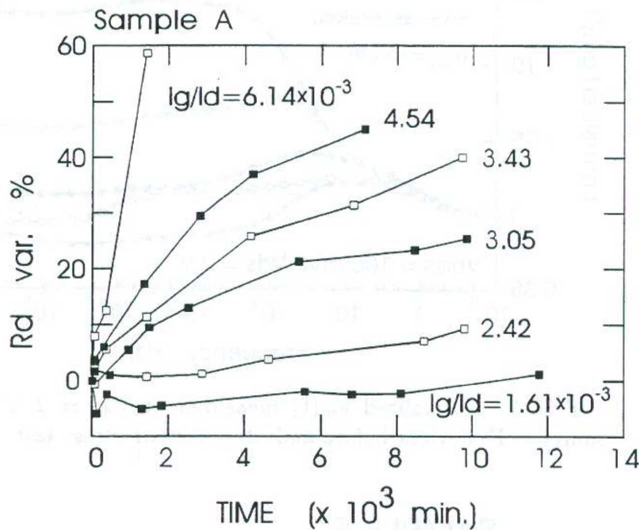

FIG. 2. Percentual increase of R_d, measured after stress tests at different I_g/I_d ratio (V_{DS} = 6.2 V, V_{GS}=var.) in a sample '**A**'.

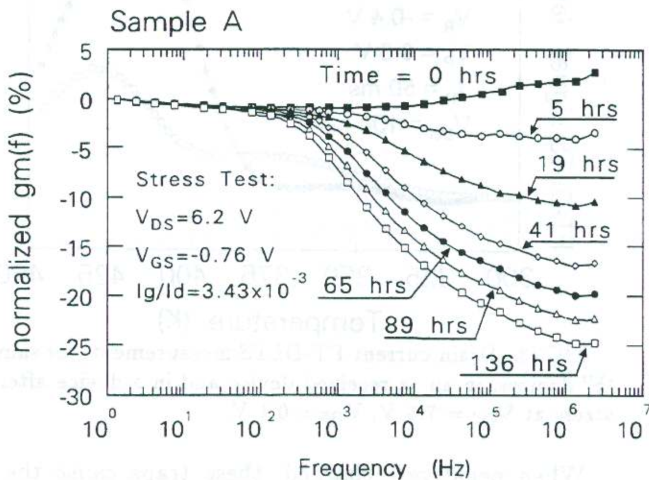

FIG. 3. Trasconductance frequency dispersion, gm(f), during the stress test at V_{DS} = 6.2 V, V_{GS}=-0.76 V in a sample '**A**'.

Source resistance and gate-source breakdown voltage remain unchanged. Various bias conditions have been adopted during accelerated tests; the amount of I_d and R_d degradation result to be proportional to the I_g/I_d ratio measured during the tests, which is proportional to the impact-ionization rate and is related to the channel electron energy [6].

In samples '**A**', hot electrons generate deep levels in the access region between gate and drain. These traps, when charged, reduce the channel width and increase R_d, thus reducing I_d. They also lower the longitudinal electric field and lead to higher gate-drain breakdown voltages [7].

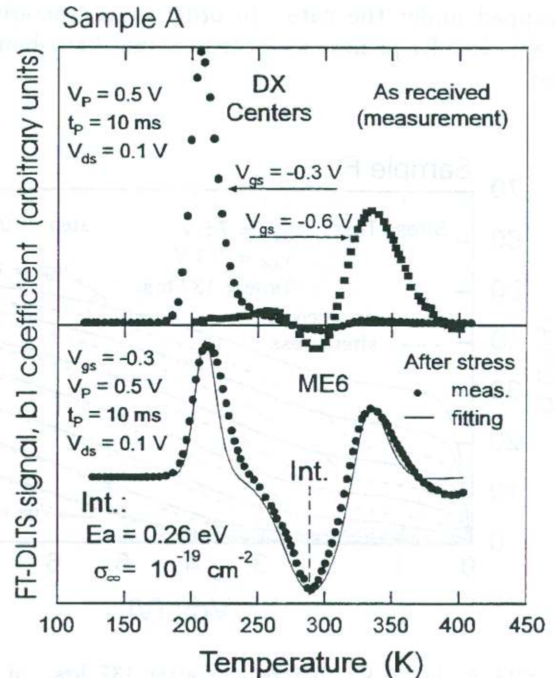

FIG. 4. Drain current FT-DLTS measurement, for samples '**A**' devices, in an as-received sample and in a sample after the stress at V_{DS} = 6.2 V, V_{GS}=-0.76 V.

The effect of traps is also evident in $g_m(f)$ measurements, Fig.3. Since at high frequencies the trap emission rate is too slow to follow the gate signal, a decrease in g_m is observed with respect to low frequencies (the access regions no longer contributes to modulating I_d); the dispersion in transconductance increases on increasing the testing time. By measuring the frequency dispersion of g_m as a function of temperature, the activation energy of these deep levels, Ea, can be obtained as Ea = 0.26 eV.

Drain current Fourier Transform DLTS (FT-DLTS) spectra are shown in Fig.4. DX and ME6 centers are present in both the untreated and the failed devices; the latter, however, also shows a 'negative' peak which can be attributed to interface traps located in the access region [8]. Fitting of the DLTS spectra provides Ea = 0.26 eV for interface traps, with a cross-section $\sigma = 10^{-19}\text{cm}^2$. The intensity of this negative peak is correlated with the amount of the degradation and with the transconductance dispersion.

In samples '**F**', hot electron tests induce a decrease in I_d at low V_{ds}, followed by a kink, see Fig.5. This is the first observation of the generation of a kink in the I-V characteristics of a HEMT induced by hot electron aging. The degradation is permanent, and can not be

electrons thus compensating them. In all cases, the consequent result is a sudden increase in the drain current, which causes a kink in the output characteristics (see Fig.5).

Current DLTS spectra (Fig.8) of untreated devices reveal in this case two peaks, corresponding to Ea = 0.77 eV and 1.22 eV, already observed in [11]. Hot electron testing induced a remarkable increase in the density of the 1.22 eV peak, which is proportional to the threshold shift.

IV. CONCLUSIONS

Significant degradation of GaAs based HEMT's and PM-HEMT's can be induced by hot-electrons stress test consisting in:

(a) for samples 'A (AlGaAs/GaAs HEMT's) a decrease in the drain current and an increase in the parasitic drain resistance. The amount of the degradation has been found to be proportional to the ratio of the gate current to the drain current, i.e. to the impact-ionization generation rate, which is related to the electron energy. Transconductance dispersion measurements and current DLTS analysis identify interface traps, possibly located at the AlGaAs/GaAs interface, in the gate-drain access region as the cause of the observed degradation. These traps are generated by hot-carriers, as demonstrated by the increase in the transconductance dispersion during accelerated tests, and by the appearance of a big 'minority-carrier' peak in DLTS spectra. DLTS and $g_m(f)$ results are correlated, indicating an activation energy Ea = 0.26 eV for the traps, and a cross-section of about 10^{-19}cm^2;

(b) for samples 'F'a permanent decrease of I_d in the low V_{ds} part of the output characteristics and the formation of a kink are observed, which are related to the creation of additional electrons traps under the gate during hot electron stress at high V_{DS}. Experimental data also suggest that traps are not created in the source/drain access regions of the device, but rather under the gate or close to it. This is confirmed both by $g_m(f)$ measurements and by the absence of any increase in the source and drain parasitic resistances after the tests. The increase in trap density due to hot-electron tests in samples 'F' has been confirmed by low frequency and drain current DLTS measurements. Frequency trasconductance dispersion increases after hot-electron stress tests, confirming the creation of additional deep-levels.

The present work also demonstrates that trasconductance frequency dispersion and drain current DLTS measurements are a powerful tools for the analysis of failure mechanisms of GaAs-based HEMTs due to deep levels generation. The determination of the origin of the observed interface traps requires further study in order to correlate trap features with device fabrication and aging characteristics.

ACKNOWLEDGMENTS

We wish to acknowledge the support of INFM (Istituto Nazionale di Fisica della Materia).

[1] E. Zanoni, A. Paccagnella, P. Pisoni, P. Telaroli, C. Tedesco, C. Canali, N. Testa and M. Manfredi, "Impact Ionization, Recombination, ans Visible Light Emission in AlGaAs/GaAs High Electron Mobility Transistors", *Journal of Applied Physics*, vol. 70, n. 1, pp. 529–531, July 1991.

[2] C. Canali, A. Paccagnella, P. Pisoni, C. Tedesco, P. Telaroli and E. Zanoni, "Impact Ionization Phenomena in AlGaAs/GaAs HEMT's", *IEEE Transactions on Electron Devices*, vol. ED–38, n. 11, pp. 2571–2573, November 1991.

[3] C. Canali, F. Magistrali, M. Sangalli, C. Tedesco, E. Zanoni, G. Castellaneta and F. Marchetti, "Reliability Aspects of Commercial AlGaAs/GaAs HEMTs", *IEEE/IRPS 91*, pp. 206–213, 1991.

[4] E. Zanoni, M. Manfredi, S. Bigliardi, A. Paccagnella, P. Pisoni, C. Tedesco and C. Canali, "Impact Ionization and Light Emission in AlGaAs/GaAs HEMT's", *IEEE Transactions on Electron Devices*, vol. ED–39, n. 8, pp. 1849–1857, August 1992.

[5] K. Lee, M. S. Shur, A. J. Valois, G. Y. Robinson, X. C. Zhu and A. Van Der Ziel, "A New Tecnique for Characterization of the "End" Resistance in Modulation-Doped FET's", *IEEE Transactions on Electron Devices*, vol. ED–31, n. ED–10, pp. 1394–1398, October 1984.

[6] A. Neviani, C. Tedesco, E. Zanoni, C. Canali, M. Manfredi and A. Cetronio, "Impact Ionization and Light Emission in GaAs Metal-Semiconductor Field Effect Transistors", *Journal of Applied Physics*, vol. 6, n. 6, pp. 4213–4220, September 1993.

[7] P. H. Ladbrooke and S. R. Blight, "Low-Field Low-Frequency Dispersion of Transconductance in GaAs MESFET's with Implication for Other Rate-Dependent Anomalies", *IEEE Transactions on Electron Devices*, vol. ED–35, n. 3, pp. 257–267, March 1988.

[8] M. Takikawa, "Electrical Properties of Interface-Traps in Selectively Doped AlGaAs/GaAs Heterostructures", *Japanese Journal of Applied Physics*, vol. 26, n. 12, pp. 2026–2032, December 1987.

[9] C. Canali, F. Magistrali, A. Paccagnella, M. Sangalli, C. Tedesco and E. Zanoni, "Trap-Related Effects in AlGaAs/GaAs HEMTs", *IEE Proceedings-G*, vol. 138, n. 1, pp. 104–108, February 1991.

[10] L. Partain, D. Day and R. Powell, "Metastable Impact Ionization of Traps Model for Lock-On in GaAs Photoconductive Switches", *Journal of Applied Physics*, vol. 74, n. 1, pp. 335–340, July 1993.

[11] P.M. Mooney, R. Fischer and H. Morkoç, "Transient capacitance study of electron traps in AlGaAs grown with As$_2$", *J. Appl. Phys.*, vol. 57, n. 6, pp. 1928–1931, 1985.