# A 2-18 GHz Monolithic Matrix Amplifier for Low Power Consumption Applications

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## Abstract

In this paper we present a (2x5) matrix amplifier with a DC power consumption as low as 200 mW with 13 dBm of RF output power (@1 dB compression point) achieving 7 dB of small-signal gain (residual ripple 0.3 dB) and input-output return loss always better than -14 dB. Designed using the *LN05* monolithic process of Thomson Composants Microondes (TCM), the amplifier employs ten MESFETs of 160 µm (4x40 µm) gate width and sub-micron (0.5 µm) gate length, for a total chip area of 2.5x3.5 $mm^2$. Broadband performance and very low power consumption make this amplifier very well suited for high-volume realization of monolithic multiple-stage front-ends in integrated high bit-rate fiber-optic receivers.

## Introduction

The principle of distributed amplification, based on coupling input and output capacitances of the transistors with lumped or distributed inductors so as to form artificial transmission lines [1], has been widely demonstrated [2]: the amplifier can be designed to give a flat, low-pass response up to very high frequencies. It is possible to achieve both additive and multiplicative amplification paralleling two or more distributed amplifiers in a way that resembles the distribution of elements in an array: hereafter the name of matrix amplifier (fig. 1) [3-6].

This construction is very compact and offers circuits with higher gain per unit area (lower power consumption), better input-output return loss and noise figure, than can be obtained with conventional cascaded multistage distributed amplifiers. Using monolithic technology the higher costs and lower reliability problems associated with the use of a relatively large number of active devices in hybrid realizations are completely overcome.

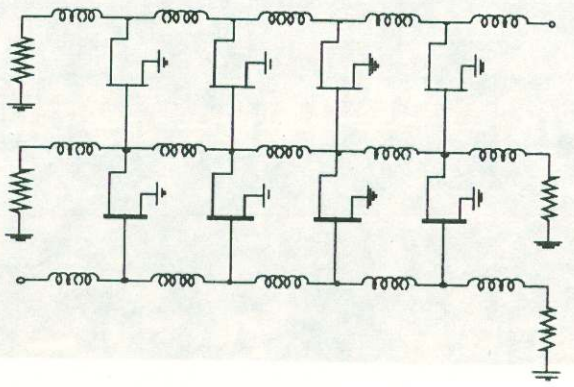

Fig. 1 Schematic of the 2x4 Matrix Amplifier.

## Circuit design and realization

Following previous analyses [7-8] a 2x5 matrix amplifier has been designed, optimizing small-signal gain flatness and input-output return loss. The circuit was designed at ESTEC (European Space Agency Technology and Research Center, Noordwijk, The Netherlands) and realized using the *LN05* process of Thomson Composants Microondes GaAs foundry process. A photograph of the chip is shown in fig. 2. Main features of TCM process are: selective ion implantation, submicrometer gate length, E-beam gate lithography, a Ti/Pt/Au metallization system, silicon nitride passivation and via holes through the substrate for improved high frequency performance and minimal bonding. The *LN05* process is specifically designed for small-signal

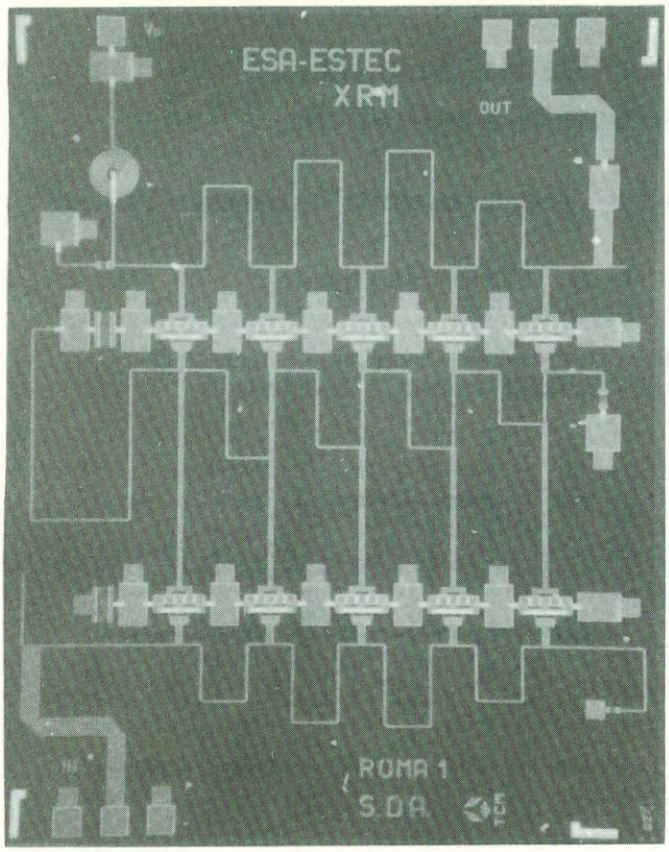


Fig. 2 Photograph of the monolithic matrix amplifier.

and low noise applications up to 18 GHz. We chose 4 fingers MESFETs (each finger 40 μm wide) with $g_m$ = 21 mS, $C_{gs}$ = 150 fF, $C_{gd}$ = 32 fF, $C_{ds}$ = 45 fF, $R_{ds}$ = 300 Ω and $R_i$ = 5.7 Ω. Low noise performance (2.2 dB @12 GHz) and high cutoff frequency (29 GHz) enabled us to design a broadband, low power consumption amplifier, without compromising gain and matching design targets. Direct masking on an electron beam machine features 0.5 μm gate length and provides better gate alignment in the drain source space of the FETs. The same process allows the choice between two implantation levels so as to choose low-power, low-noise FETs or medium power FETs. The one we chose is the so-called *I1* with activation energy and doping levels, respectively, of 150 keV and $6x10^{12}$ atoms/cm$^2$ (layer N) and 250 keV and $6x10^{12}$ atoms/cm$^2$. Metal coated via-holes are 40 μm wide (with a 80x80 μm collar) and result in a series resistance as low as 0.03 Ω. Previous realizations of monolithic matrix amplifiers suffered from the high drain current necessary to bias the several transistors employed (in the order of hundreds of milliamperes [9,10,11]). Using a self-biasing scheme (fig. 2) we achieve a two-fold objective: simple bias network and only one external bond to correctly bias ten FETs. Thus, in contrast to preceding realizations [10-11], the whole biasing network is integrated on the chip (fig. 2). RF blocking is achieved through series spiral inductor and Metal-Insulator-Metal (MIM) shunt capacitor grounded through via-hole. Even if it results in a higher area occupation, this greatly simplifies implementing two or more cascaded stages in low-power, low-weight satellite subsystems: very low power consumption and very good input and output matching allows us to attain even better performances as compared to other single-stage solutions employing external bias networks [10-11]. Other realizations of matrix amplifiers required four termination resistors at the idle ports of the artificial transmission lines [3-4]. We found that, with a careful layout and design it is possible to eliminate one of them in the central line without affecting input and output matching figures, simplifying both layout and biasing scheme. The elimination of this resistor contributes to lower power consumption and improves noise figure performance.

Distributed inductors needed in Π artificial transmission lines are realized by means of 10 μm wide microstrip lines. Narrow lines are preferable to achieve higher impedance values with shorter lines and thus lower RF attenuation and smaller chip area occupation: low bias currents allow us to employ lines with only 60 mA DC current maximum (10 μm). In designing line paths we had to maintain chip size as small as possible while minimizing line coupling: according to TCM foundry manual [12] we can neglect coupling when distances between adjacent lines are above 200 μm (e.g., above double of substrate height, 100 μm).

## Experimental results

The experimental results (obtained at the ESTEC XRM section) for the monolithic matrix amplifier, shown in figs. 3 and 4, are obtained on a Cascade Station using HP 8510B

Network Analyzer and Noise Meter Station. Probe pads are included at input/output ports for on-wafer measurements. The DC power consumption is as low as 200 mW ($V_d$ = 4.85 V and $I_d$ = 41 mA). A small-signal gain of 7 ± 0.3 dB and a maximum input-output return loss of -14 dB are recorded over the whole 2-18 GHz band.

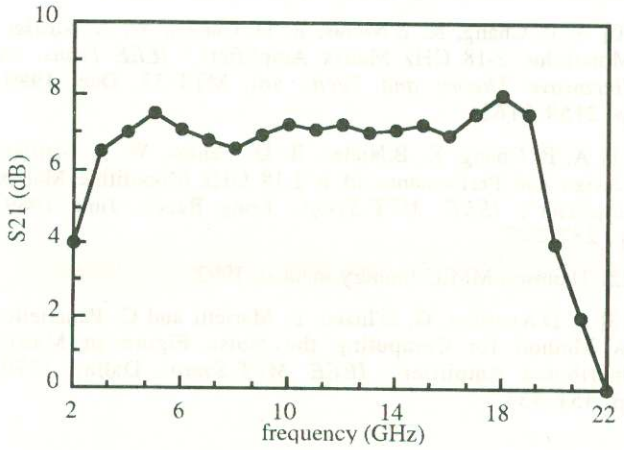


Fig. 3 Measured gain of the amplifier.

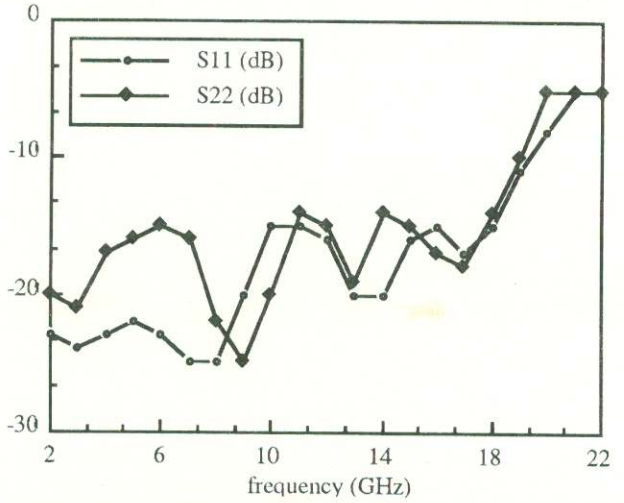


Fig. 4 Input-output reflection coefficients.

This amplifier has the characteristic noise performance of a distributed amplifier [13] as shown by the curve in fig. 5.
It shows a high noise figure at low frequencies due to the gate termination resistor. The noise figure near the cutoff frequency rises because of increasing impedance of the transmission line as the cutoff is approached. In the mid band, the amplifier has the lowest noise figure.
Output power, at 1 dB compression point, is 13 dBm with intermodulation ($IM_3$) better than 20 dBc at the frequency of 13 GHz.

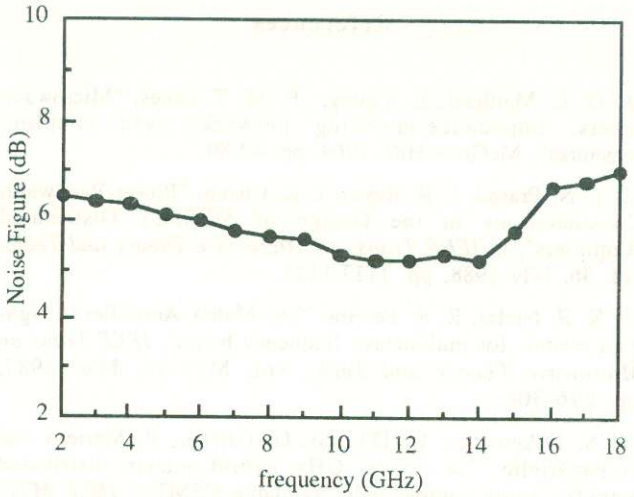


Fig. 5 Measured Noise Figure.

Such a low distortion in matrix amplifiers follows from previous analyses [8] and encourages to look for better power performances of MMIC matrix amplifiers.
The results obtained are excellent considering that were derived using MESFET's that do not represent the up to date devices.

## Conclusion

In this paper we described the measured performances of a 2x5 monolithic matrix distributed amplifier. Broadband operations up to 18 GHz are obtained using a 0.5 μm gate length technology. To avoid coupling effects we had to keep chip area relatively large. Electromagnetic simulations allowing better confidence in circuit simulations than usual microwave tools would result in a smaller chip design. However, very low power consumption, minimal external bonding and excellent input-output matching, make this amplifier well suited for mobile systems, where low manufacturing costs and low power operations are main design goals.
The experimental results recorded across the 2-18 GHz frequency band proved that this amplifier can be a very powerful competitor to the equivalent two-stage distributed amplifier.

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