An Experimental All-GaAs 10 Gbit/s Synchronous Transmission System for Optical Fibers

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Abstract

An experimental 10 Gbit/s system, based on synchronous 155.52 Mbit/s channels was implemented with the aid of monolithic integrated GaAs circuits and a thorough going applied hybrid thinfilm technology. The combination of digital and microwave circuits proved to be necessary and successful. The system can be used both for measuring and testing purposes as well as for an experimental insertion to the existing network of Deutsche Bundespost Telekom.

Introduction

For more than one decade there has been a rather continuous trend in optical communication systems towards high and highest bit rates. Systems with bit rates below 1 Gbit/s, based mainly on plesiochronous input signals, have been installed in a great number all over the world. The next higher level of hierarchy, which is 2.5 Gbit/s, was fixed for synchronous transmissions for the range of Deutsche Bundespost Telekom (STM 16, this means 16 input and output channels, 155,52 Mbit/s each). Several prototypes of 2.5 Gbit/s systems were fabricated by different German companies and were carefully and comprehensively tested for the purpose of the project "Berlin V". Furthermore, in 1991, an experimental 5 Gbit/s system for synchronous transmission channels was built up at the Telekom Research Center in a tentative time-division multiplexing technic for investigations of broadband optical transmission links. In 1992, first tests with an experimental 10 Gbit/s system (exact bit rate: 9.95328 Gbit/s) were initiated [1]. This system has been improved in the meantime and turned into a compact and reliable measuring and transmission equipment [2].

Processing of bit rates in the 10 Gbit/s range makes it needful to combine the monolithic integrated GaAs-circuits and a hybrid thinfilm technology as it is well known from microwave integrated circuits. Circuitry and layout have to be in accordance with both the demands of digital and microwave technics. And under some circumstances the microwave technic may become the dominating factor. Problems such as parasitic propagation delay times, unintentional coupling between adjacent lines or components, resonances of unmatched lines, inductivities of bond wires, mismatchings, reflections at line crossings and bends or at the inevitable junctions between micro-striplines and coaxial connectors have to be avoided. On the other hand, it can be very advantageous to apply proved microwave components to a digital design, as e.g. couplers, transforming lines, phase shifters or open stubs.

The tendency of the last years has shown that monolithic GaAs circuits were favourized for analog microwave applications while the range of high speed digital circuits was occupied by monolithic bipolar Silicon circuits which unfortunately even until today are not commercially available; but since the middle of 1992 first members of a 10 Gbit/s GaAs family (NEL) came to the market. Therefore the described experimental system could be built up by using exclusively such circuits.

Experimental System

A. Transmitter

Figure 1 shows the block diagram of the transmitting part. The two commercial STM 16 systems (STM 16A and STM 16B) are driven by 622 MHz clock signals which are phase locked to each other and obtained by dividing the 10 GHz output signal of a quartz stabilized oscillator by sixteen. This oscillator can be synchronized to a 155,52 MHz network standard frequency. A pseudo random generator working at 2.5 Gbit/s produces two output signals which are pattern correlated and combined with the two STM 16 signals by means of the first multiplexer (MUX 10) into a 10 Gbit/s-channel. This multiplexing is done bit by bit and, therefore, all signals faster than 2.5 Gbit/s are no standard signals with regard to the Synchronous Digital Hierarchy (SDH). But

this is absolutely unimportant for the case the experimental system was developed for. This signal is pulse shaped and jitter reduced by a last D-flipflop (DFF) and the connection to the laser diode is done via a laser-driver chip, which was developed by Fraunhofer Institute for Applied Solid-State Physics, Freiburg, Germany [3]. All circuits working at bit rates equal or higher than 2.5 Gbit/s are monolithic integrated GaAs-circuits.

The experimental system has to work also with plesiochronous input signals (139 Mbit/s) to make it as versatile as possible. Therefore, two STM 16 systems, fabricated by PKI, Nürnberg, were chosen to generate two standard basic signals at 2.5 Gbit/s (exact bit rate: 2.48832 Gbit/s). They are able - by manipulating hardware and software switches - to accept the plesiochronous input signals (139.264 Mbit/s, relating to CCITT Rec. G 703) as well as the synchronous input signals (155.52 Mbit/s, CMI, bit rate tolerance +/-20 ppm). From the system-capacity of 10 Gbit/s 50 percents are used for communication purposes. The other 50 percents are simulated by pseudo random signals to reduce cost, size, and increase the complexity of the experimental system.

B. Receiver

The optical part (from laser driver to laser diode and from photo diode to transimpedance amplifier) shall not be dealed with this paper. The amplified output signal of the photo diode is the input signal for the receiver (Fig. 2). An active power divider (consisting of two parallel driven buffer circuits with push-pull outputs) controls both the clock recovery circuit and the demultiplexer (DMX 10). The clock recovery circuit consists of an EXOR-gate to differentiate the NRZ-signal, a dielectric resonator and a smallband amplifier (a PLL-solution is under development). The demultiplexer splits the 10 Gbit/s signal into four 2.5 Gbit/s channels, two of them are the input signals for the STM 16 receivers (STM 16A and STM 16B). The other two signals are used for error rate measurements and for channel synchronizing of the receiver.

Fig. 3 gives the details of the regenerator, demultiplexer and signal processing module, which is the fastest digital part of the receiver. The buffer-ICs are used as amplitude regenerator and drivers for the demultiplexer and the EXOR-gate. This gate is applied for signal processing of the NRZ-data signal to obtain a straight spectral line at the bit repetition frequency of 10 GHz. This results from connecting the two inputs of this gate to one push-pull output of the buffers, where one signal is delayed by half the bit duration (50 ps). The push-pull output signals of the EXOR-gate are added in a 180^{o}/3dB coupler and fed to the high-Q filter of the clock recovery circuit.

Figures 4 and 5 show two examples of typical modules with GaAs-circuits in flat-packs. Fig. 4 is a printed circuit board which serves as a carrier for the ceramic-filled Teflon-substrate with the flat-packs. Interconnections between the circuits and the coaxial connectors are realized by 50 Ohm micro-striplines. This type of mounting is useful up to some Gbit/s. For bit rates of 10 Gbit/s and beyond mainly ceramic substrates with thinfilm layer structures should be preferred. Fig. 5 shows the hardware of the receiver input module (see Fig. 3). The flat-pack at the lower left is the input buffer circuit, the larger IC at the right hand side is the 1:4-demultiplexer. The rotated IC is the EXOR-gate. The unequal length of the input lines which produces the 50 ps delay can be seen. At the upper left one finds the 10 GHz/180^{o} coupler.

Summary

The paper shows, that by the use of commercial GaAs-circuits it is possible to develop a reliable and small-sized transmission system for 10 Gbit/s and experimental and also operational application for a fiber transmission system.

References

[1] Hanke, G.: Signal Processing at 10 Gbit/s with Si-ICs for Optical Communication Systems. Proc. 3rd Intern. Symp. on Recent Advances in Microwave Technology, 1991, pp 574-577

[2] Hanke, G.: Experimental Synchronous 10 Gbit/s Transmission System for Optical Fibers. Proc. 1993 SBMO International Microwave Conference Brazil, Sao Paulo, Aug. 1993, pp 657-662

[3] Wang, Zhi-Gong, et.al.: Integrated Laser-Diode Voltage Driver for 20-Gb/s Optical Systems Using 0.3-/um Gate Length Quantum-Well HEMT's. IEEE Journal of Solid-State Circuits, Vol. 28, No. 7, July 1993, pp 829-834

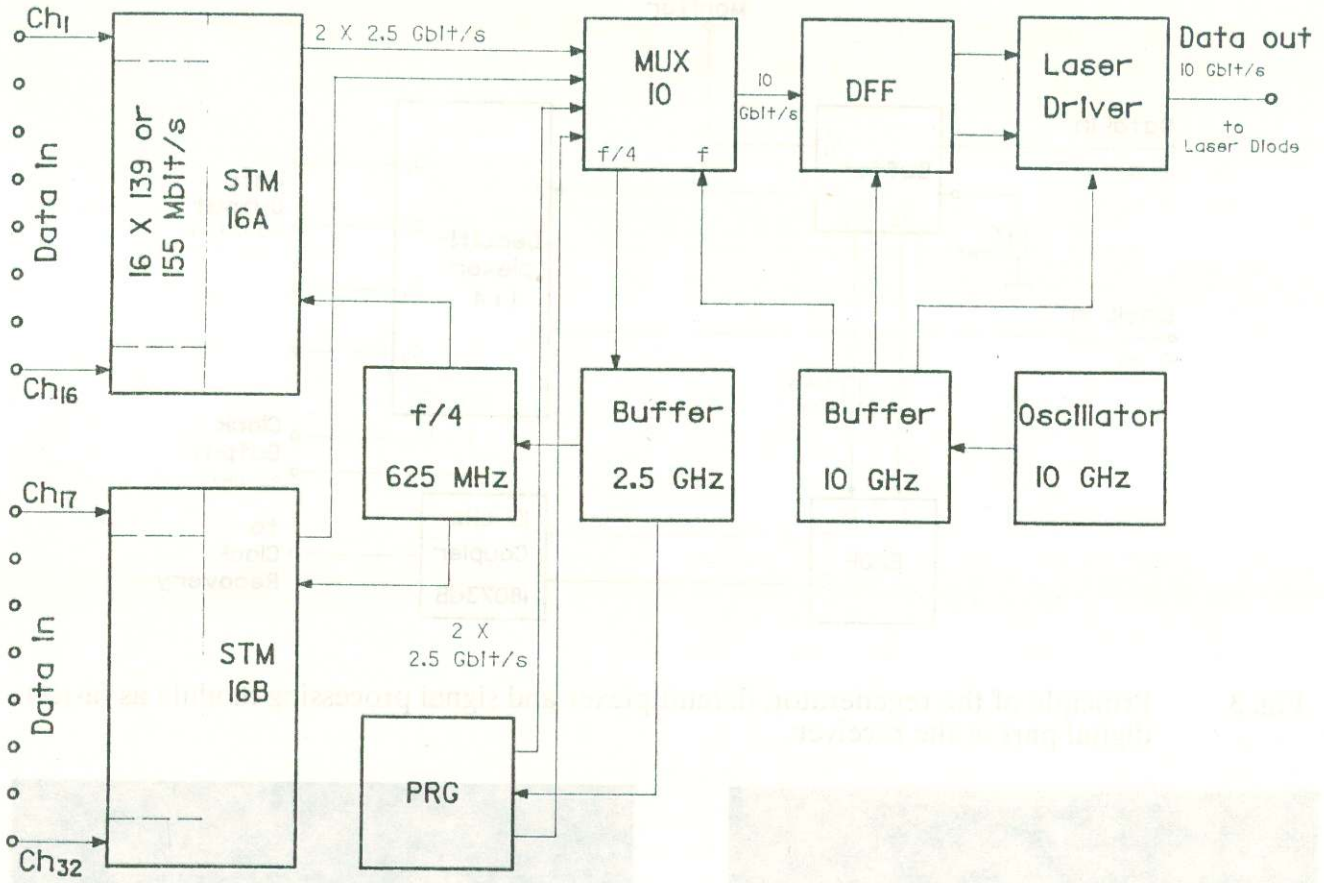

Fig. 1 Block diagram of the experimental 10 Gbit/s transmitter
Two STM-16 systems and a pseudo random generator with 2.5 Gbit/s output channels are used as signal sources

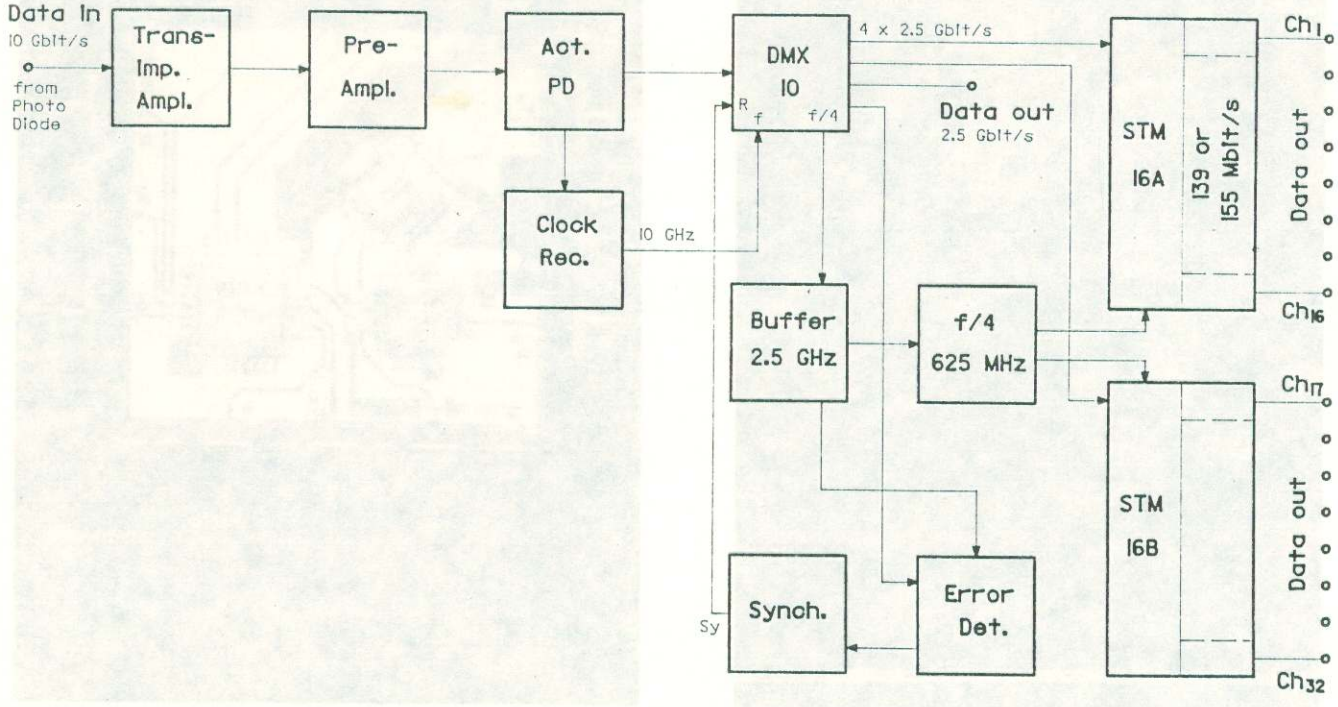

Fig. 2 Block diagram of the experimental 10 Gbit/s receiver
For transmission, 32 synchronous (or plesiochronous) channels of 155 (or 139) Mbit/s are accessible. Synchronization is done by use of one pseudo random signal.

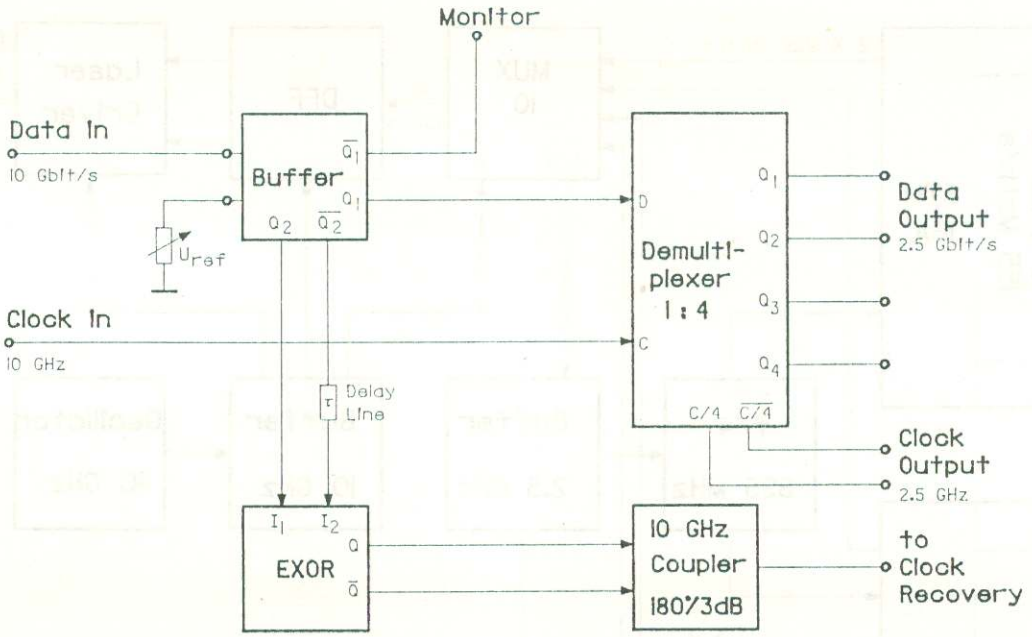

Fig. 3 Principle of the regenerator, demultiplexer and signal processing module as fastest digital part ot the receiver

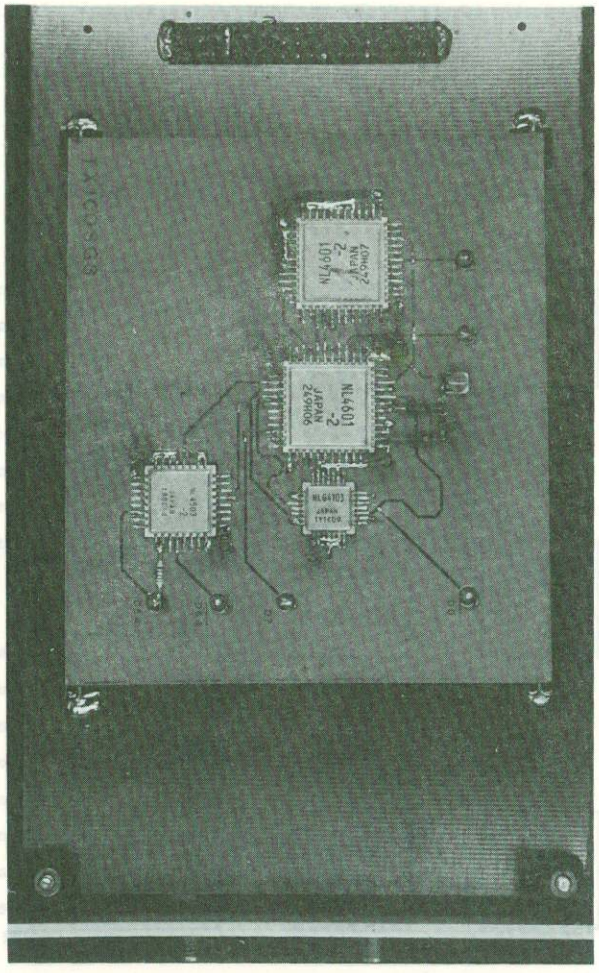

Fig. 4 PCB as carrier for a ceramic-filled Teflon substrate with four GaAs-ICs (PRPS-generator for 2.5 Gbit/s)

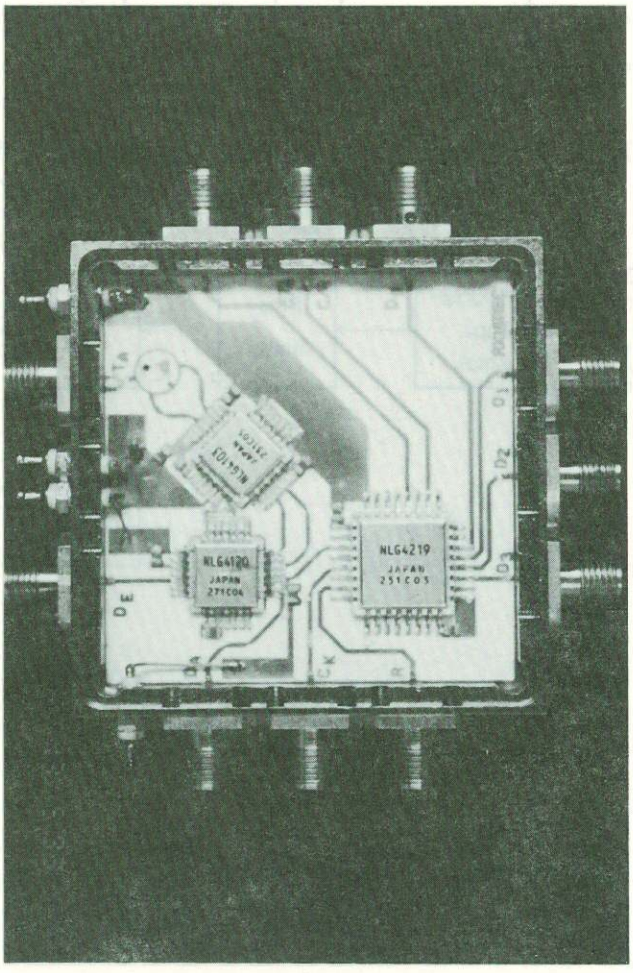

Fig. 5 Receiver module in a microwave package for 10 Gbit/s, as shown in Fig. 3