EXPERIMENTAL EXTRACTION OF EQUIVALENT SCHEME FOR DUAL GATE FIELD EFFECT TRANSISTORS

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Abstract

The purpose of this paper is to describe a new method that we have developped to determine accurately all the elements of dual gate FET equivalent scheme. The parasitic and intrinsic elements are separately determined by biasing the DGFET in 'cold' and 'hot' regime. Some new results about 0.15µm dual gate PM-HEMT, obtained from on-wafer three-ports S-parameters measurements in the 1.5-26.5 GHz range, are presented.

Introduction

Dual gate HEMT can constitute the basis of very promising circuits in the millimeter frequency range. The design of such circuits like amplifiers or mixers needs to dispose of an accurate model based on an experimental extraction of electrical parameters. We have chosen to develop an experimental characterization which gives directly electrical parameters rather than usual S-parameters acquisitions followed by computer optimization (like simplex, multidimensional gradient and random search), because of large numbers of elements. Indeed, the principle of these computer optimization techniques is to minimize an error function EF defined by :

$$EF = \sqrt{\sum_{fk}\sum_{i,j} \frac{\left|Sij_{meas} - Sij_{calc}\right|^2}{\sum_{fk}\sum_{i,j}\left|Sij_{meas}\right|^2}}$$

(i,j)=(1,2,3) k=1..10
(as used in [1]).

With a lot of variables, the global minimum of EF becomes difficult to reach and, sometimes, the found solution does not fit the physical reality.
In order to characterize such devices, a three-ports measurements set-up has been realized in our laboratory, using a specific system of switches between a conventional HP8510 network analyzer and a Cascade Microtech probes system [2]. On-wafer S-parameters measurements are performed from 1.5 to 26.5 GHz.

Equivalent scheme of dual gate transistor

The study of the main physical parameters inside the structure of a dual gate transistor shows that the average electric field remains low between the two gates along the longitudinal axis, and consequently, potential variation is not important in this intergate zone (Fig. 1). These results have been obtained by using a simplified quasi-two-dimensional simulation tool (Helena) developped in our laboratory [3]. It clearly appears that the dual gate FET can be considered as two equivalent single gate transistors in cascode configuration, while the intergate distance is much larger than about 0.2µm. Fig. 2 presents the entire equivalent scheme of the DGFET which is deduced by combining two single gate FET models : parts A and B are related to the intrinsic part of each equivalent transistor and the rest being composed of parasitic elements like access resistances, inductances, pad and coupling capacitances. This kind of complex equivalent circuit has already been used by Tsironis [1]. In order to extract all 27 electrical parameters, our method can be divided in two sequences of several steps in which the parasitic and intrinsic parameters are successively determined.

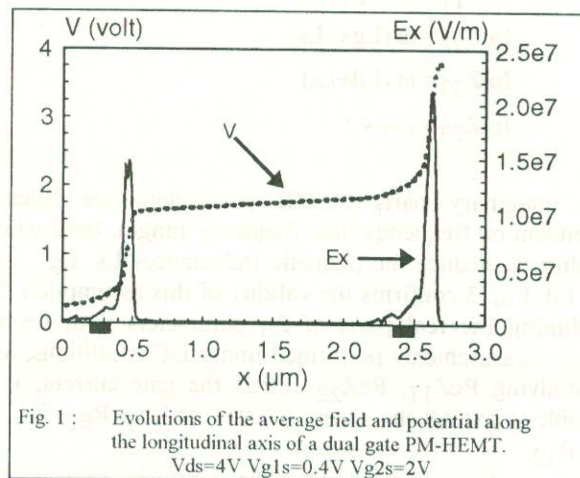


Fig. 1 : Evolutions of the average field and potential along the longitudinal axis of a dual gate PM-HEMT.
Vds=4V Vg1s=0.4V Vg2s=2V

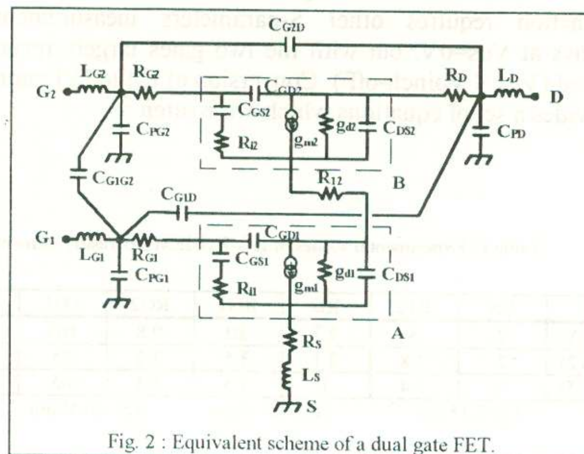


Fig. 2 : Equivalent scheme of a dual gate FET.

Extraction of parasitic elements

In the first sequence, the dual gate FET is always under 'cold' regime (at Vds=0V) in order to switch off the active behaviour, and so, to emphasize only effects of the parasitic elements. In addition, the two gates are biased in a similar way, in order to be sure that no potential appears in the intergate zone, and so, the two equivalent transistor remain under 'cold' regime. In these conditions, the intrinsic scheme under each gate can be very simple and easy to evaluate [4].

• In the first step, the device under test with the two gates being forward biased, allows to bring out the effects of serie parasitic elements, like access resistances and inductances. It can be shown, by neglecting capacitances in the low frequency range, that the Zij impedance parameters are written as follow ($port_1=gate_1$, $port_2=gate_2$, $port_3=drain$) :

$$ReZ_{11}= Rs+Rg_1+Rdy_1+Rc/3$$
$$ReZ_{22}= Rs+Rg_2+Rdy_2+4Rc/3+R_{12}$$
$$ReZ_{33}= Rs+Rd+2Rc+R_{12}$$
$$ReZ_{12}= Rs+Rc/2$$
$$ReZ_{23}= Rs+3Rc/2+R_{12}$$

Rdy_i=dynamic resistance of Schottky diode i

$$ImZ_{11}= \omega.(Lg_1+Ls)$$
$$ImZ_{22}= \omega.(Lg_2+Ls)$$
$$ImZ_{33}= \omega.(Ld+Ls)$$
$$ImZ_{23}= \omega.Ls$$

The imaginary parts of Zij parameters are linearly dependent on frequency (low frequency range), from which we directly deduce the parasitic inductances Ls, Lg_1, Lg_2 and Ld. Fig. 3 confirms the validity of this assumption. By combining the real parts of Zij parameters with several others measurements performed under DC conditions, and by studying ReZ_{11}, ReZ_{22} versus the gate current, it is possible to extract the access resistances Rg_1, Rg_2, Rd, Rs and R_{12}.

• In a second step, the extrinsic capacitances extraction requires other S-parameters measurements, always at Vds=0V, but with the two gates largely reverse biased (Vgs < Vpinch-off). Conversion of [S] to [Y] matrix provides a set of equations which are written :

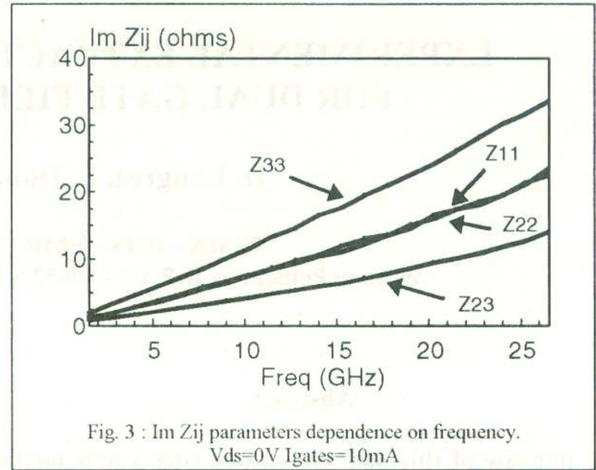


Fig. 3 : Im Zij parameters dependence on frequency. Vds=0V Igates=10mA

$$ImY_{11}= \omega.(Cpg+3Cb/2+Cg_1g_2+Cg_1d)$$
$$ImY_{22}= \omega.(Cpg+3Cb/2+Cg_1g_2+Cg_2d)$$
$$ImY_{33}= \omega.(Cpd+Cb+Cg_1d+Cg_2d)$$
$$ImY_{31}= - \omega.Cg_1d$$
$$ImY_{21}= - \omega.(Cb/2+Cg_1g_2)$$
$$ImY_{32}= - \omega.(Cb+Cg_2d)$$

In these relations, Cpg and Cpd represent, respectively, the pad capacitances of gates and drain ; Cg_1d, Cg_2d and Cg_1g_2 are coupling capacitances between each pair of electrodes and Cb is the edge capacitance related to the depleted zone under each gate. All these parallel elements are simply deduced from the linear variations of the Yij imaginary parts versus frequency (Fig. 4). On table I are summarized several typical values of parasitic elements obtained for different 0.15 µm dual gate PM-HEMTs fabricated by Thomson TCS. Scaling rules versus W are verified for the access and even the intergate R_{12} resistances. The presence of source and drain air bridges

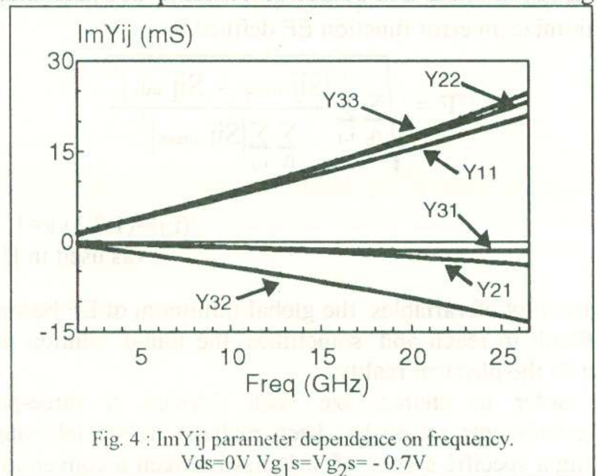


Fig. 4 : ImYij parameter dependence on frequency. Vds=0V $Vg_1s=Vg_2s=$ - 0.7V

Table I : Experimental values of DG-PMHEMT parasitic elements. R(Ω) L(pH) C(fF)

	RS	R12	RD	RG1	RG2	LG1	LG2	LD	LS	CPG	CPD	CG1G2	CG1D	CG2D
(1)	2	3	2.3	10	9.8	100	100	65	20	35	50	2	10	20
(2)	2	2.8	2.1	3.5	3.2	45	45	105	55	40	45	3	15	20
(3)	1	1.4	1	3.5	3.3	65	65	105	45	40	70	4	15	25

Lg=0.15µm (1) : 1x150µm (2) : 3x50µm (3) : 3x100µm

on the multi-fingers gates devices increases the value of source and drain inductances. It can be noticed that, in fact, two source air bridges are in parallel on the 3x100μm device, but only one on the 3x50μm device ; that clearly explains the inequality $Ls_{3x100\mu m} < Ls_{3x50\mu m}$. All results are in good agreement with theoretical predictions considering gate configurations and device topology.

Extraction of intrinsic elements

In the second sequence, the intrinsic elements of each equivalent single gate transistor are separetely extracted. S-parameters are systematically de-embedded from known parasitic elements previously determined, in order to acceed to the active and intrinsic part of the device. This means that the accuracy of intrinsic results depends on quality of the extrinsic elements extraction ; also the first sequence requires the greatest care.

- The first step consists to characterize the equivalent single gate FET B. This requires to build previously the static composite characteristics Id=f(Vds) of the dual gate transistor (Fig. 5). These characteristics represent the variation of DC current Id in the structure versus internal biases of each partial single gate device and for a constant drain bias :

$Id=f(Vd_1s)$ with Vg_1s = constant

$Id=f(Vdd_1)$ with Vg_2d_1 = constant

D_1 is an arbitrary floating point, considered as a pseudo-drain for FET A or pseudo-source for FET B, and logically chosen in the middle of intergate zone. By denoting the relationship $Vg_2s=Vg_2d_1+Vd_1s$, it is possible to know accurately if equivalent single gate FETs are under their saturate or linear regime for any external bias (Vg_1s, Vg_2s and Vds). This property is used to shift FET A in ohmic regime (low Vd_1s) without changing internal bias of FET B. In these conditions, S-parameters are performed between $gate_2$ and drain while $gate_1$ is closed on 50Ω load, and by applying a similar method so that developped for single gate devices [5], all the elements of FET B can be extracted.

- Finally, in order to determine the intrinsic elements of FET A, in this second and last step, it would be interesting to proceed in a similar way ; in word, shifting FET B in ohmic regime without modifying internal bias of FET A and performing S-parameters two-ports measurements between $gate_1$ and drain electrodes. Unfortunately, the effect of $gate_2$ cannot be neglected and then, this principle can also not be applied in this particular case. On the contrary, by considering the cascode configuration (Fig. 6), it can be shown that a very simple relationship exists between the three-ports Zij impedance parameters and the two-ports Zij parameters of each equivalent single gate FET [6] :

$$[Z] = \begin{bmatrix} Z_{11}^A & Z_{12}^A & Z_{12}^A \\ Z_{21}^A & Z_{22}^A + Z_{11}^B & Z_{22}^A + Z_{12}^B \\ Z_{21}^A & Z_{22}^A + Z_{21}^B & Z_{22}^A + Z_{22}^B \end{bmatrix}$$

Three of the four two-ports parameters of FET A (Z_{11}^A, Z_{12}^A and Z_{21}^A) are given explicitly, and the fourth Z_{22}^A is simply added to each impedance parameter of FET B.The determination of intrinsic elements for the A equivalent transistor becomes obvious. Indeed, three-ports S-parameters measurements are performed, the dual gate being biased in a usual way. As FET B has been previously characterized, the conversion of [S] to [Z] matrix after de-embedding, allows the knowledge of two-ports Z^A_{ij} parameters, and consequently to the intrinsic equivalent scheme of FET A deduced from $[Y]^A$ admittance matrix. Here is summarized a diagram of this step of extraction :

(1) $[S]_{3x3\ \text{usual bias}} \Rightarrow [Z]_{3x3}$

(2) $[Z]_{3x3} - [Z]^B_{2x2\ \text{previously determined}} \Rightarrow [Z]^A_{2x2}$

(3) $[Z]^A_{2x2} \Rightarrow [Y]^A_{2x2} \Rightarrow$ FET A

Typical results: A 0.15 μm dual gate PM-HEMT has been characterized with this procedure at Vds=3V, Vg_2s=1V and $gate_1$ bias being varied. On-wafer S-parameters were performed from 1.5 to 26.5 GHz. It can be remarked by referring to the static composite characteristics (Fig. 5), that the potential of the internal point D_1 changes with Vg_1s bias, but the two equivalent FET remain in their saturate regime. Their internal DC biases are modified at the same time following two ways, when Vg_1s changes. Vg_1s and Vg_2d_1 vary in the same way, on the contrary Vd_1s and Vdd_1 vary in opposite way (because Vds=constant). These variations show the complex behaviour of the dual gate transistor, and they have to be taken into account while reading results. Here are

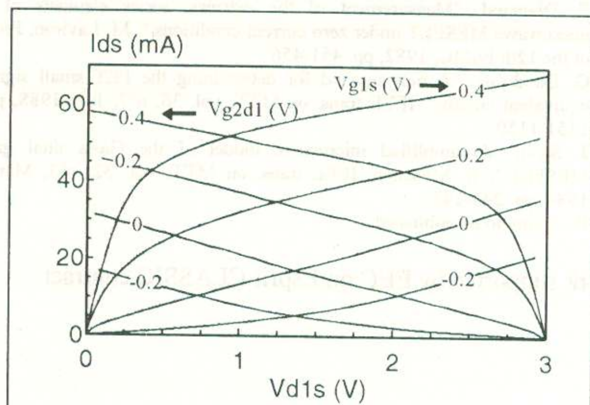


Fig. 5 : Static composite characteristics of a dual gate PM-HEMT Lg=0.15μm W=3x50μm Vds=3V

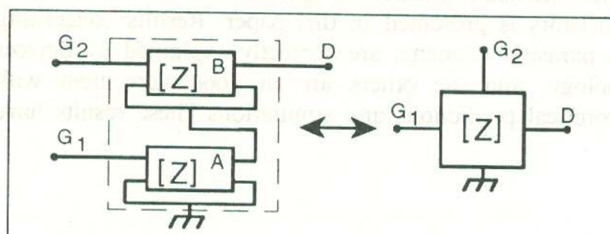
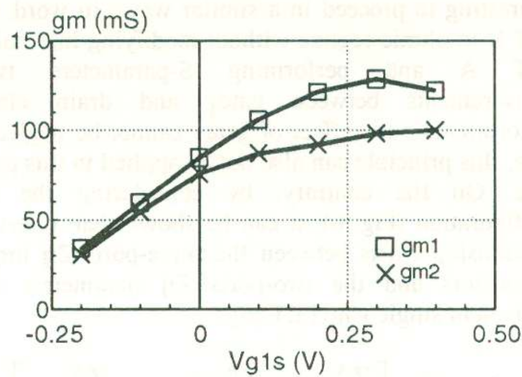


Fig. 6 : Representation of a dual gate FET by considering two two-ports networks in cascode configuration



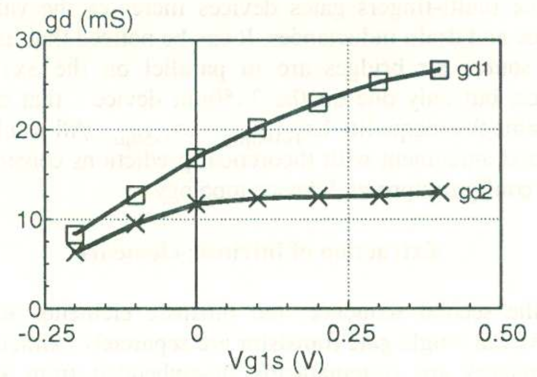
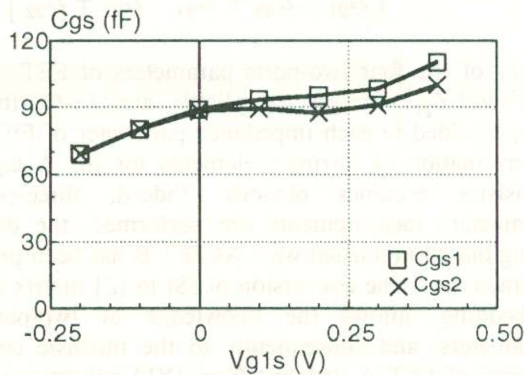


Fig. 7 : Intrinsic transconductances gm and output conductances gd versus Vg1s
DG-PMHEMT Lg=0.15μm w=3x50μm Vds=3V Vg2s=1V



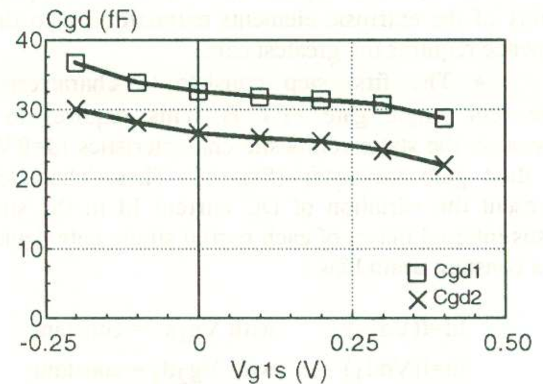


Fig. 8 : Input gate capacitances Cgs and feedback capacitances Cgd versus Vg1s
DG-PMHEMT Lg=0.15μm w=3x50μm Vds=3V Vg2s=1V

presented the variations of the eight most important intrinsic parameters of the dual gate transistor versus Vg_1s bias : transconductances, output conductances, input gate capacitances and feedback capacitances (Fig. 7 and Fig. 8). General evolutions are in good agreement with theoretical predictions and with results obtained for 0.15μm single gate PM-HEMTs. This clearly indicates the validity of our extraction method and the high level of performance that can be obtained by using these devices : for instance, the intrinsic current gain cut-off frequency ($gm/2\pi Cgs$) may reach 200 GHz, that is very promising for millimeter applications. All the results can be easily interpreted, for instance, the increase of output conductance gd_1 for positive Vg_1s values can be understood by considering that the first equivalent transistor approaches its ohmic regime.

Conclusion

A new method to extract the equivalent scheme of dual gate transistors is presented in this paper. Results concerning the parasitic elements are correctly explained by devices topology, and the others are in good agreement with theoretical predictions and simulations. These results have been used for electrical modelling in order to design a mixer in millimeter frequency range [5].

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