PHYSICAL SIMULATION: A TOOL FOR TECHNOLOGICAL EVALUATION AND OPTIMIZATION OF GAAS MESFET DEVICES

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Abstract. *The paper presents a case study on the technological optimization of GaAs MESFETs by means of a two-dimensional physical DC and small-signal simulator (MESS). Two examples are discussed, the first concerning the dose and recess optimization of an analog device, the second, the recess optimization of a MESFET series or parallel switch.*

Introduction

Gallium arsenide field-effect transistors (MESFETs) with gate lengths in the range 0.3-1 μm are today the most commonly used active element for hybrid and monolithic MICs up to $\approx$ 20 GHz. Analog devices have reached technological maturity; in other words, all *simple* means to improve their performances have been exploited. However, considerable space is left open by new and often more complex solutions, based e.g. on the combined use of several implanted profiles and of the recessed gate technology. On the other hand, the design of devices for advanced, non-conventional applications, such as MESFET switches [1], poses optimization goals which are fairly unusual whith respect to the analog case, thereby leaving more space to performance improvements.

Owing to the moderately large number of parameters influencing the design of a technologically complex device (e.g. a double-implant recessed-gate MESFET [2] or a p-buried layer recessed-gate MESFET) the designer's insight has to be supported either by experiment or by the less expensive simulation. Quasi-physical (1D) MESFET models has been used during the past years as a device optimization tool [4,5]; two-dimensional models, on the other hand, though potentially more accurate and able to yield the frequency-domain small-signal device behaviour, rather than a quasi-static lumped model, have been seldom used for optimization [2], owing to their large CPU times. The purpose of the present paper is to show that a 2D simulator (MESS [3]) can indeed be effectively exploited for multiparameter device optimization. Of course, device optimization based on a 2D simulator must be performed with some care to keep the CPU times under reasonable limits and to obtain consistent results. In [2] optimization was started with a quasi-physical 1D simulator to have some preliminary trends; here a more systematic procedure, entirely based on 2D simulation, is followed.

The paper will address two specific case studies. The first study is the small-signal optimization of a single-implant recessed-gate MESFET by varying the implant dose and recess depth. A second, less conventional, study is the optimization of a recessed-gate MESFET for switching applications. Since switching devices operate in the linear region, the 2D small-signal time-domain analysis implemented in MESS performs poorly; a direct frequency-domain technique was therefore interfaced to MESS and used in all simulations presented in the paper.

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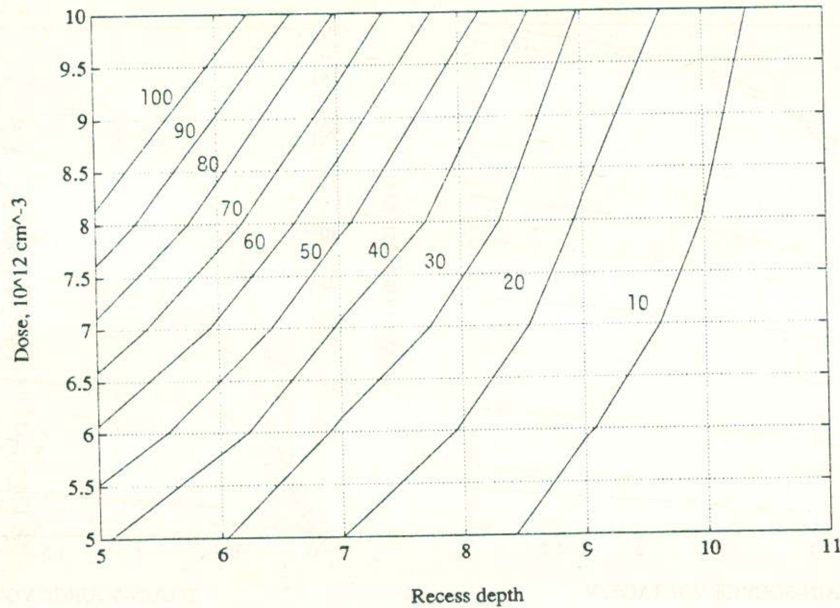

Figure 1: Contour plot of saturation current I_{DSS} (mA) as a function of implant dose and recess depth (10^{-2} μm).

Optimization of implanted MESFETs

The goal is the small-signal optimization of a Si-implanted recessed gate 0.5 μm MESFET. The device geometry (gate width 300 μm, gate-drain spacing 3.5 μm, gate-source spacing 1. μm) and the implant energy (100 keV) are kept constant, while the implanted dose is made vary between 5 and 10×10^{12} cm−2. The substrate is supposed to have zero compensated doping and therefore a n^- behaviour results owing to the implant tail. In order to work with a set of comparable devices, the additional constraint of equal saturation current was added: I_{DSS} = 50 mA for zero gate bias.

The first goal was the achievement of the given I_{DSS} by tuning the recess depth together with the implanted dose. A set of 42 simulations was performed by varying the recess depth between 0.05 and 0.11 μm with step 0.01 μm and the dose between 5 and 10×10^{12} cm−2 with step 1×10^{12} cm−2. The saturation current was computed at $V_D = 3$ V, working with the *same* 2D discretization (about 1400 nodes) in order to have consistent and comparable results. The first set of simulations required about 18 hours CPU on a VaxStation 3500, and the results are summarized in the contour plot of Fig.1. The 50 mA level curve yields the recess depth needed to obtain the required saturation current.

A full set of DC curves was now simulated (V_G = 0, -0.5, -1., -1.5, -2., -2.5, -3. V) for the 50 mA devices. The results are shown in Fig.2; fairly good agreement was obtained for the maximum required saturation current (50 mA) using the recess depth derived from Fig.1. This second set of 6 simulations required about 12 h CPU. Finally, the small-signal simulation of the same devices was carried out for $V_D = 3$ V, V_G = 0, -0.5, -1. V. The simulations took about 6 h CPU and the resulting intrinsic elements, derived by fitting the small-signal admittance parameters, are shown in Fig.3 and Fig.4.

The behaviour of the small-signal parameters as a function of the dose suggests the following remarks. First, the constraint on I_{DSS} is important since it reverses the trend of some parameters with respect to the case in which the dose is varied but the recess depth is kept constant (see [5, Fig.3]). Second, an almost monotonic improvement is achieved for increasing dose: R_{DS} and g_m increase, while the parasitic R_S and R_D decrease. A small increase can be detected also for C_{GS}; the resulting current cutoff frequency $f_T = g_m/2\pi C_{GS}$ is therefore sensibly constant as a function of the dose, whereas the maximum oscillation frequency $f_{\max}$ increases owing to the decreasing R_I. A

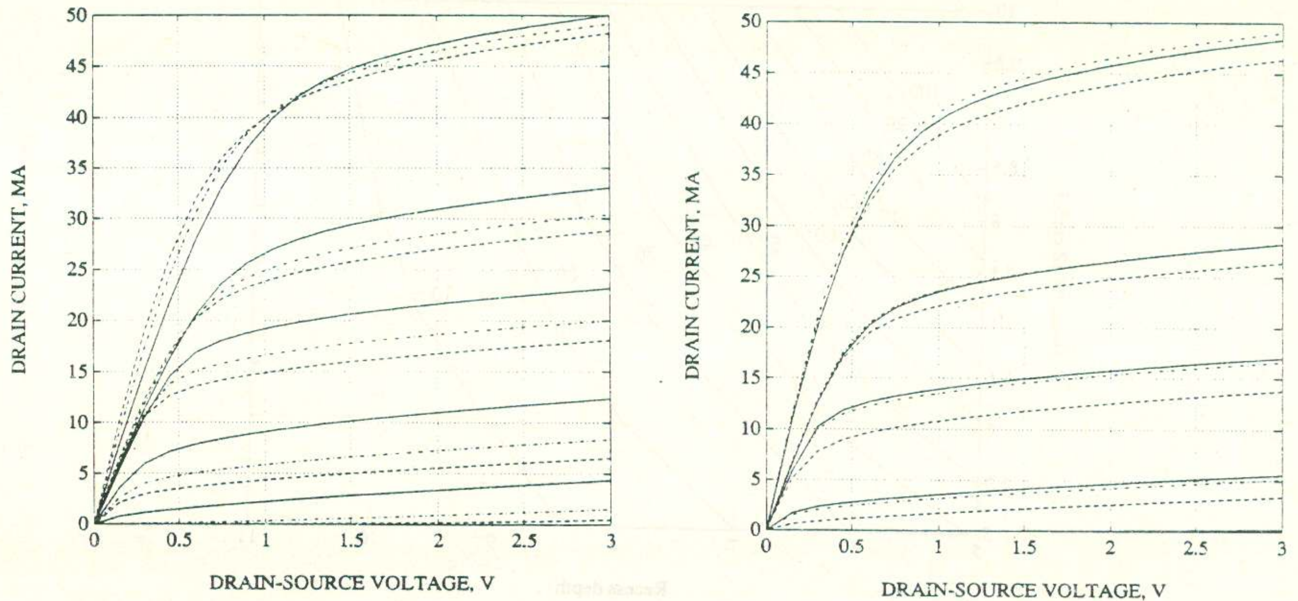

Figure 2: DC curves for 50 mA MESFETs as a function of dose. The V_g step is 0.5 V starting from V_g = 0. Left: 5×10^{12} cm^{-2} dose (continuous line); 6×10^{12} cm^{-2} dose (dashed-dotted line); 7×10^{12} cm^{-2} dose (dashed line). Right: 8×10^{12} cm^{-2} dose (continuous line); 9×10^{12} cm^{-2} dose (dashed-dotted line); 10×10^{12} cm^{-2} dose (dashed line).

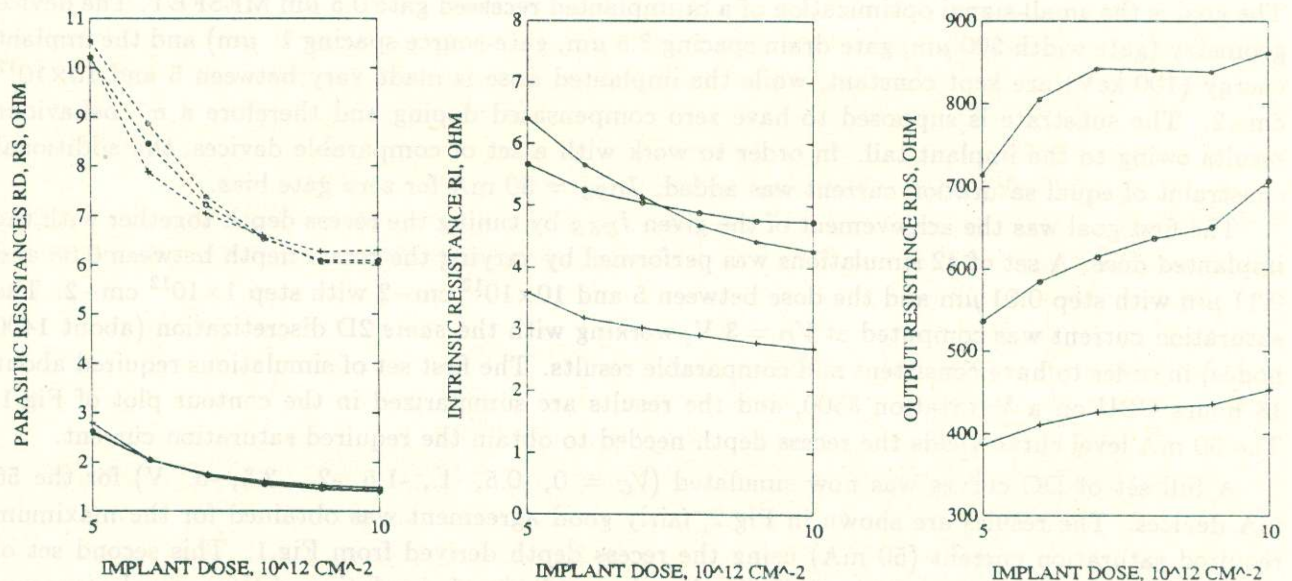

Figure 3: Equivalent circuit elements as a function of implant dose for $V_G = 0$ (+), -0.5 (o), -1 (*) V.

further increase of the dose beyond 1×10^{13} cm^{-2} could lead to a performance improvement but in this case the actual activated doping profile can become flatter than an ideal Gaussian one owing to the effect of solid solubility limits.

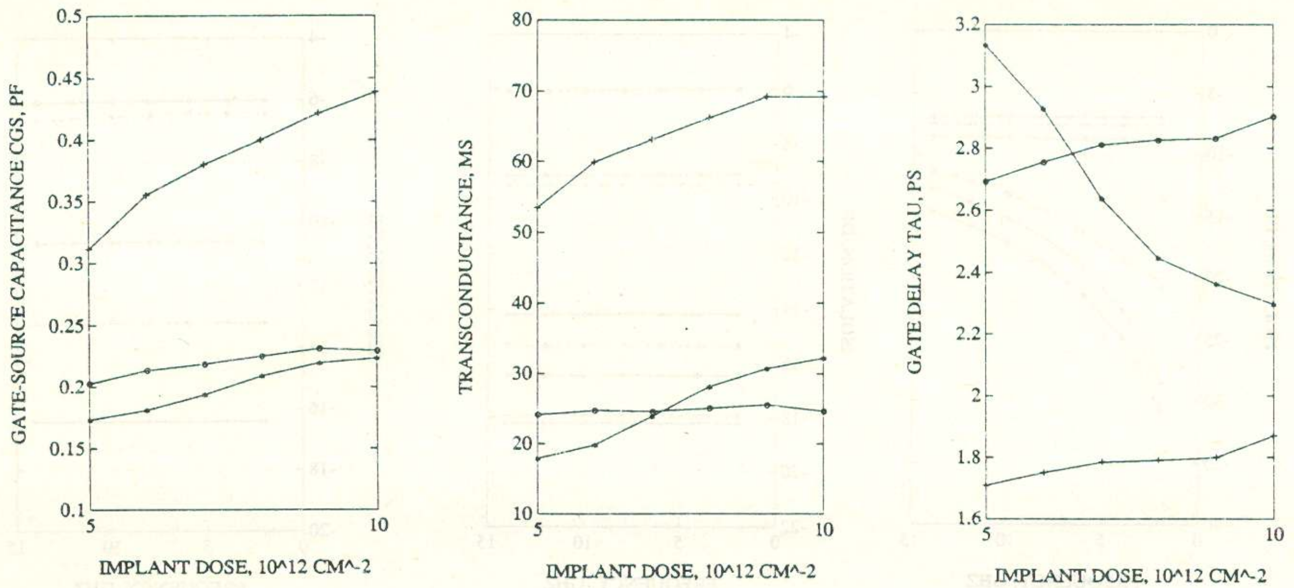

Figure 4: Equivalent circuit elements as a function of implant dose for $V_G = 0$ (+), -0.5 (o), -1 (*) V.

Optimization of MESFETs for switching

A more advanced and unconventional topic is the optimization of MESFETs used as microwave switches [1]. These devices are usually designed according to rules which are typical of analog MESFETs, whereas switch optimization should take into account not only the peculiarity of their operation, but also that RF switches can be realized in the series (S) or parallel (P) configuration (Fig.5), which are not necessarily optimized by the same parameters. Better performances can be obtained by combining series and parallel switching sections; however, these cases will not considered here for the sake of simplicity. The gate resistance R_{gg}, which in practical switches takes on rather high values (e.g. 1 kΩ) is replaced here by an open circuit (i.e. the gate is open) in order to concentrate on the device performances alone.

The equivalent circuit of a MESFET switch, shown in Fig.5, is considerably simpler than for analog devices. This circuit can be characterized through fitting on the impedance matrix element z_{DD}, which can be derived from 2D simulation. The device to be optimized is a symmetric 1 μm recessed-gate MESFET with 5 μm drain-source spacing and 600 μm periphery. The doping is 2×10^{17} cm^{-3} up to 0.2 μm [1]; a compensated p-type substrate with a residual doping of 1 $\times10^{12}$ cm^{-3} is assumed. The gate recess depth a was made vary between 0 and 0.1 μm. The I_{DSS} as a function of V_G and of the recess depth is shown in Fig.5 while the equivalent circuit elements at zero drain bias are in Fig.6. The "on" and "off" state are taken at V_G=0, -3 V for the S-switch and at V_G=-3, 0 V for the P-switch.

The results suggest that only for $a > 0.6$ μm does the device have acceptable on-off resistance ratio both in the S and P configuration. The on-off ratio has a maximum towards 0.9 μm recess depth, and then begins to deteriorate owing to the increase of the low-bias resistance. The extremely high value of the S-off resistance obtained from simulation is nonphysical, and is due to the p-type substrate model. Practical values exceed several kΩ; in order to have realistic trends from a given technology, the substrate parameters should be properly tuned so as to give the correct post-annealing resistivity.

Since P and S switches are complementary (i.e. the *on* state of the P-switch corresponds to the *off* state of the S-switch, and *vice-versa*) taking the on-off resistance ratio as the sole figure of merit

[1] This flat profile can be obtained either through epitaxy or by repeated implants.

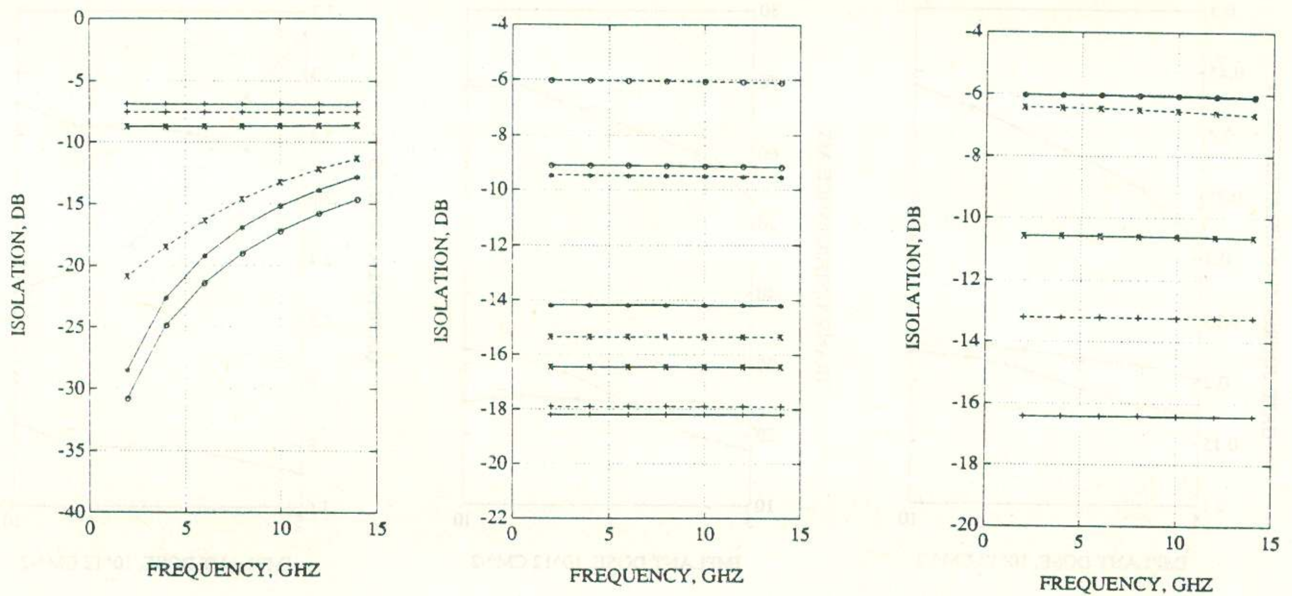

Figure 7: Left: frequency behaviour of S-switch for $V_G = 0$ (+), -1 (x), -2 (*), -3 (o) V; 0.08 μm (continuous line) and 0.1 μm (dashed line) recess depth. Center: same for P-switch, 0.04 μm (continuous line) and 0.08 μm (dashed line) recess depth. Right: same for 0.08 μm (continuous line) and 0.1 μm (dashed line) recess depth.

significantly worse than the ideal value of 6 dB. With this value the *off* isolation is greater than 20 dB up to 7 GHz. For the P-switch, the optimum recess value is slightly different and equal to 0.06 μm, corresponding to a flat *off* isolation of 18 dB and *on* isolation of about 6 dB. With shallower recess the *on* isolation is unacceptable, wheras for deeper recess the *off* isolation deteriorates. The optimization of P-switches is somewhat made simpler by its flat frequency behaviour; however, there is a tradeoff with the maximum achievable isolation, wich is lower in P-switches than in S-switches.

Conclusions

Two optimization studies of GaAs MESFETs have been presented to show the possibilities offered by 2D physical simulation in the design of advanced devices or devices for switching. For the latter class, some interesting conclusions are brought out, e.g. that series and parallel switching devices should be separately optimized. The CPU times required for a multiparameter trend analysis are comparatively large (several hours CPU) but still acceptable, considering that 2D simulations can be performed on a small, low-cost workstation.

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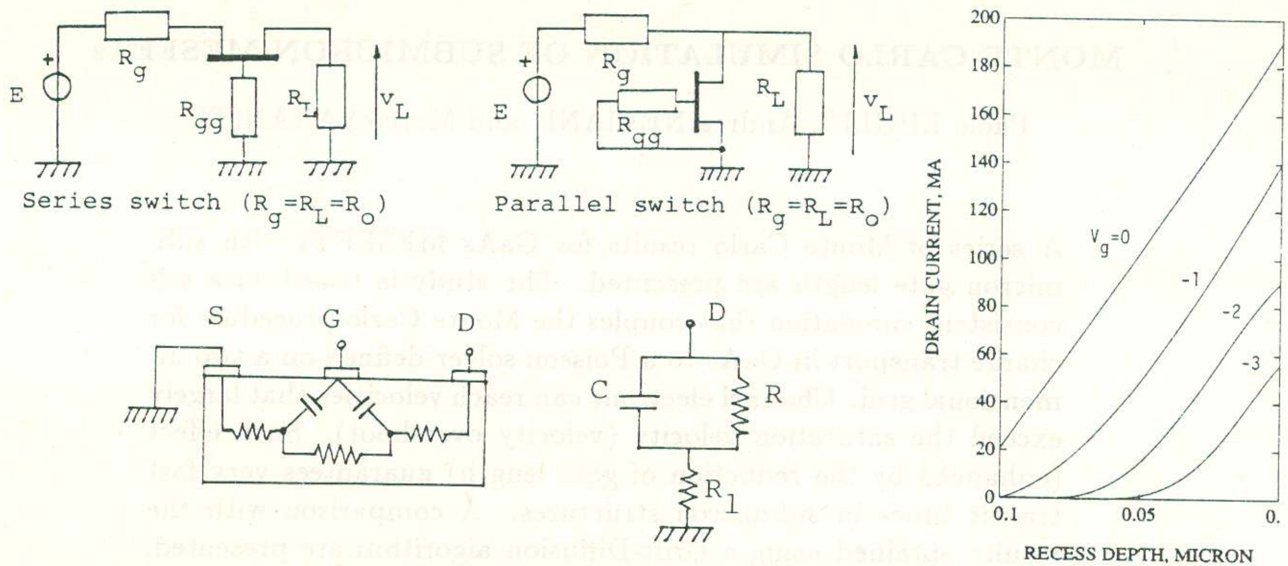

Figure 5: Left: switching configurations and equivalent circuit. Series switch (left); parallel switch (right). Right: I_{DSS} as a function of recess depth.

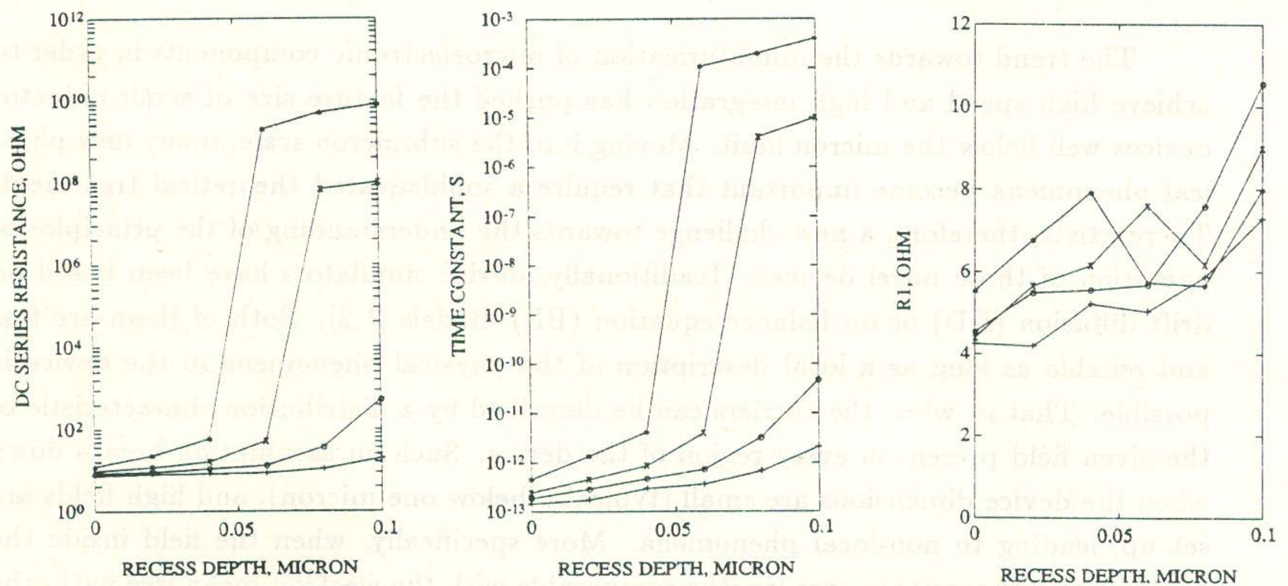

Figure 6: Behaviour of equivalent circuit elements as a function of recess depth: $R_1 + R$ (left); RC (center); R_1 (right). Polarizations are: $V_G = 0$ (+), -1 (o), -2 (x), -3 (*) V.

could be simplistic, i.e. an optimum P-on state does not necessarily provide and optimum S-off state. While the P-switch has an almost flat frequency behaviour, the analysis of the S-switch is made more complex by bandwidth considerations: the higher the S-off resistance, the higher the time constant, and the narrower the bandwidth of the S-switch.

A more direct insight on the properties of S and P switches can be derived from the frequency behaviour of the isolation I (Fig.7). Here this parameter has been simply defined with respect to the generator voltage as $I = 20\log_{10}(v_L/E)$. The minimum isolation is therefore -6 dB (matched load directly connected to the generator) rather than 0 dB. The isolation of off S-switches decreases with frequency, whereas the one of P-switches is almost constant, but lower. For the case at hand, the value of 0.08 μm seems to be optimum for the S-switch, since for deeper recess the *on* isolation is