Influence of 0-level packaging on the microwave performance of RF-MEMS devices

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Abstract
RF-MEMS devices (Radio Frequency-MicroElectroMechanical Systems) are made of moveable and fragile structures (membranes, beams, cantilevers,…) that must be encapsulated for protection and for stable performance characteristics. Zero-level or wafer-level packaging developed so far has been limited to dc-components. This paper elaborates on the design and fabrication of a 0-level package for housing RF-MEMS devices. The fabrication process is described and packages are characterized in terms of mechanical strength, hermeticity and microwave performance in the range 1-50 GHz. Simulations and experiments show minimal impact of the package on the RF losses if the cap has a minimal height of 50μm, if low-loss materials (e.g., glass) are used, and if matched RF feedthroughs are implemented. Finally, in a multi-switch design, we recommend to minimize the number of feedthroughs, i.e. to use a single cap for the entire design.

1. INTRODUCTION

RF-MEMS devices, such as switches, tunable capacitors, mechanical resonators and filters (1), contain movable and fragile parts that must be encapsulated for reasons of protection (such as handling, wafer dicing or plastic moulding operations) and to ensure stable and reliable performance characteristics. The work on wafer-level or 0-level packaging done so far has been limited to dc components, e.g., accelerometers (2) or microrelays (3,4). And, although micromechanical switches were among the first devices studied in the field of RF-MEMS, packaged switches have *not* been described so far. In fact, packaging issues of RF-MEMS components have only been marginally addressed (1,6). Since the 0-level package defines the first interface of the RF-MEMS device to the outside world, it is clear that the RF design of the package and in particular of the RF signal feedthroughs is very important. For instance, for a RF-MEMS switch, the package and interconnects can degrade the switch performance, but a proper design of the lines and the feedthroughs can overcome this problem. The 0-level package for RF-MEMS devices we propose here consists of a cavity with built-in RF feedthroughs as depicted in Fig. 1, illustrated for a series RF-MEMS switch implemented on a CoPlanar Waveguide (CPW). The general idea behind the 0-level package is to cap the RF-MEMS structures with a "capping" chip, which is bonded to the substrate chip. The thickness of the sealing ring defines the cavity height as indicated in Fig. 1. The 0-level package must satisfy requirements on (shear) strength of the bond, on hermeticity of the cavity walls, and on introduced RF losses. The study has been carried out on elementary RF structures based on CPWs, but any kind of RF-MEMS component can be packaged in this way. This paper elaborates on the design and fabrication of a 0-level package for housing RF-MEMS devices. The influence of different cap materials is investigated, including low loss borosilicate glass (AF45) and standard silicon (1-10Ωcm). The influence of the cap height g and the feedthrough length w (which is related to the width of the sealing ring) are also investigated. The total cap height g is defined as the distance between the top of CPW and the bottom of sealing cap. It is thus defined by the solder layer thickness, the 2 metal adhesion layers (Top Surface Metallization and Bottom Surface Metallization) and the BCB top layer (see Fig.2). Both modeling and experimental results are presented.

2. DESCRIPTION OF THE 0-LEVEL PACKAGING PROCEDURE (THE IRS METHOD)

The 0-level package or cavity is realized using a flip-chip assembly method based on a solder bond and is referred to as the indent reflow sealing (IRS) technique (4). This technique allows the realization of hermetically sealed cavities with a controlled ambient (gas and pressure) at relatively low temperatures (typically 220-320°C). The technique is only briefly described here as the focus is on the RF design and RF characteristics (details of the IRS method can be found in (4)). First, a solder (SnPb) layer with the required thickness is electroplated on the cap wafer, thus defining the sealing ring and the cap height g as indicated in Fig. 1. Next, prior to the flip-chip assembly, an indent (or groove) is made in the solder ring. The chips are then aligned to each other and then pre-bonded (at a temperature well below the melting point of the solder), and next reflowed in an oven which is set at the desired ambient and at a temperature high enough to melt the solder (around 240°C for SnPb). The solder layer melts, thereby closing the indent, resulting in a hermetically sealed cavity.

3. MECHANICAL TESTING: HERMETICITY AND SHEAR STRENGTH RESISTANCE

Hermeticity and shear strength testing are both related to reliability characterization. Indeed, the degree of hermeticity plays a predominant role in the long-term drift characteristics of a RF-MEMS switch as the ambient inside the cavity (gas, pressure, vacuum if desired) determines the time response of the switch. *Hermeticity* testing includes both fine leak and gross leak tests (5). Fine leak testing is based on a He leak detection after the sample is placed for a few hours in a high He pressure chamber (24 hours in He at 2.5 bar pressure), and gross leak testing is a visual test based on liquid Fluorocarbon bubble observation. On 17 tested samples (9 devices capped with silicon and 8 devices capped with glass), the measured fine leak rates remained in the range of the detection limit of the He spectrometer ($0.2\ 10^{-9}$ mbar.l/sec) as specified by the MIL-STD883E procedure (method 1014.9) for a good hermetic package. However, the tested volumes are much smaller (in the order of 10^{-4} cm^3) than the typical volumes measured by such a technique (> $0.05 cm^3$). Thus we have to stay careful about these results, and fine leak detection of

such small cavities is still under investigation. For further verification concerning gross leak detection, only 2 devices out of 17, with a glass cap showed a gross leak. Those 2 samples corresponded to a weak bond strength (below 1MPa), and thus this gross leak was certainly caused by a bad bonding operation. We can thus conclude from those results that the solder bonds, in a first approximation, show a good hermeticity.

Shear strength testing determines the integrity of the materials and the procedure used to attach the cap chip to the device chip. This determination is based on the measure of a force applied to the cap chip, in the plane of the bonded interface, until the cap is removed from the device chip. The MIL-STD 883E procedure (method 2019.5) specifies a minimum shear force of 6MPa for a die area smaller than $4mm^2$.

From all 17 tested samples, the shear test showed globally a higher resistance for silicon caps than for glass caps: 42MPa for silicon caps versus 17MPa for glass caps, for identical sealing rings (solder ring: 3x3mm, width: 50µm, area: $0.59mm^2$, height: 10 µm). Indeed, the adhesion of solder on glass is weaker than on silicon and a chemical pretreatment of the glass wafers prior to metal electroplating is necessary to increase the adhesion. The bond strength also appears to be higher for narrow solder widths than for wide solder rings as shown in Fig.7 for silicon caps. The bonding has been realized at a constant mechanical force, thus one can expect that a higher bonding force is required for wider solder rings to obtain an equivalent bond strength. The shear resistance also appears to be independent from the solder height as shown in Table 2 for silicon caps. All the results obtained are in perfect agreement with he MIL-STD883 specifications.

4. DESIGN OF THE RF FEEDTHROUGHS

The design and realization of CPW feedthroughs is based on a technique developed for connecting a ceramic package to a multilayer board through small diameter balls (7). In our application, the realization of RF-feedthroughs is similar but uses a multi-layer thin-film technology (8). This technology consists of alternating thin layers of photosensitive benzocyclobutene dielectric (BCB series 4000) and low loss copper metallizations deposited on a borosilicate glass carrier substrate (type AF45). An RF feedthrough consists of a CPW input and output line that passes under the metal seal of the cap. The intrinsic feedthrough can be regarded as a local microstrip line (MSL) as illustrated in Fig. 2. The length of the feedthroughs varies with the width of the sealing ring and the design is such that the microstrip line keeps a characteristic impedance identical to the CPW (typically 50Ω).

5. RF SIMULATIONS AND RF MEASUREMENTS ON CAPPED CPWs

The high-frequency performance can be disturbed in two ways when soldering a capping wafer on a MEMS device: 1. The feedthrough lines running under the solder sealing ring is a transition with a possible mismatch and extra loss. 2. The CPW lines used as interconnection in the capped wafer can be detuned by applying a capping wafer above them. This is especially true when applying a lossy high-dielectric capping wafer as e.g. silicon.

A proper matched design of the feedthrough can be found in (8). To investigate the influence of the capping wafer on the CPW transmission lines a test structure as outlined in Fig.5 was used. The length of the taper is T=50µm, the length of the actual feedthrough running under the sealing ring has a value of 50, 200 or 500 µm depending on the test structure with corresponding lengths of the CPW line inside the package L of 2720, 2420 and 1820 µm respectively. The size of all capping wafers is only slighly larger then the sealing ring size i.e. C=L+2F+4T. Three solder heights were used for testing: 5µm, 15µm and 30µm thick layers electroplated respectively on silicon and glass wafers, corresponding to total cap heights *g* of 22, 32 and 47µm (including the UBM and TSM layers, and BCB top layer). In all measurements a feeding line length S of 400 µm is used.

The capped transmission lines can be divided in three types of transmission line (see Fig.5 and Fig.6): Linetype 1 is a normal unpackaged CPW transmission line. It's accurate model is part of the IMEC library for microwave design on Thin Film (9). Linetype 2 is the feedthrough including tapers and via connections between metal 1 and 2. It can be modelled as a microstrip line in a two layer medium (glass-BCB) with the sealing ring acting as a groundplane. Linetype 3 finally is the capped CPW line on metal 2. One can use a similar model as for the uncapped CPW line (9) but with modifications on the scaling equations for the characteristic impedance Zc, epseff and losses. The modified equations are based on extracted data from the measured test structures for Glass and Si capping wafers with different cap heights as indicated in Fig.7. Fig.6 shows the model of the complete test structure: it includes full scalable models for all three line types. In Fig.8 a comparison is shown between the measurements and the modelled S parameters of a complete test structure (F=50µm, L=2720µm) for 22 and 47µm cap height for both Si and Glass caps. A good agreement between measurements and model can be realised.

Although a full scalable model is good for an in-depth analysis of the capped structure a simplified technique can be used in design: the small impedance mismatch for the feedthrough and metal 2 lines allows to compute the total insertion loss (in dB) by adding the insertion losses (in dB) of the individual line types as indicated in Table2. In this table one can see that a feedthrough line has considerably higher losses then a metal 2 line because of the smaller line width to realise a 50 Ω microstrip line and the higher losses of the metal 1 layer. It is therefore prefered to keep the feedthrough line length and thus the sealing ring width to a minimum value which is mechanically still tolerable. From Table2 and Fig.6 it follows that a Si capping wafer requires a solder height of at least 30 µm to reduce the capped CPW losses while a Glass capping wafer can be soldered with a thickness as small as 5 µm. For very small solder thicknesses the CPW line on metal 2 should however be redesigned to yield a matched line.

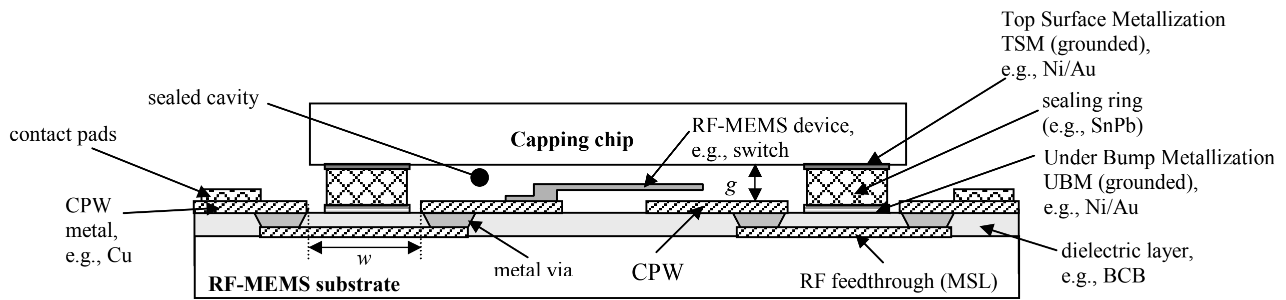


Figure 1. Schematic of an RF-MEMS device in a 0-level package (shown is a series switch implemented on a CPW)

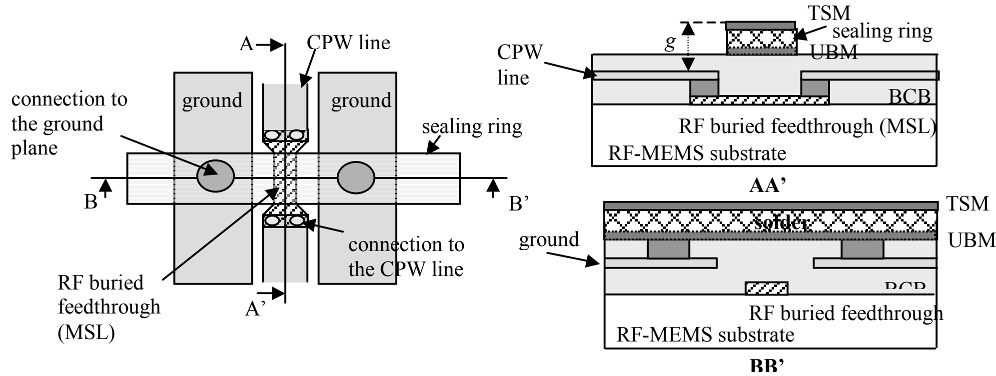
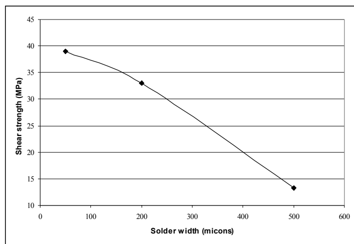


Figure 2. Design of RF buried feedthroughs locally configured as a microstrip line (an extra BCB layer covers the CPW lines, which is not shown in Fig.1)



Solder width (µm)	Solder height (µm)	Shear strength (MPa)
50	**10**	42
	35	39
500	**20**	20
	35	14

Table 1. Shear strength versus solder height (sealing ring: 3x3mm)

Figure 3. Evolution of shear strength resistance with solder width (solder ring: 3x3mm, height: 35µm)

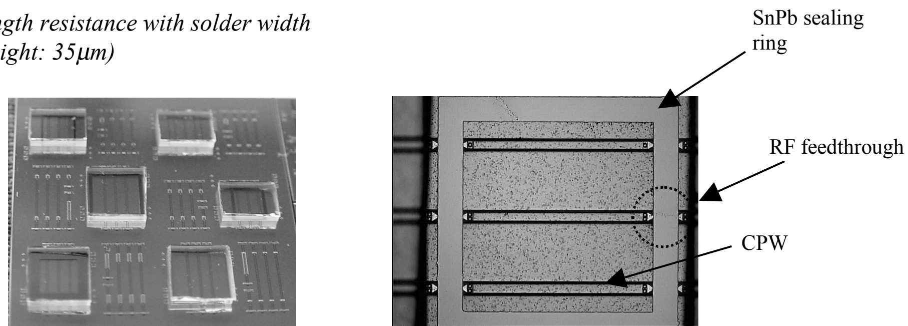


Figure 4. Pictures of packaged CPWs clearly showing the solder sealing ring

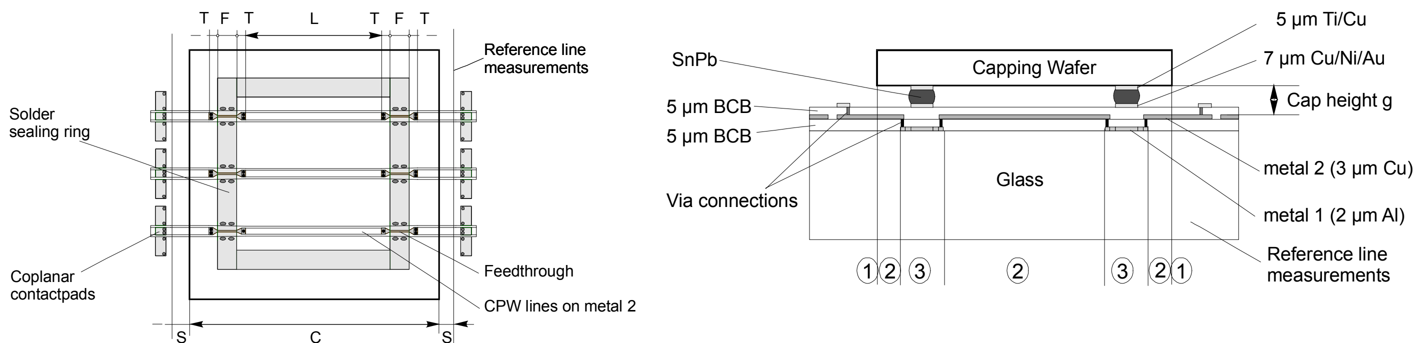


Figure 5. Layout of the test structure (top view on the left and cross section on the right).The complete test structure can be divided in three linetypes: 1. Uncapped CPW lines, 2.capped CPW line and 3. Feedthrough including tapers and via's.

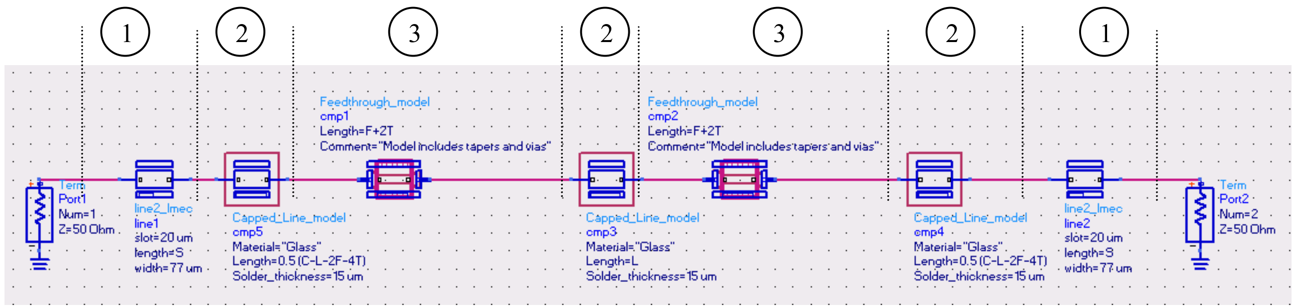


Figure 6. *Implementation of the model in ADS: the complete test structure is divided in three linetypes: 1. Uncapped CPW lines, 2.capped CPW line and 3. Feedthrough including tapers and via's All linetypes have a full scalable model.*

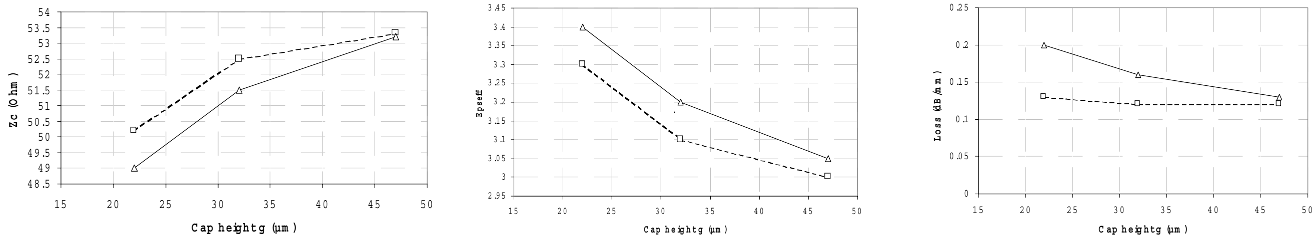


Figure 7. *Capped line characteristics as extracted from measurements: it shows the influence of the capping wafer on the line characteristics of a CPW line on metal 2(line width=77µm, spacing=20µm). Triangles is for a standard Si capping wafer, squares is for a AF45 glass capping wafer.*

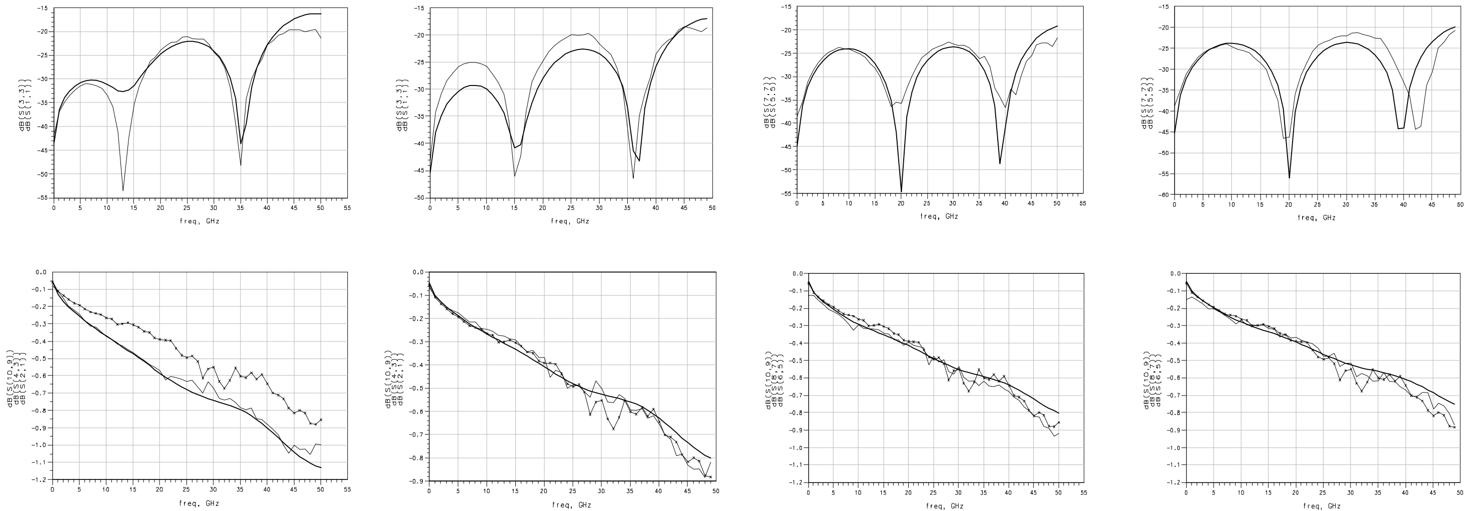


Figure 8. *Comparison of model and measurements for the complete test structure of Fig.5 (leftmost Si caps with g=22µm, centre left Glass caps with g=22µm, centre right Si caps with g=47µm, rightmost Glass caps with g=47µm). The thick line is the model as shown in Fig.6, thin line with circles is the corresponding measurement results. Measurement results for the same test structure without capping wafer (thin line with crosses) are included as a reference. Following parameters are used in the model: S=400µm, T=90µm,F=50µm,L=2720µm,C=3200µm.*

Table 2. *Insertion loss contributions for different line types. This can be used for loss estimation of the complete structure when one assumes that all line types are perfectly matched.*

Freq.	**IL unpackaged transmission line**	**IL feedthrough**	**IL Glass capped line g=22µm**	**IL Si capped line g=22µm**	**IL Glass capped line g=47µm**	**IL Si capped line g=47µm**
5 GHz	0.04 dB/mm	0.26 dB/mm	0.04 dB/mm	0.07 dB/mm	0.04 dB/mm	0.05 dB/mm
30 GHz	0.12 dB/mm	0.46 dB/mm	0.12 dB/mm	0.22 dB/mm	0.14 dB/mm	0.15 dB/mm

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