High Power LDMOS technology for wireless infrastructure

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ABSTRACT

The progress in wideband cellular systems was followed by the development of the necessary transistor technology. This contribution describes microwave LDMOS transistors used in RBS (Radio Base Station) amplifiers. We discuss the issues of the manufacturing process, packaging, reliability, RF performance and models necessary for successful devices for 3G systems at 2.1 - 2.2 GHz.

I. INTRODUCTION

Cellular radio telephone systems have been in use for 20 years with NMT-450 introduction during 1981. Since then the systems evolved from analogue to digital modulation schemes for both speech and data transfer with much increased bandwidth. The ever-increasing market demand of digital basestation power amplifiers in PCS, CDMA, and WCDMA systems requires a low cost, ease of use technology which can provide high power and better linearity performance. LDMOS started replacing bipolar devices in basestation applications 3-4 years ago and has become the leading technology for basestation power amplifier applications because of the multiple reasons. LDMOS is a majority carrier device and thus has potentially higher cut-off frequency than BJT. It also has a backside source contact which substantially decreases the source inductance. As a result LDMOS has high gain. The grounded backside allows also use of cheaper packages with better thermal properties in which the dies are directly soldered to the flange, instead of older bipolar variety with toxic beryllium oxide isolator. Since the drain current has a negative temperature coefficient, LDMOS doesn't need ballast resistors and also has a better thermal uniformity compared to BJT. It also shows an excellent back-off linearity. In addition to the performance gain LDMOS technology has some practical advantages. The breakdown voltage BV_{dss} can be easily adjusted by layout to fit different application voltage. It uses mature low cost technology and it's simple to integrate with CMOS. The device size can be scaled with reasonable ease.
However, there are some fundamental limits to LDMOS technology. Frequency response is limited by gate charging and transit time required through N- drift region, making LDMOS less suitable for operation over 3 GHz. It suffers also from excess efficiency degradation with increasing frequency operation and due to hot electron injection in the gate oxide we experience I_{dq} drift.

II. DEVICE PROCESS

The latest generation of LDMOS transistors from Ericsson Microelectronics (GOLDMOS V), primarily intended for use in the 1.8-2.2 GHz frequency range, has a cross-section as shown in Fig.1. The transistor is built into a p+ substrate with a p-epi on top. It consists of alternating n+ drain and n+ source regions where the n+ drain is separated from the gate by an n- drift region. The p-type channel dopant is diffused laterally in under the gate from its source side to form p-well. Deep p+ diffusion allows the current to pass from the n+ source to the p+ substrate with minimal voltage drop by means of a metal jumper shorting these regions to one another.
This metal is wrapped around the gate to act as a shield between gate stack and drain metal, which reduces the feedback capacitance (C_{rss}) significantly. A second metal layer fills two purposes. The metal-2 conductor makes contact to the gate at regular intervals to reduce RC delays. On the drain side metal-1 and metal-2 conductors are stacked to decrease current density. Nominal gate length is 0.6 µm and gate oxide thickness is 500 Å. The gate stack consists of n+ doped polysilicon and 2500 Å $MoSi_2$ with sheet resistivity of 2.5 Ω/sq. The n-drift region length is 3 µm, resulting in a typical breakdown voltage BV_{DSS} of 75V, with the prerequisite of a high enough p-type dopant concentration in the p-well region to avoid a premature punch-limited breakdown. This in turn results in a typical threshold voltage V_{th} of 4V. Both metal layers are gold with a TiW/TiW(N)/TiW barrier metal underneath. Nominal metal-1 gold thickness is 1.0 µm and metal-2 is 1.8 µm.

III. DEVICE PERFORMANCE

Ericsson has developed GOLDMOS technologies for 3G base station applications. The 30W PEP (peak envelop power) single ended and the 120W push-pull devices WCDMA performance at 28V and 2.14GHz are summarized in Table 1 and 2. The two-tone tests are done using 100kHz tone spacing. The single carrier 3GPP WCDMA evaluation are done with 3 DPCH channels, ~ 9 dB peak to average ratio, -45 dBc ACPR @ 5MHz and 3.84 MHz BW. LDMOS technology shows excellent backed-off linearity compared to BJT and GaAs devices. The 28V LDMOS benchmarking results showed > 5 dBc better IM3 compared to 12V GaAs [1].

	IMD/ACPR (dBc)	Pavg/PEP (W)	Gain (dB)	Efficiency (%)
2 tone	-30 (IM3)	15/30	16	34
WCDMA	-45 (ACPR)	5.5	16	18

Table 1. 30W PEP LDMOS device for WCDMA linear PA

	IMD/ACPR (dBc)	Pavg/PEP (W)	Gain (dB)	Efficiency (%)
2 tone	- 30 (IM3)	60/120	13	33
WCDMA	-45 (ACPR)	22	13	16

Table 2. 120W PEP LDMOS device for WCDMA linear PA

IV . DEVICE MODELING

With increasing demands on performance, consistency and time-to-market on LDMOS devices for 3G applications and beyond, new methods for improving and predicting performance on both device and PA levels are needed. Device models, both behavioral [3] and physics based [4], provide a way to understand device operation, and more importantly to give PA and system designers an efficient tool to do performance optimization on PA and even system levels. Among various modeling approaches physics-based model can facilitate the optimization of the process parameters and easily incorporate electro-thermal (self-heating) effect, in addition to quickly predicting the device performance. Ericsson has developed physics-based compact models for LDMOS dies and fully packaged devices including internal matching networks, by paying special attention to the N- drift region that is the unique and the most difficult to model part of a LDMOS transistors. An intrinsic LDMOS sub-circuits model is shown in Fig. 2, where the drift region is modeled by a nonlinear resistor controlled by both gate and drain voltages or by a FET model. The BISIM3 model is used to model the MOS channel region. Fig. 3 shows good correlation between pulse-measured and modeled I-V curves. Good agreement between measured and modeled s-parameters on small test LDMOS structure from 100MHz up to 10GHz under two different bias conditions is shown in Fig. 4. The equivalent circuits for package and wires in packaged device are obtained from measurements done on the "dummy" devices where the LDMOS dies are replaced by Si "dummy" dies of known characteristics. The package and wire equivalent circuits can also de derived from EM simulation using the drawing and material information of the package and the bonding wire profiles.

V. RELIABILITY

There are five major reliability considerations for LDMOS technology development:
(1) I_{dq} shift: I_{dq} shift results from hot electron injection effect with high drain voltage (28V). The typical industrial spec is <10% I_{dq} drift in 20 years. The I_{dq} drift spec sets the limit of R_{dson} and BV_{dss} optimization.
(2) Thermal: Thermal dissipation issue results in device performance degradation, bias and match-in issues, and reliability degradation. The die spreading layout design, thinner substrate thickness, and better heat sink and packaging material are needed to reduce temperature gradient and minimize the temperature rise in the die.
(4) Ruggedness: Capable of withstanding certain amount of current into breakdown operation without bipolar turn on in mismatch condition.
(5) Electromigration: MTTF > 100 years. Preferable to use Au or thick Al stack. It will be a design issue for high power (>240W) single ended device.
(6) ESD: 1000 V HBM device integrated in LDMOS flow is needed.

VI. PACKAGE

Packaging is a crucial element of RF power transistor design, posing many conflicting requirements. The traditional packages with CuW flanges and flat leads have some inherent problems and the trend is to replace these packages with various types of surface mount packages. One of the problems with the old package types is the fairly low thermal conductivity of the CuW flanges. The cost of these high temperature brazed packages is high and as they are intended for manual assembly the total cost will be very high. The electrical grounding path from this type of component is not well defined if the component is mounted on a heat sink, as is the normal assembly method. As it is absolutely necessary to use a heat sink paste between the component flange and the heat sink and as those heat sink pastes are insulators the DC ground current cannot pass directly into the heat sink, Fig. 5. The DC ground current has to find its way to some points around the screws where the clamping force is high enough to squeeze away the heat sink past and thereby form an electrical contact between the flange and the heat sink. The DC ground current has then to pass back up to the ground plane in the PCB where the PCB happens to be in contact to the heat sink This variable ground path gives rise to spread and degrades the performance of the components, especially at the high frequencies (2GHz). At these high frequencies it is also very critical where the component is paced in the slot in the PCB and that the solder joint between the leads and the PCB reaches all the way to the edge of the metal pad on the PCB. All the above mentioned problems can be solved by using a surface mount package with a copper heat spreader.

VII. HIGH VOLTAGE LDMOS

Operation at higher supply voltage will increase the transistor output impedance for a given power level. It'll make the wideband matching easier and manufacturing tolerances less critical. LDMOS transistors for 48 V operation have already been proven. However, higher breakdown voltage results in higher resistance of drain drift region, limiting the maximum available drain current. New concepts for higher voltage devices maintaining low drain resistance are explored. An example of such research is a RESURF device, Fig. 6, from Uppsala University, Sweden, with a dual-layer extended drain region, which shields the active gate region from high voltage and thus overcomes the fundamental incompatibility between short channels and high voltage operation [4,5]. The 1 mm wide transistor showed output power of > 2 W/mm, Fig. 7, and gain > 20 dB at 1 GHz and V_{DD}=70 V. Gain at 3 GHz was 10 dB.

VIII. SUMMARY

LDMOS transistors are today preferred technology for linear RF Power Amplifiers for W-CDMA. This paper shows the excellent linearity characteristics of the transistors even at high power. The low power conversion efficiency, compared to older narrow-band systems, makes the thermal management and packaging an issue. New device concepts, offering both higher impedance level and higher power density, are under development.

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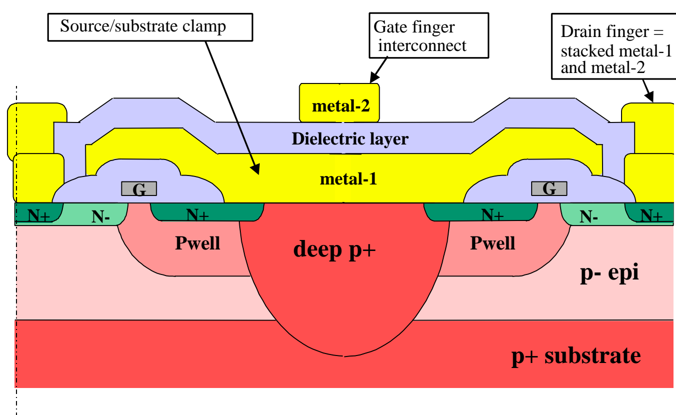

Fig. 1. Cross-section of the multi-finger LDMOS transistor

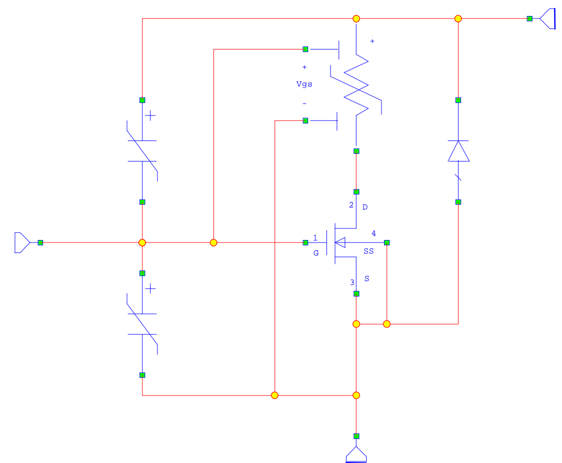

Fig. 2. Intrinsic LDMOS transistor die model

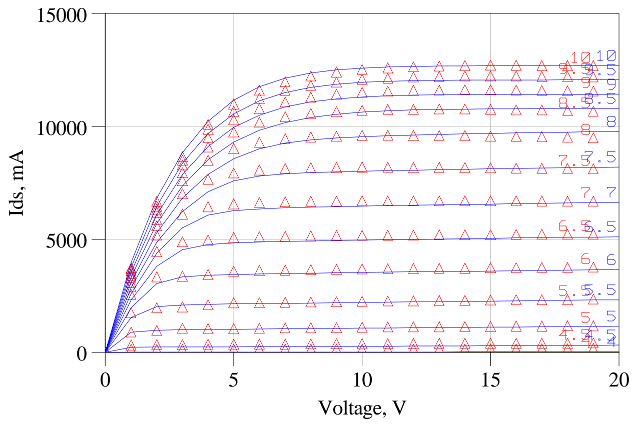

Fig. 3. Pulse measured (triangles) and modeled (solid line) DC performance on a full die with total gate periphery W_g=120 mm.

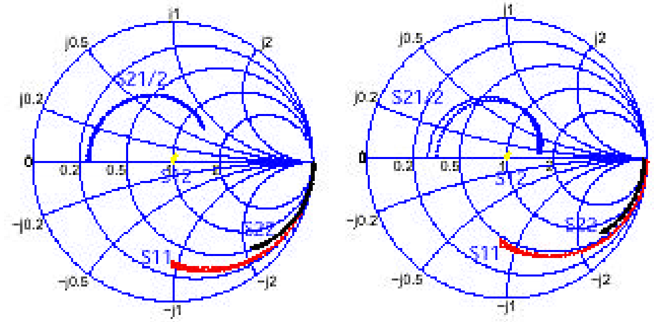

Fig. 4. Measured and modeled s-parameters under 2 bias conditions, left: V_{gs}=6V, V_{ds}=30V, right: V_{gs}=5V, V_{ds}=30V.

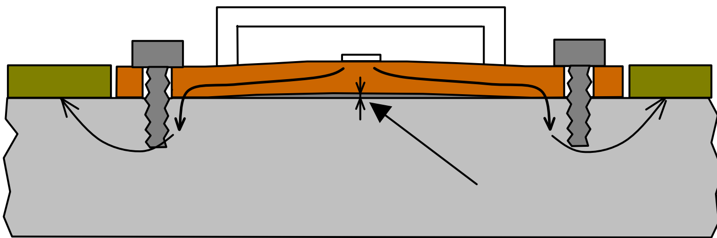

Fig. 5. DC ground current path from the transistor die to PCB ground plane in transistor with conventional package

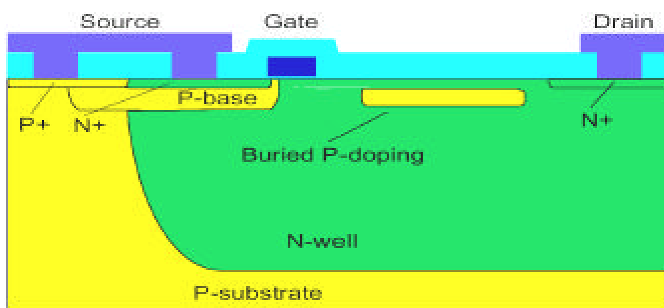

Fig. 6. Novel LDMOS transistor concept with a dual-layer extended drain region (courtesy of J. Olsson, Uppsala University).

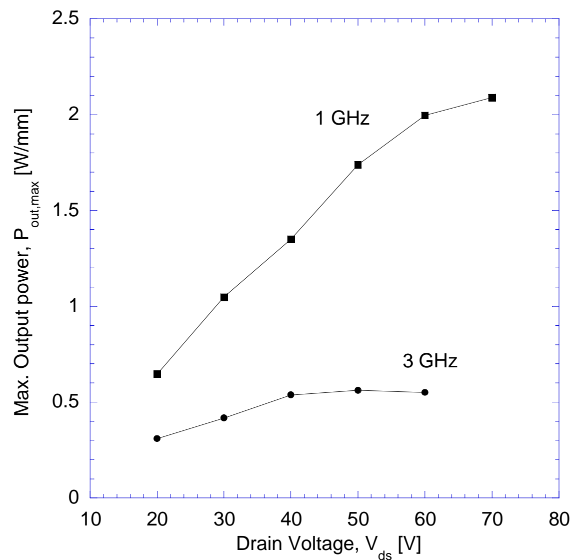

Fig. 7. Load-pull measurements of high-voltage LDMOS transistor with Wg=1 mm (courtesy of J. Olsson, Uppsala University).