

Measured Attenuation of Coplanar Waveguide on 6H, p-type SiC and High Purity Semi-Insulating 4H SiC through 800 K

George E. Ponchak¹, Zachary D. Schwartz², Samuel A. Alterovitz¹, and Alan N. Downey¹

1. NASA Glenn Research Center, Cleveland, OH 44135, USA

2. Analex Corporation, NASA Glenn Research Center, Cleveland, OH 44135, USA

Abstract — Wireless sensors for high temperature applications such as oil drilling and mining, automobiles, and jet engine performance monitoring require circuits built on wide bandgap semiconductors. In this paper, the characteristics of microwave transmission lines on 4H-High Purity Semi-Insulating SiC and 6H, p-type SiC is presented as a function of temperature and frequency. It is shown that the attenuation of 6H, p-type substrates is too high for microwave circuits, large leakage current will flow through the substrate, and that unusual attenuation characteristics are due to trapping in the SiC. The 4H-HPSI SiC is shown to have low attenuation and leakage currents over the entire temperature range.

Index Terms — SiC, Coplanar Waveguide, High Temperature.

I. INTRODUCTION

There is an increasing demand for microwave circuits that operate throughout the temperature range of 300 to 800 K for wireless sensors in aircraft engine performance monitoring, oil drilling, and mining machinery [1], [2]. This high temperature requires wide bandgap semiconductors such as SiC. In addition, wide bandgap semiconductors are required for high power microwave amplifiers, which increase the temperature to 500 K under the transistor. However, there is very limited data available on the characteristics of microwave transmission lines on SiC substrates as a function of temperature. The authors have reported on the attenuation of Coplanar Waveguide (CPW) on High Purity Semi-Insulating (HPSI) 4H SiC through 50 GHz and 300 to 800 K at zero bias [3], [4], but there has been no reported characteristics of the bias dependence of CPW on HPSI 4H-SiC, and there is no information on transmission lines on the more mature and widely used 6H SiC.

In this paper, we report the effects of bias on the attenuation of CPW lines on HPSI 4H SiC. Furthermore, we report for the first time the attenuation characteristics of CPW lines on 6H, p-type SiC substrates as a function of frequency, temperature, and bias.

II. CIRCUIT AND SUBSTRATE DESCRIPTION

The substrates used in the experiments are a High Purity, Semi-Insulating (HPSI) 4H-SiC wafer with a thickness of 409 μm and a room temperature resistivity greater than $10^5 \Omega \text{ cm}$ [5] and a 6H, p-type SiC wafer with a thickness of 418 μm and a room temperature resistivity of 2.4 $\Omega \text{ cm}$ [6]. Before processing, an RCA

clean is performed. No insulator is purposely grown on the SiC before or after processing. Finite width ground plane CPW lines with a center conductor width, slot width, and ground plane width of 50, 25, and 150 μm respectively are fabricated on the SiC using a liftoff process. After processing, the wafers are cleaned again to assure all photoresist and adhesion promoting material is removed. The CPW lines consist of 20 nm of Ti and 1.5 μm of evaporated Au. CPW lines of 5000, 5850, 6700, 8500, and 17500 μm lengths are used for the measurements.

III. MEASUREMENT PROCEDURES

A specially designed RF probe station capable of measurements through 813 K [7] was used to measure the CPW propagation characteristics. For the 4H HPSI SiC wafers, a full TRL calibration implemented with the NIST MULTICAL software [8] was performed at each temperature. Note that this is different than in [4] where the TRL calibration was performed only at room temperature and the high temperature data was corrected mathematically. To measure the effects of bias on the CPW attenuation, after calibration, the probes were left down on the 5000 μm long through line and the bias was varied between -20 and +20 V. Thus, the differential attenuation was measured. For the 6H SiC wafer, the attenuation was too high to perform a TRL calibration; thus, each transmission line was measured at each temperature and over the full bias range. The insertion loss was determined for each line from:

$$IL = -10 \log \frac{|S_{21}|^2}{1 - |S_{11}|^2} \quad (1)$$

and the attenuation was determined from

$$\alpha = \frac{1}{N} \sum_{n=1}^N \frac{IL(l_n) - IL(0.5 \text{ cm})}{l_n - 0.5 \text{ cm}} \quad (\text{dB/cm}) \quad (2)$$

where $l=0.5850, 0.6700, 0.8500, \text{ and } 1.7500 \text{ cm}$.

The leakage current between the CPW center conductor and the ground planes was measured on a Tektronix curve tracer by applying the bias to the CPW center conductor while the ground plane was held at ground potential. The capacitance-voltage (C-V) measurements were made between the CPW center conductor and the CPW ground plane, which was held at ground potential, with a HP 4192A LF Impedance Analyzer across the temperature range using the heater

stage described above. Lastly, in this paper, “dark” means the room lights and microscope lights are off and the window blinds are closed, and “light” means the room lights are on and a bright microscope light was directed at the wafer.

IV. 4H HPSI SiC RESULTS

The measured attenuation of CPW lines on 4H HPSI SiC is shown in Fig. 1. It is noted that the attenuation reported here verifies the conclusions of [4], which was derived from corrected data obtained from a system that was calibrated only at room temperature. The change in attenuation as a function of bias is shown in Fig. 2, where it is seen that there is no variation in attenuation with bias. Furthermore, no leakage current was detected between the center conductor and the ground planes of the CPW with an applied potential between -20 and +20 V with the light on or dark.

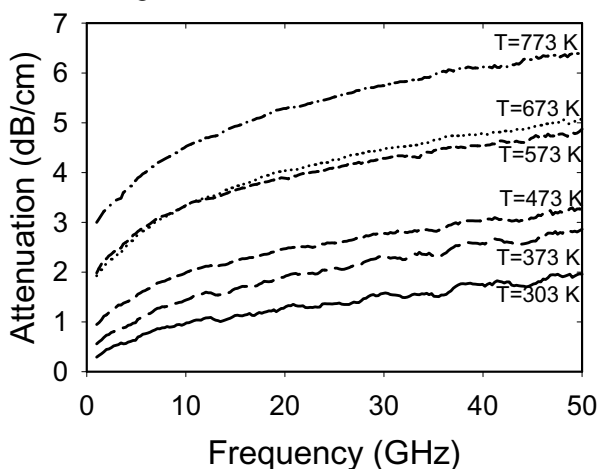


Fig. 1: Measured attenuation of coplanar waveguide on 4H HPSI SiC with $V=0$ and with light off.

V. 6H, P-TYPE SiC RESULTS

Van der Pauw measurements of the resistivity of the p-type, 6H SiC substrate are shown in Fig. 3. The room temperature resistivity of the wafer reported by Cree and confirmed by Hall measurements is $2.4 \Omega \text{ cm}$. Considering the steep slope of resistivity at low temperature and the uncertainty in the actual temperature of “room temperature,” this is in agreement with Fig. 3. The decrease in resistivity with increasing temperature below 450 K is due to increasing number of carriers; whereas, the increase in resistivity above 450 K is due to a decrease in carrier mobility. Since the metal resistivity of the CPW transmission line increases linearly with temperature and the SiC resistivity is nearly constant above 400 K, we expect the low frequency attenuation to increase linearly with temperature.

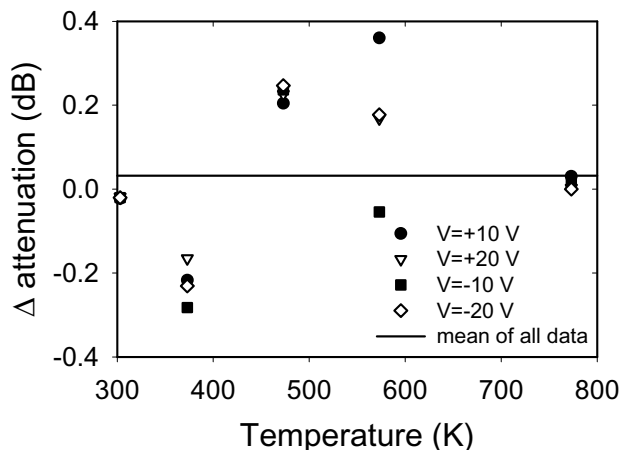


Fig. 2: Measured change in attenuation of CPW lines on 4H HPSI SiC as a function of bias and temperature at 25 GHz (dark).

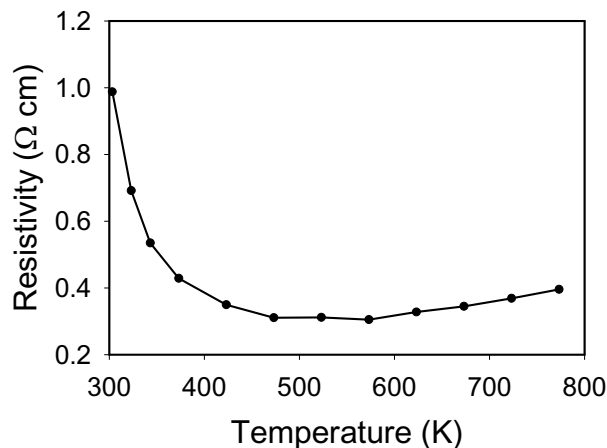


Fig. 3: Measured resistivity of 6H SiC by Van der Pauw technique. (There is no measured difference between light on and light off)

The attenuation of CPW lines on 6H SiC was measured across the temperature range of 303 to 773 K and for biases of -20, -10, 0, +10, and +20 V. Fig. 4 shows a typical measurement. There are a few interesting characteristics. First, above a few GHz, the attenuation increases monotonically with temperature, but unfortunately, the attenuation was too high to measure accurately and conclusions for high temperature, high frequency cannot be made. Second, the frequency dependence changed at elevated temperatures, which results in lower attenuation at 373 K than at room temperature. Figs. 5 and 6 summarize the attenuation versus temperature of the CPW lines in the dark and with the light on respectively. In both cases, it is noted that there is a minimum in attenuation at 373 K that is not predicted by the temperature dependence of the SiC resistivity measured by Van der Pauw or the metal resistivity. It is also seen that there is a 10 dB/cm reduction in attenuation when positive bias is applied if the temperature is greater than 400 K. Because the SiC is a p-type wafer, positive bias creates a wider depletion region, which should act as a high resistivity area, under the CPW center conductor. However, the decrease in attenuation is not seen at room temperature, which is unexpected.

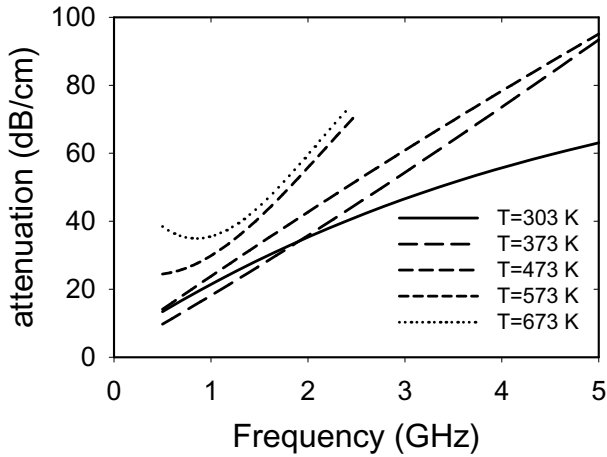


Fig. 4: Measured attenuation of CPW on 6H SiC at $V=+20$ V with light on.

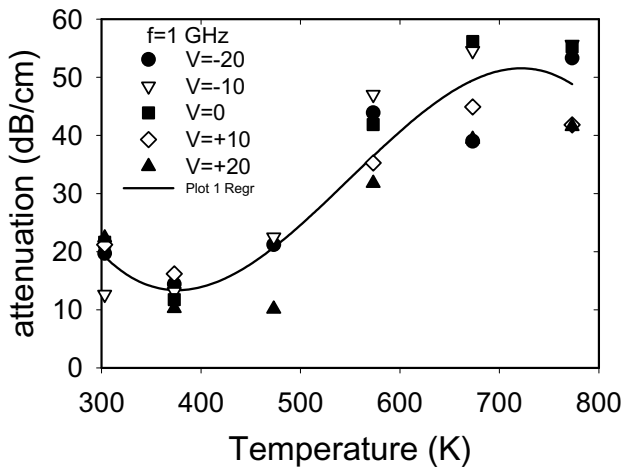


Fig. 5: Summary of measured attenuation of CPW on 6H SiC at 1 GHz in dark.

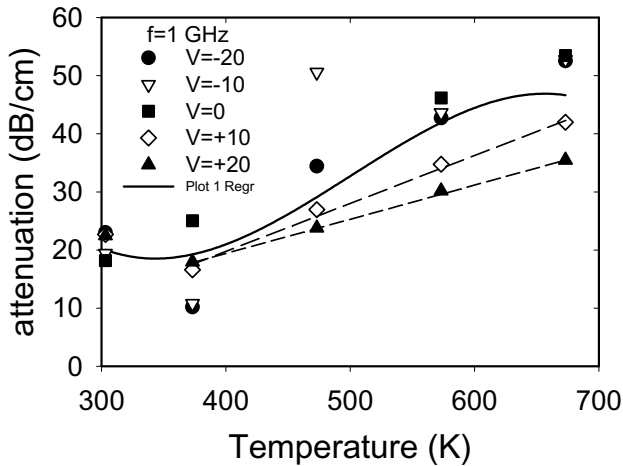


Fig. 6: Summary of measured attenuation of CPW on 6H SiC at 1 GHz with light on.

More interesting, the attenuation of the CPW lines for the wafer in the dark does not increase linearly with temperature, but if light is also applied, the attenuation increases linearly above 400 K if a positive bias is applied. Lastly, Fig. 6 shows that the attenuation is slightly decreased if the light is on compared to measurements in the dark, which is opposite to the authors experience with CPW lines on high resistivity Si.

The measured leakage current between the CPW conductors as a function of bias and temperature is shown in Figs. 7 and 8 for dark and light respectively. Note that SiC and other wide bandgap semiconductor transistors are often biased at 10 V or higher so this voltage range is required for SiC circuits. It is seen that the leakage current increases with increasing temperature, and it is higher for both negative and positive bias with the light on, which would imply a reduction in SiC resistivity with the light on.

The reduced attenuation and increased leakage current, with its implied reduction in SiC resistivity, with the light on are contradictory conclusions. Also, the fact that the attenuation increases linearly with temperature above 400 K only if the light is on indicates that there are other factors influencing the CPW propagation characteristics.

It has been reported that the trap density in 6H SiC substrates is approximately 10^{12} traps/cm² eV [9] and that the trapping time constants are long, on the order of msec, [10], which implies that they cannot react to short pulses or RF fields. Thus, Van der Pauw and Hall measurements of SiC resistivity will not agree with C-V and pulsed current measurements of resistivity. Lastly, it has been reported that light changes the trapping emission time constant [11], [12], allowing the SiC to better follow a time varying signal and eliminating built up trap charges.

Traps can be detected and measured by performing C-V measurements. If there are no traps, the slope of $1/C^2$ versus V in reverse bias should be independent of temperature and frequency, but if there are traps, the slope will vary with both parameters [13], [14]. We performed C-V measurements and found that the slope varied by 16% at 500 kHz in dark while it varied by only 7% in light as temperature is varied between 300 and 800 K. Also, the slope varied by 56% in light as frequency is varied from 1 kHz to 500 kHz, which indicates that deep level traps exist in the SiC.

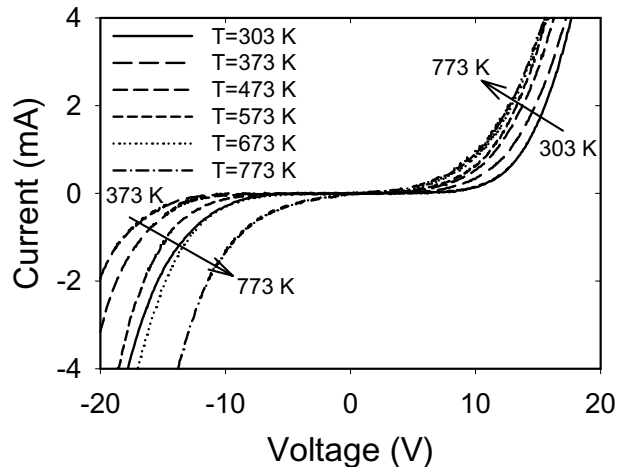


Fig. 7: Measured current between conductors of CPW line on 6H SiC in dark.

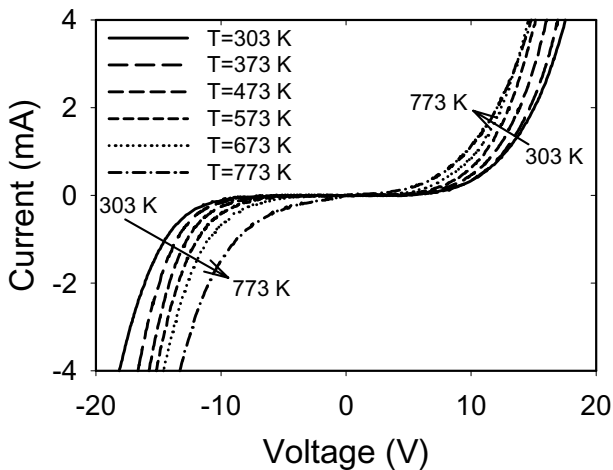


Fig. 8: Measured current between conductors of CPW line on 6H SiC in light.

VII. CONCLUSION

The attenuation of p-type, 6H SiC is too high to use for most microwave applications. There is a strong temperature dependence to leakage current in the 6H SiC, but not in the HPSI 4H SiC. Lastly, and more interesting, these preliminary results indicate that there is a strong influence of traps in the 6H SiC wafer on the CPW propagation characteristics. The authors believe that this is the first time traps in the semiconductor have been shown to influence transmission line characteristics.

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