Analysis of Drain Lag and Power Compression in GaN MESFET

K. Horio and K. Yonemoto

Faculty of Systems Engineering, Shibaura Institute of Technology
307 Fukasaku, Minuma-ku, Saitama 337-8570, Japan

***Abstract* — Two-dimensional transient simulation of a GaN MESFET is performed in which deep levels in a semi-insulating buffer layer is considered. It is shown that the drain voltage V_D is raised, the drain current overshoot the steady-state value, and when V_D is lowered, the drain current remains at a low value for some periods, showing drain lag behavior. This drain lag is shown to become a cause of so-called power compression in the GaN MESFET.**

I. Introduction

Recently, GaN-based FETs have received great interest because of their potential applications to high power and high temperature microwave devices [1]. However, slow current transients are often observed even if the drain voltage or the gate voltage is changed abruptly [2]. This is called drain lag or gate lag, and is problematic in circuit applications. The slow transients mean that the DC *I-V* curves and the AC *I-V* curves become quite different, resulting in lower AC power available than that expected from the DC operation [1],[2]. This is called power compression. These are serious problems, and there are many experimental works reported on these phenomena. But to our knowledge, few theoretical works have been reported for GaN-based FETs, although several numerical analyses were made for GaAs-based FETs [3]-[6]. So, in this work, we have made transient simulation of a GaN MESFET in which deep levels in a semi-insulating buffer layer is considered, and discussed how the lag phenomena and the power compression could be reproduced.

II. Model

Fig.1 shows a device structure analyzed in this study. The donor density in the active layer is 2×10^{17} cm^{-3}, and its thickness is 0.2 μm. As a model for the semi-insulating buffer layer, we use a three level compensation model which includes a shallow donor, a deep donor and a deep acceptor. Some experiments show that two levels (E_C – 1.75 eV, E_C – 2.85 eV) are associated with current collapse (or power compression) in GaN-based FETs with the semi-insulating buffer layer [2], so that we use energy levels of E_C – 2.85 eV (or E_V + 0.6 eV) for the deep acceptor and of E_C – 1.75 eV for the deep donor. Other experiments show shallower energy levels for the deep donor [7],[8], and hence we vary the deep donor's energy level (E_{DD}) as a parameter. Here, the deep donor's density (N_{DD}) and the deep acceptor's density (N_{DA}) are typically set to 5×10^{16} cm^{-3} and 2×10^{16} cm^{-3}, respectively.

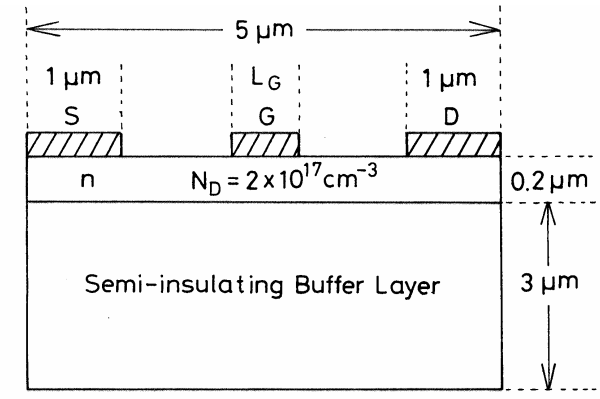

Fig.1. Device structure analyzed in this study.

Basic equations to be solved are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels. They are expressed as follows.

1) Poisson's equation

$$\nabla^2\psi = -\frac{q}{\varepsilon}(p - n + N_D + N_{DD}^+ - N_{DA}^-) \tag{1}$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - (R_{n,DD} + R_{n,DA}) \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p - (R_{p,DA} + R_{p,DA}) \tag{3}$$

where

$$R_{n,DD} = C_{n,DD} N_{DD}^+ n - e_{n,DD}(N_{DD} - N_{DD}^+) \tag{4}$$

$$R_{n,DA} = C_{n,DA}(N_{DA} - N_{DA}^-)n - e_{n,DA} N_{DA}^- \tag{5}$$

$$R_{p,DD} = C_{p,DD}(N_{DD} - N_{DD}^+)p - e_{p,DD} N_{DD}^+ \tag{6}$$

$$R_{p,DA} = C_{p,DA} N_{DA}^- p - e_{p,DA}(N_{DA} - N_{DA}^-) \tag{7}$$

3) Rate equations for the deep levels

$$\frac{\partial}{\partial t}(N_{\mathrm{DD}} - N_{\mathrm{DD}}^{+}) = R_{n,\mathrm{DD}} - R_{p,\mathrm{DD}} \tag{8}$$

$$\frac{\partial}{\partial t} N_{\mathrm{DA}}^{-} = R_{n,\mathrm{DA}} - R_{p,\mathrm{DA}} \tag{9}$$

where N_{DD}^{+} and N_{DA}^{-} represent ionized densities of deep donors and deep acceptors, respectively. C_n and C_p are the electron and hole capture coefficients of the deep levels, respectively, e_n and e_p are the electron and hole emission rates of the deep levels, respectively, and the subscript (DD, DA) represents the corresponding deep level. The above equations are put into discrete forms and are solved numerically.

III. Results and Discussions

Fig.2 shows calculated drain-current responses of the GaN MESFET when the drain voltage V_{D} is raised from 0 V (V_{Dini}) to V_{Dfin}, where the gate voltage V_{G} is kept constant (0 V). Here $E_{\mathrm{C}} - E_{\mathrm{DD}}$ is 1.0 eV. When V_{Dfin} is 6 to 10 V, the drain currents become constant temporarily around $t = 10^{-10}$ s ("quasi-steady state" [3]), and begin to decrease gradually after some time, reaching real steady-state values. For $V_{\mathrm{Dfin}} = 20$ V, the quasi-steady state is not observed, and for $V_{\mathrm{Dfin}} = 2$ V, no slow transients are observed. It is understood that when V_{D} is raised enough, electrons are injected into the buffer layer, and hence the drain currents overshoot. The quasi-steady state is regarded as a state where the deep levels in the buffer layer are not responding. When the deep donors in the buffer layer begin to capture injected electrons, the drain currents begin to decrease, showing the slow current responses (drain lag).

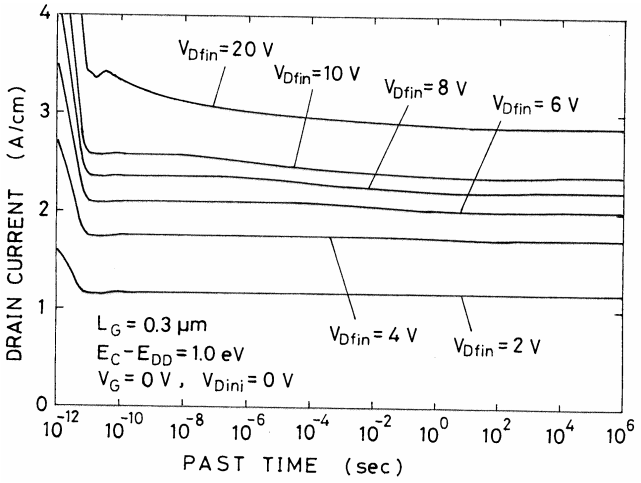

Fig.2. Calculated drain-current responses of GaN MESFET when V_{D} is raised from 0 V to V_{Dfin}. $V_{\mathrm{G}} = 0$ V. $E_{\mathrm{C}} - E_{\mathrm{DD}} = 1.0$ eV.

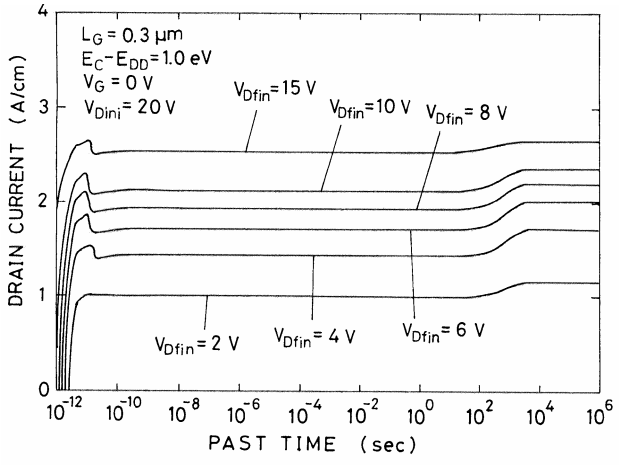

Fig.3. Calculated drain-current responses of GaN MESFET when V_{D} is lowered from 20 V to V_{Dfin}. $V_{\mathrm{G}} = 0$ V. $E_{\mathrm{C}} - E_{\mathrm{DD}} = 1.0$ eV.

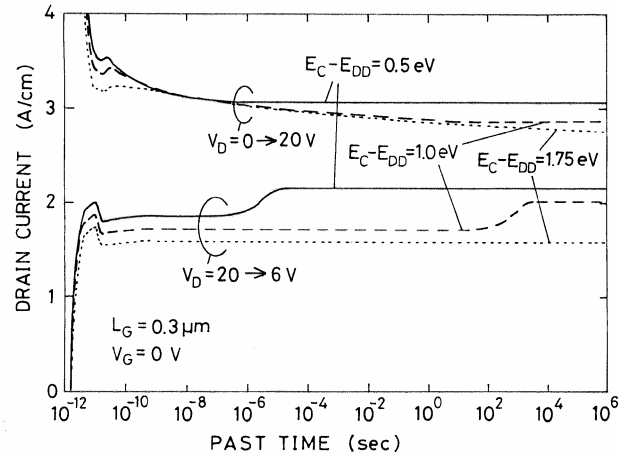

Fig.4. Comparison of drain-current responses of GaN MESFET as a parameter of deep donor's energy level E_{DD}.

Fig.3 shows the calculated drain-current responses when V_{D} is lowered from 20 V (V_{Dini}) to V_{Dfin}, where V_{G} is kept 0 V. Here $E_{\mathrm{C}} - E_{\mathrm{DD}}$ is 1.0 eV. It is seen that the drain currents remain at low values for some periods, and begin to increase slowly around $t = 10^{2}$ s, showing drain lag behavior. This is due to the slow response of the deep donor. It is understood that the drain currents begin to increase as the deep donors begin to emit electrons.

Fig.4 shows a comparison of the drain-current responses when the deep donor's energy level E_{DD} is varied. For relatively shallow E_{DD} of 0.5 eV, the responses are rather fast, and the drain currents reach the steady-state values around $t = 10^{-5}$ s both when V_{D} is raised and when V_{D} is lowered. On the other hand, for deep E_{DD} of 1.75 eV, electron emission from the deep donor occurs quite slowly, and the drain current remains at a low value even at 10^{6} s.

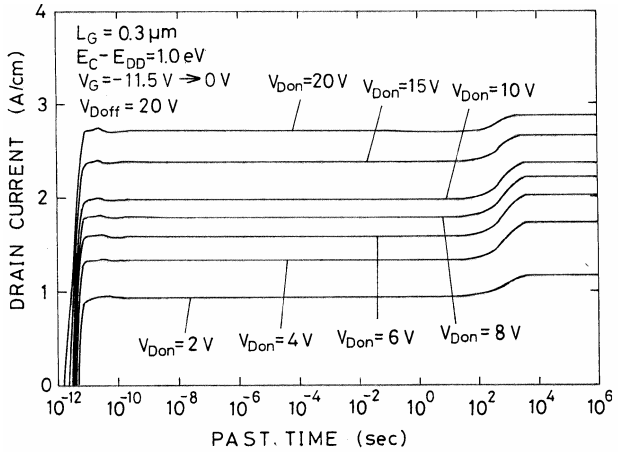

Fig.5. Calculated turn-on characteristics of GaN MESFET when V_G is changed from threshold voltage V_{th} (= – 11.5 V) to 0 V, with on-state drain voltage V_{Don} as a parameter. Off-state drain voltage V_{Doff} is 20 V. $E_C - E_{DD}$ = 1.0 eV.

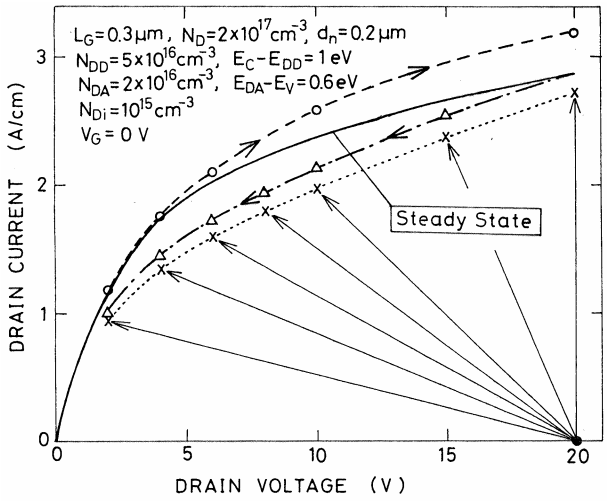

Fig.6. Steady-state *I-V* curve (V_G = 0 V) and quasi-pulsed *I-V* curves for GaN MESFET. (x): V_{Doff} = 20 V and V_{Goff} = V_{th} (t = 10^{-6} s; Fig.5), (○): V_{Dini} = 0 V and V_G = 0 V (t = 10^{-9} s; Fig.2), (Δ): V_{Dini} = 20 V and V_G = 0 V (t = 10^{-6} s; Fig.3).

We have next calculated a case when V_D and V_G are both changed abruptly [9],[10]. Fig.5 shows the turn-on characteristics ($E_C - E_{DD}$ is 1.0 eV) when V_G is changed from the threshold voltage V_{th} (– 11.5 V) to 0 V. The off-state drain voltage V_{Doff} is 20 V, and the parameter is the on-state drain voltage V_{Don}. The characteristics are similar to those in Fig.3, and hence the change of drain voltage is essential in the characteristics, although some transients are seen when only V_G is changed (V_{Don} = 20 V in Fig.5). Fig.6 shows calculated I_D-V_D curves. In this figure, we plot by point (x) the drain current at t = 10^{-6} s after the gate voltage is switched on. This is obtained from Fig.5, and this curve corresponds to a quasi-pulsed *I-V* curve with pulse width of 10^{-6} s. (We are also plotting other quasi-pulsed *I-V* curves by using Figs.2 and 3.) It is seen that the drain currents in the pulsed *I-V* curve are rather lower than those in the steady state. This indicates that the power compression could occur due to the slow response of deep levels in the semi-insulating buffer layer.

IV. Conclusion

We have simulated the transient characteristics of a GaN MESFET on the semi-insulating buffer layer, where the three level compensation model is used. Particularly, the drain lag behavior (when the drain voltage is lowered) has been reproduced, and it is attributed to the slow response of the deep donor. It has also been shown that this drain lag becomes a cause of power compression in the GaN MESFET.

References

[1] U. K. Mishra, P. P. Parikh and Y.-F. Wu, "AlGaN/GaN HEMTs — An overview of device operation and applications", *Proc. IEEE*, vol.90, pp.1022-1031, 2002.

[2] S. C. Binari, P. B. Klein and T. E. Kazior, "Trapping effects in GaN and SiC Microwave FETs", *Proc. IEEE*, vol.90, pp.1048-1058, 2002.

[3] K. Horio and Y. Fuseya, "Two-dimensional simulations of drain-current transients in GaAs MESFET's with semi-insulating substrates compensated by deep levels", *IEEE Trans. Electron Devices*, vol.41, pp.1340-1346, 1994.

[4] S. H. Lo and C. P. Lee, "Analysis of surface state effect on gate lag phenomena in GaAs MESFET's", *IEEE Trans. Electron Devices*, vol.41, no.9, pp.1504-1512, 1994.

[5] K. Kunihiro and Y. Ohno, "A large-signal equivalent circuit model for substrate-induced drain-lag phenomena in HJFET's", *IEEE Trans. Electron Devices*, vol.43, no.9, pp.1336-1342, 1996.

[6] K. Horio and T. Yamada, "Two-dimensional analysis of surface-state effect on turn-on characteristics in GaAs MESFET's", *IEEE Trans. Electron Devices*, Vol.46, no.4, pp.648-655, 1999.

[7] W. Kruppa, S. C. Binari and K. Doverspike, "Low-frequency dispersion characteristics of GaN HFETs", *Electron. Lett*., vol.31, pp.1951-1952, 1995.

[8] H. Morkoc, *Nitride Semiconductors and Devices*, Springer-Verlag, 1999.

[9] D. Kasai, Y. Kazami, Y. Mitani and K. Horio, "Physics-based device simulation of lag and power compression in GaAs FETs", *Proceedings of the 11th European Gallium Arsenide & Other Semiconductor Application Symposium (GAAS 2003)*, Munich, Germany, pp.235-238, 2003.

[10] Y. Kazami, D. Kasai and K. Horio, "Numerical analysis of slow current transients and power compression in GaAs FETs", to be published in *IEEE Trans. Electron Devices*, vol.51, 2004.