A Differential-Based Single-Ended 2 GHz Low-Noise Recursive Filter on Silicon

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Abstract — **In this paper, we present a novel single-ended active integrated bandpass filter employing recursive principles. This circuit is based upon an original method to combine input and delayed feedback signals of a first-order recursive structure thanks to a differential pair combination. The chip surface is 1.12 mm². The filter performs a simulated gain close to 10 dB with a 160 MHz bandwidth. Power consumption is about 32 mW. Noise figure is 4.6 dB at the center frequency. Philips QUBIC4 Si BiCMOS technology is used [1].**

I. INTRODUCTION

Off-chip passive filters are actually widely used in RF receivers front-ends. However, these filters are often expensive and occupy an important surface. A promising alternative solution has found interest through the use of active integrated filters that can simultaneously replace in a single chip a bandpass filter and a low noise amplifier. This approach leads to more compact and lower cost circuits. Among all the possible implementations and techniques proposed through articles, recursive and transversal topologies have been widely developed because of their low frequency digital origins.
In this article, we propose an original 2 GHz single-ended first-order recursive filter integrated using a silicon MMIC process and based on the differential recombination of input and delayed feedback signals within the recursive structure.

II. THEORETICAL BACKGROUND

The concept of recursive filters has been mainly developed at low frequencies for digital applications. However, as demonstrated in [2], it can also be applied to microwave analogue filters.

Fig. 1 presents the flow graph of a first-order recursive filter. For such circuits, the transfer function is expressed as :

$$H(f) = \frac{a_0}{1 + b_1.e^{-j2\pi f\tau}} \qquad (1)$$

When implementing that kind of filter, one of the major issues that must be faced is the summation of signals within the structure. Several different solutions have been proposed such as voltage matching between the different elements [3] or lumped and distributed power splitters /combiners [4-7]. In this paper, we propose an original solution based on the use of a differential structure. Fig. 2 presents the basic principle of the circuit.

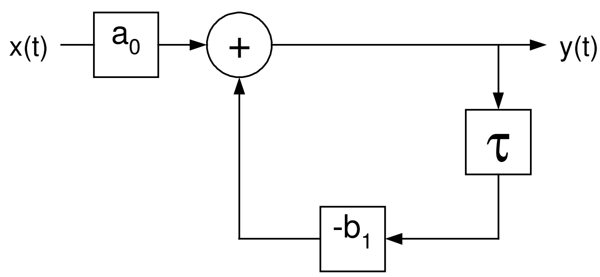

Fig. 1 Flow graph of a first-order recursive filter

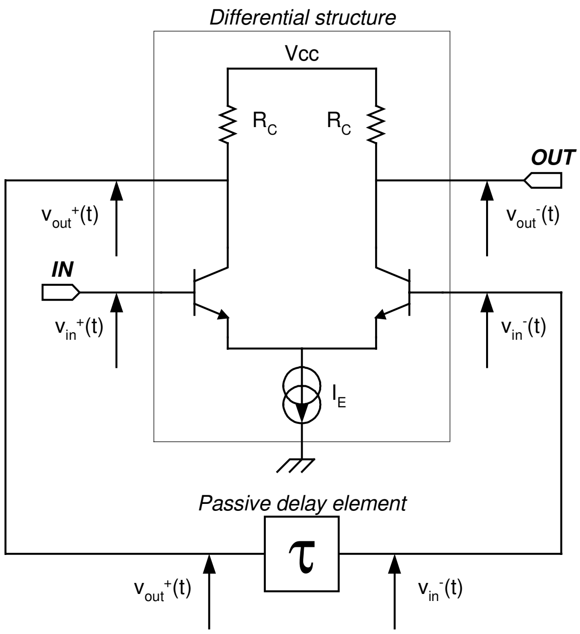

Fig. 2 Scheme of a differential-based recursive filter

Considering voltages at the input/output of the circuit, and in the feedback branch, we can write :

$$\begin{cases} v_{in}(t) = v_{in}^{+}(t) \\ v_{out}(t) = v_{out}^{-}(t) \\ v_{in}^{-}(t) = v_{out}^{+}(t-\tau) \end{cases} \qquad (2)$$

Considering an ideal differential structure (i.e. common-mode is totally rejected, only differential mode is present at the output), it can be derived :

$$v_{out}^{+}(t) = -v_{out}^{-}(t) \quad (3)$$

and

$$\begin{aligned} & v_{out}^{d}(t) = A_d . v_{in}^{d}(t) \\ \Leftrightarrow\ & v_{out}^{+}(t) - v_{out}^{-}(t) = A_d . v_{in}^{+}(t) - A_d . v_{in}^{-}(t) \end{aligned} \quad (4)$$

where A_d represents the differential mode voltage gain.

Then, by injecting (2) and (3) in (4), the voltage gain of the filter can be written as:

$$G_v(f) = \frac{V_{out}(f)}{V_{in}(f)} = \frac{-\frac{A_d}{2}}{1 + \frac{A_d}{2} . e^{-j2\pi f \tau}} \quad (5)$$

Comparing (5) with (1) shows that the structure of Fig. 2 clearly describes a first-order recursive filter response corresponding to the structure of Fig. 1.

III. Implementation

To achieve stability, a recursive filter must satisfy the condition $b_1 < 1$ which, in our case and referring to equations (1) and (5), leads to $A_d / 2 < 1$.

This condition implies that the standard differential amplifier presented in Fig. 2 is not suitable for this application due to its important voltage gain. The only possible choice is then to use a differential "common-collector" structure, so-called because the transistor pair is connected by the collectors. This structure, presented in Fig. 3, will ideally exhibit a unity gain, and is also useful to achieve 50-Ohm output matching, as the output impedance presented by a common collector structure is significantly lower than that of a classic common emitter topology.

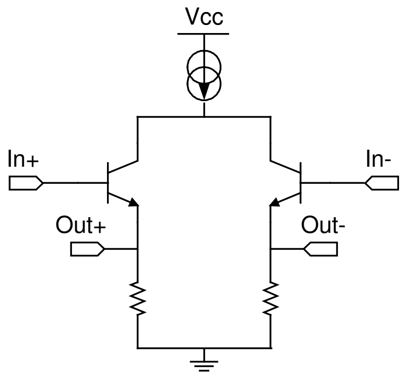

Fig. 3 Schematic view of the differential structure

Basically, a recursive filter response selectivity is directly driven by the delay-time parameter value. Because of the characteristics of the inductors and capacitors used for the delay-time (i.e. the losses), the global selectivity of the filter is generally lower. To minimise the problem, the inductors have been designed and optimised using an electromagnetic simulator. In this way, the main inductor, including its access lines, performs a series resistance of 0.76 Ω for an inductance value of 1.5 nH.

Moreover, the complete structure also includes standard single-ended common-emitter structures at each input of the differential circuit.

The first one is placed at the input of the whole circuit and acts as an input buffer. It is used to increase isolation, achieve 50-ohm input matching, and set the overall gain.

The second one, inserted at the output of the passive delay element, helps to achieve the time shifting, and to partially compensate losses of the inductor and capacitors.

Schematic of the complete circuit is presented in Fig. 4.

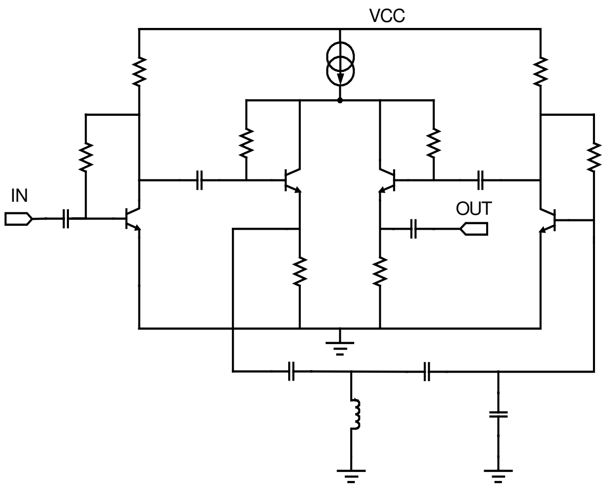

Fig. 4 Simplified schematic view of the global circuit

The circuit realised is presented in Fig. 5. Layout dimensions are 1.12 x 1 mm². However, as it can be seen in Fig. 5, an important space on the chip is either occupied by the inductors, or empty (top-right part of the circuit). The active part, visible at the centre of the chip occupies only 140 x 100 µm², which represents about 1 percent of the global area.

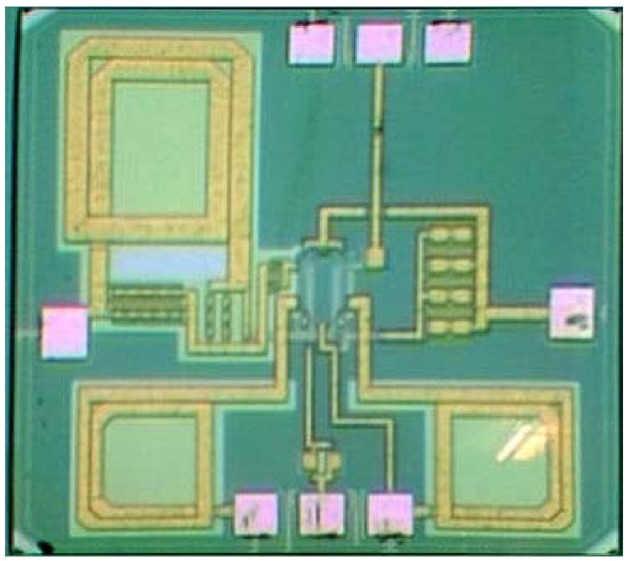

Fig. 5 Chip micrograph

Electromagnetic simulations were performed in order to ensure the absence of magnetic coupling between the 3 inductors present in the circuit.

IV. MEASUREMENTS

Computed S-parameters of the circuit are presented in Fig. 6 and Fig. 7. The filter exhibits a 160 MHz 3-dB bandwidth at 1.96 GHz, with a gain close to 10 dB for a power consumption of 32 mW. Input and output matchings are lower than –10 dB for nearly 800 MHz around the centre frequency. Isolation, which is not presented here, is greater than 30 dB in the [0.5 ; 3.5] GHz range. Noise figure is equal to 4.6 dB @ f_0.

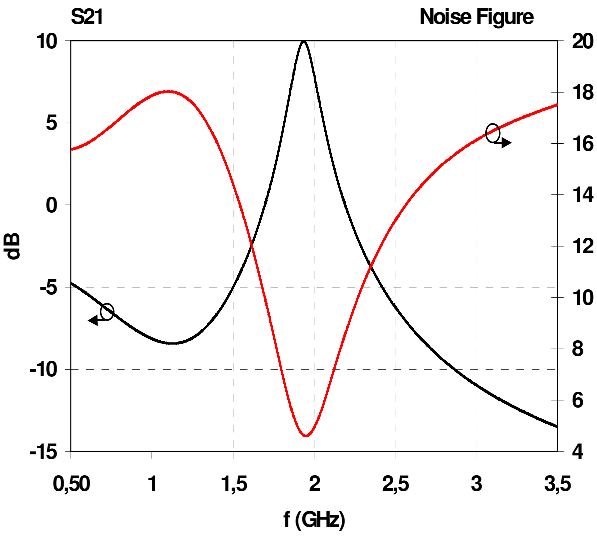

Fig. 6 Simulated gain and noise figure of the circuit

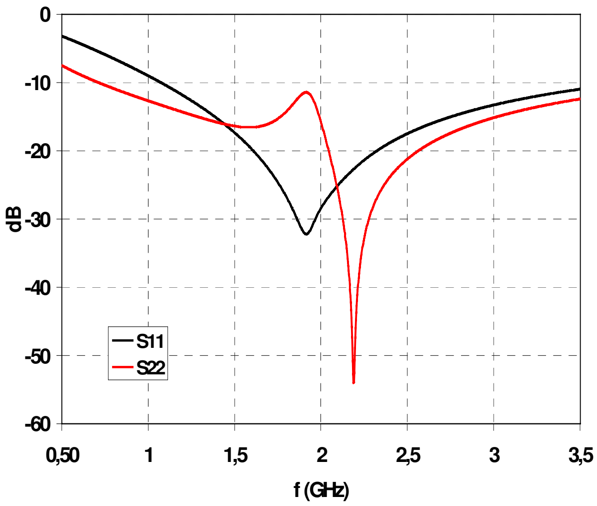

Fig. 7 Simulated input/output matching of the circuit

The -1dB compression point simulation result is presented in Fig.8. It is obtained for an output power of –11.7 dBm, and IP3 for 13.31dBm.

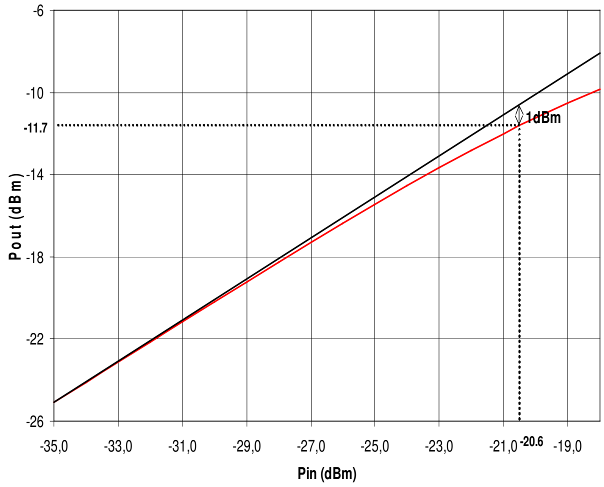

Fig. 8 Simulated –1dB compression point

Measurements results are presented in Figs. 9 and 10. They show a good agreement with simulations for input/output matching, gain and isolation. Centre frequency was measured at 1.94 GHz, very close to what had been obtained during simulations. This parameter confirms the validity of the method used for the design of the inductors.

However, the circuit is not as selective as awaited at the lower side of the response (i.e. before the centre frequency), thus leading to a 260 MHz 3-dB bandwidth instead of the 160 MHz expected. Noise characterisation has not been realized yet.

Power consumption is as scheduled with 35 mW at 2.7 V. The results obtained for the linearity characterisation are also comparable with simulations, with a –14.5 dBm output referred –1dB compression point. IP3 was not measured.

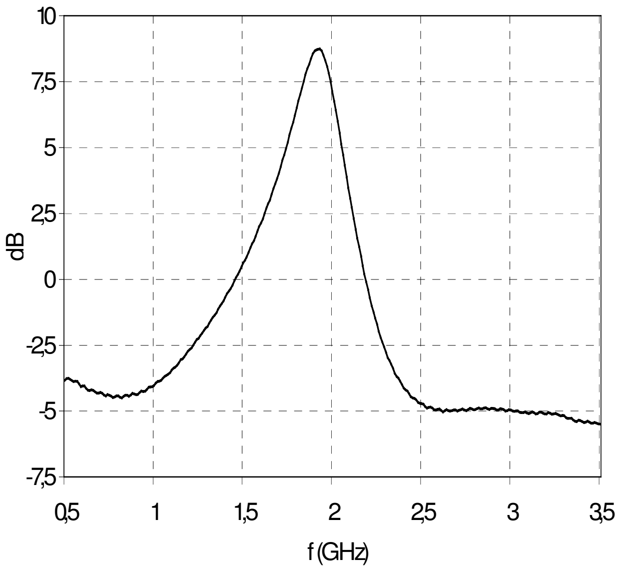

Fig. 9 Measured gain of the circuit

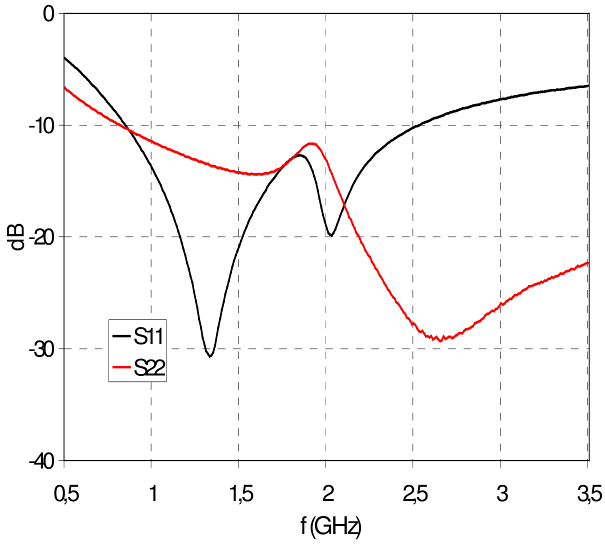

Fig. 10 Measured input/output matching

V. Conclusion

In this article, we have presented an original single-ended first-order recursive filter. The originality of this work resides in the way of combining the elementary signals within the structure by using the input ports of a differential stage. This circuit performs a simulated gain of 10 dB (9 dB measured) with a 160 MHz bandwidth (260 MHz measured). Measured power consumption at 2.7V is 32 mW. Simulated noise figure is about 4.6 dB at the centre frequency. P_{-1dB} is obtained for an output power of –11.7 dBm. The overall chip surface 1.12 mm².

Acknowledgment

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