A Miniature 4.3-7-GHz, 1-V CMOS LNA with Helical Inductors

Ming-Da Tsai, Huei Wang, Jui-Feng Kuan*, Chih-Ping Chao*

Department of Electrical Engineering and Graduate Institute of Communication Engineering,
National Taiwan University, Taipei, Taiwan, R.O.C.
Phone: +886-2-23635251 ext.317 Fax: +886-2-23638247 e-mail: hueiwang@ew.ee.ntu.edu.tw
*Taiwan Semiconductor Manufacturing Corporation, Hsinchu, Taiwan, ROC

***Abstract* — A fully-integrated 4.3-7 GHz CMOS low-voltage wideband low-noise amplifier with helical inductors has been demonstrated in this paper. The CMOS LNA, operating at a supply voltage as low as 1 V, achieves a small signal gain of 14 dB and 3-dB bandwidth from 4.3 to 7 GHz. The minimum noise figure is 2.9 dB at 6 GHz. With the benefits of helical inductors, the total effective chip size is only 0.2 mm^2.**

I. Introduction

The CMOS RF chips are getting more attractive due to the advantages of low cost and integration ability with baseband circuitry. As the supply voltage of the digital circuitry becomes smaller with technology scaling, RF circuit topologies that operate at voltages at or below 1 V are required. This is because integration of analog/RF and digital circuitry on the same die is desirable from both cost and packaging considerations. LNAs using CMOS process have demonstrated good gain and noise performance in the 5-6 GHz ISM band [1]-[6]. The typical CMOS LNA topology is cascode with the source inductance degeneration [1]-[2]. One of the drawbacks of cascode topology is the undesirable relative high supply voltage. In order to support low-voltage design, folded-cascode topology can also be chosen for CMOS LNA with the benefits of controllable gain at the expense of poor performances of PMOS transistor [3]-[4]. Recently, a transformer feedback CMOS LNA is proposed at low-voltage operation [6] with a narrow bandwidth.

In this paper, a miniature wideband 1-V CMOS was presented. A two-stage cascaded topology was chosen for low-voltage design. Instead of the monolithic planar inductors, we first proposed the helical inductors for the CMOS LNA to reduce the chip size. Table 1 summarizes the recently performances of CMOS LNA compared with this work. It is observed our chip demonstrated the widest bandwidth with smallest effective chip area for a CMOS LNA operating at 5-GHz ISM band. The miniature CMOS LNA achieves 14-dB power gain with a 3-dB bandwidth from 4.3 to 7 GHz, operating at 1 V supply voltage and 17 mW power consumption. The measured noise figure has minimum value of 2.9 dB at 6 GHz, and below than 3.2 dB from 4.3 to 7 GHz. The effective chip area is only 0.2 mm^2 using a 0.18-μm CMOS commercial MS/RF process.

Process	Frequency (GHz)	BW (MHz)	NF (dB)	Gain (dB)	Effective chip size (mm^2)	P_{DC} (mW)	Power Supply	Design Features	Ref.
0.25μm CMOS	5.25	840	2.5	16	0.32	48	3 V	cascode	[1]
0.25μm CMOS	4.5-6	1500	< 3 (2.2 at 5.3 GHz)	10	-	10	2 V	cascode, substrate thinning	[2]
0.18μm CMOS	5.8	-	2.5	13.2	0.72$^+$	22.2	1 V	folded-cascode	[3]
0.18μm CMOS	4.5-6	1500	3.5	20	0.8 / 1.2$^+$	17	1 V	folded-cascode, splitting matching	[4]
0.18μm CMOS	5.7	1600	3.7	12.5	1.39$^+$	14.4	1.8 V	off-chip matching, current reuse	[5]
0.18μm CMOS	5.7-5.85	≧150	< 6 (0.9 at 5.75 GHz)	14.2	0.24	16	1 V	Transformer-Feedback	[6]
0.18μm CMOS	4.3-7	2700	< 3.2 (2.9 at 6 GHz)	14	0.2 / 0.37$^+$	17	1 V	Cascaded, Helical Inductors	This Work

Table 1. Recently reported performance of CMOS low noise amplifiers. BW: 3-dB bandwidth. $^+$: chip size including testing pads.

II. Circuit Design and Fabrication

The miniature low-voltage CMOS LNA was fabricated using TSMC's 0.18-μm MS/RF CMOS technology [7]-[8], which provides single poly layer for the gates of the MOS and six metal layers for inter-connection. The substrate conductivity is approximately 10 S/m. With optimized CMOS technology and deep n-well, this technology provides a f_T and f_{max} of better than 60 and 55 GHz, respectively. MIM capacitors with 1fF/mm^2 were fabricated using oxide inter-metal dielectric. Two types of polysilicon resistors, with several Ω/□ and kΩ/□, are provided by choosing the individual dose of ion-implantation separately form the gate electron doping process.

High-Q inductors can be formed using the top AlCu metallization layer of 2-μm thickness without additional process steps. In the case of the used monolithic inductors, helical inductor occupies less silicon area than that of planar spiral since the turn is expanded vertically as depicted in Fig. 1. Usually, top metal is thicker than the lower metal layers, and thus Q-factor of helical inductor would be lower than that of planar spiral inductor. However, the area of helical inductor is much smaller. Furthermore, smaller area gives smaller substrate loss, so only little performance degradation of the helical inductor over the planar spiral inductor in circuit is expected [9]. For example, a 2-nH of helical inductor can achieve peak quality factor of 8 at 5 GHz and self-resonance frequency of 16 GHz [10]. With the benefits of helical inductors, the chip size can be reduced.

The typical CMOS LNA topology is cascode with the source inductance degeneration with the shortcoming of the relative high supply voltage. Since the drain of the common-source stage is terminated with the source of the common-gate device, the gain of the common-source stage is not high enough and the total noise performance will be degraded by the noise by the common-gate stage.

To achieve low supply voltage and avoid noise performance degradation, a common-source topology is adopted as in Fig. 2. The input matching condition and noise performance of an inductive degeneration topology with ideal inductors was fully analyzed in [13], and the parasitic resistance was also considered in [12]. The input impedance is

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + R_g + R_{Lg1} + R_{Ls1} + \frac{g_{m1}}{C_{gs1}} L_{s1} \qquad (1)$$

where C_{gs} is the gate-source capacitance and g_{m1} is the transconductance of transistor M_1. R_g is the effective gate resistance. R_{Lg1} and R_{Ls1} are the parasitic resistance of the inductors L_{g1} and L_{s1}. The matching condition occurs when

$$\omega^2 C_{gs}(L_g + L_s) \simeq 1 \qquad (2)$$

$$R_s = R_g + R_{Lg1} + R_{Ls1} + \frac{g_{m1}}{C_{gs}} L_s \qquad (3)$$

A two-stage topology is used to simultaneously optimize the gain and noise performances as in Fig. 2. The first stage is designed for noise performance and the second stage is designed for power gain. The transistor size of the first stage is 160μm/0.18μm, and the second stage is 80μm/0.18μm. The inter-stage is complex conjugate matched achieved by the inter-stage inductor L_{g2}, the drain inductor L_{d1} and the shunt capacitor C_1. The inductance of L_{g2} and L_{d1} is 2.5 and 1.6 nH, respectively, and the shunt capacitor C_1 is 80 fF. The output impedance matching network is shunt-inductor L_{d2} and series-capacitor C_2. In order to accomplish the fully-integrated circuit, the parasitic capacitance of I/O pads must also be considered. The I/O pads are performed by top metal with bottom ground-shielding metal. With the benefits of helical inductors, the effective chip size of this miniature CMOS LNA is only 0.2 mm^2 fabricated using a commercial 0.18-μm CMOS process, shown as Fig. 3.

III. Measurement Results

The circuit was measured via on-wafer probing without bias-T due to the fully-integrated characteristic. The small signal performances are measured through Agilent 8510C network analyzer. Fig. 4 shows the measured results of small signal gain ($|S_{21}|$) and input return loss ($|S_{11}|$). With a power consumption of around 17 mW from a 1 V supply, the small signal gain is 14 dB with a 3-dB bandwidth of 2.7 GHz from 4.3 to 7 GHz. The input return loss is better than 10 dB from 5 to 7.6 GHz. Fig. 5 shows the measured noise figure and output return loss ($|S_{22}|$). The noise figure has minimum value of 2.9 dB at 5.6 GHz and below than 3.2 dB from 4.3 to 7 GHz. The output return loss is better than 5 dB at frequencies above 4.5 GHz.

IV. Conclusion

A fully-integrated 4.3-7 GHz CMOS low-voltage wideband low-noise amplifier with helical inductors has been demonstrated in this paper. The CMOS LNA, operating at a supply voltage as low as 1 V, achieves a small signal gain of 14 dB and 3-dB bandwidth from 4.3 to 7 GHz. The minimum noise figure is 2.9 dB at 6 GHz and below than 3.2 dB from 4.3 to 7 GHz. With the benefits of helical inductors, the total effective chip size is only 0.2 mm^2. This chip also demonstrated the widest bandwidth CMOS LNA with smallest chip area.

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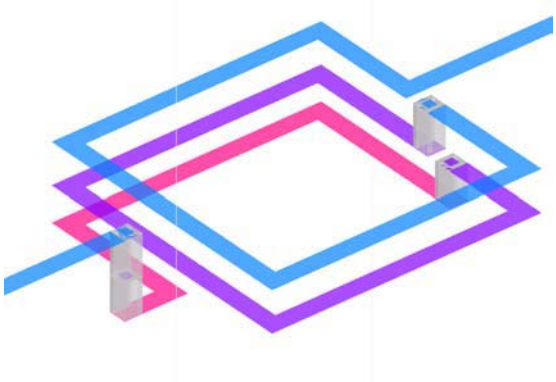

Fig.1 The structure of helical inductor.

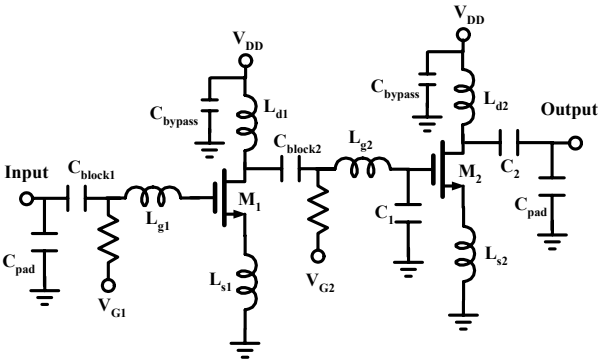

Fig. 2. Circuit schematic of the low noise amplifier.

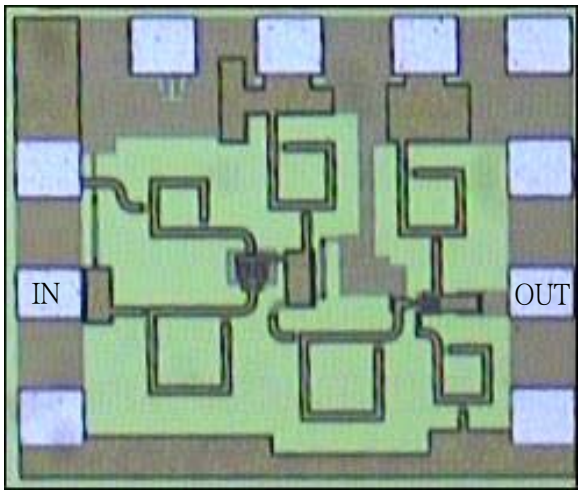

Fig. 3. The die photo of the miniature CMOS LNA with effective chip area of 0.2 mm^2.

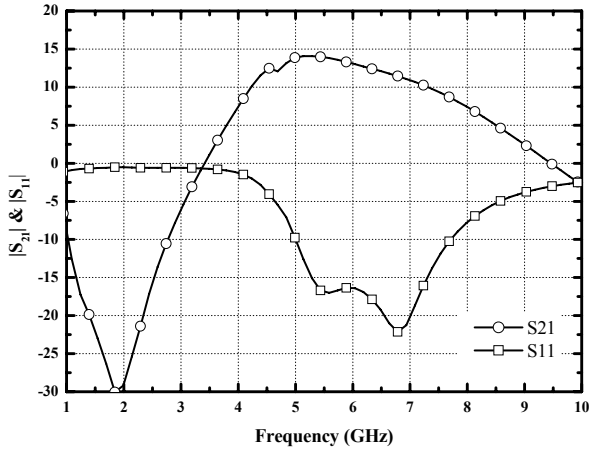

Fig. 4. The measured and simulated results of the power gain and input return loss.

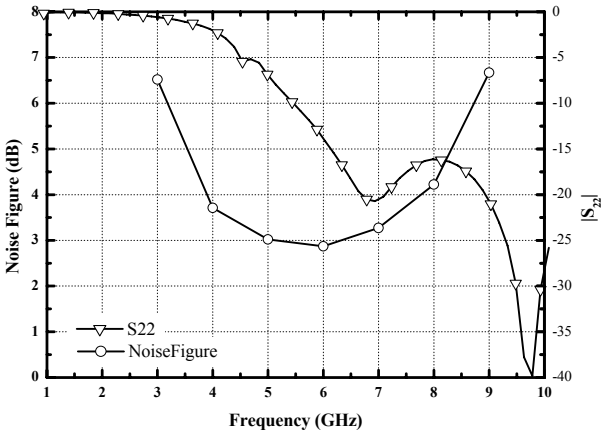

Fig. 5. The measured and simulated results of the noise figure and output return loss.