

A Novel Low Cost Enhancement Mode Power Amplifier MMIC in SMT Package for 7 to 18 GHz Applications

Kohei Fujii, Henrik Morkner, and Edward Brown

Agilent Technologies, Inc. 350 W. Trimble Road, San Jose, California, 95131 USA

Contact: Henrik Morkner, Phone: (408) 435-6513, FAX: (408)435-4801 email: henrik_morkner@agilent.com

Abstract – This paper describes a novel power amplifier based on Enhancement mode PHEMT (E-PHEMT) suitable for low cost 7-18 GHz applications. The designed power amplifier exhibits 20 dB of small signal gain, 30dBm P-1dB output power at 17 GHz. A 50 Ω output match and single 5V supply requirement simplify the application. These MMIC is fabricated in Agilent’s advanced E-PHEMT 0.25u gate process and packaged in a 5x5mm surface mount laminate package for ease in assembly. This is the only known or published E-PHEMT MMIC power amplifier to work at these frequencies for SMT applications.

I. INTRODUCTION

Enhancement mode PHEMT (E-PHEMT) Power Amplifiers (PA) are making serious inroads into handset cellular (800MHz to 2.3 GHz) and WLAN (2.4 GHz and 5.8 GHz) applications [1-4]. The combination of high power added efficiency (PAE) and high digital signal linearity make E-PHEMT MMICs attractive for handheld applications. Modern 6” fabrication combined with volume usage makes E-PHEMT cost competitive with HBT and LD MOS. Application of this technology is not restricted to sub 6 GHz [5]. With the optical placement of a small 0.25u gate a 60 GHz f_T can be realized. This allows the design of wideband, low-cost, PA MMICs that will be crucial to the development of 7-18 GHz commercial wireless links such as Local Multipoint Distribution Service (LMDS), and point-to-point radios.

The combination of a volume 6” stepper based E-PHEMT process, single supply voltage and a laminate SMT package dramatically reduces the cost to the user. This packaged MMIC is easy to use with a 50 Ω output match and single positive voltage supply, yet it delivers top 7-18 GHz performance with over 18 dB of gain, 30 dBm (1W) of output power, and PAE over 20%. Decoupled Vd1 and Vd2 pins (no choke needed) and a temperature compensated power detector voltage output minimize external components.

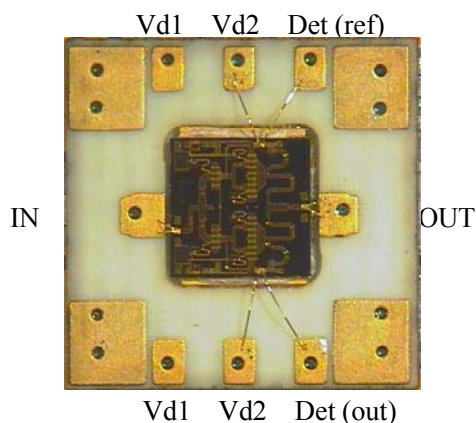


Figure 1. 7-18 GHz E-PHEMT power amplifier in a SMT package (lid removed).

II. E-PHEMT PROCESS AND CAD TOOLS

Agilent’s E-PHEMT process uses a recessed 0.25 μ m gate. The device has a f_T of 60 GHz, at $V_{ds}=2V$, $V_{gs}=0.6V$. DC parameters for the device are shown in Table 1. Plots of G_m and I_{ds} versus V_{gs} are shown in Figure 2. The wafer material is selected for high power and breakdown with some compromises for noise. A Ti/Pt/Au T-gate is used for low input resistance and high-reliability. The process is designed to operate with a DC drain voltage up to 7V. All steps are defined using stepper lithography on 6-inch wafers.

The MMIC process is equipped with passive components which include a 213 Ω/\square bulk resistor, 0.4 fF/ μm^2 Si_3N_4 MIM capacitor, backside via and two metal layers for transmission lines.

Table 1. DC Parameters for the E-PHEMT

Parameter	Mean
Gm (mS/mm)	580
Vgs @ peak Gm (V)	0.75
Ids @ peak Gm (mA/mm)	240
Imax (mA/mm) @ $V_{gs}=0.9V$	350
BVgd @ 1mA/mm (V)	-20
Vto @ 1mA/mm (V)	0.9
Vth (V)	0.1

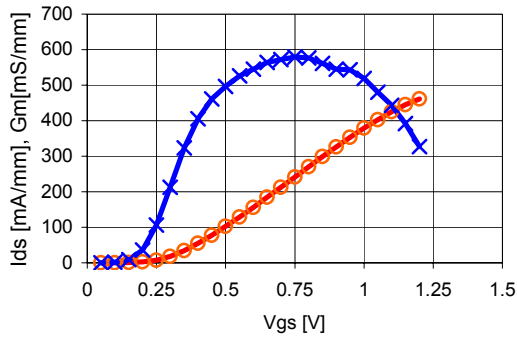


Figure 2. A plot of G_m and I_{ds} versus V_{gs} for the E-PHEMT device at $V_{ds}=2V$

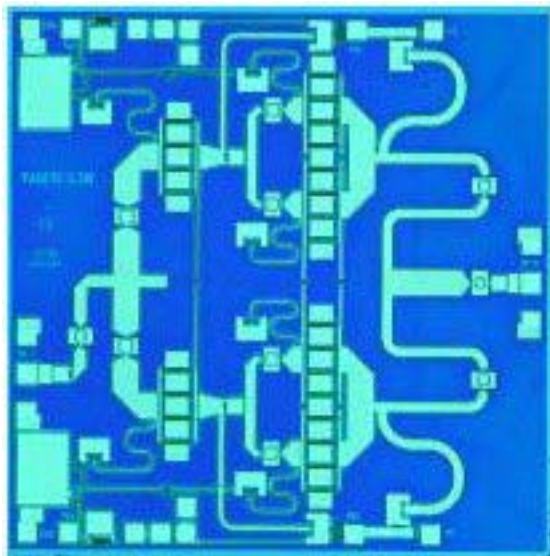


Figure 3. Layout of the power amplifier (2 x 2mm)

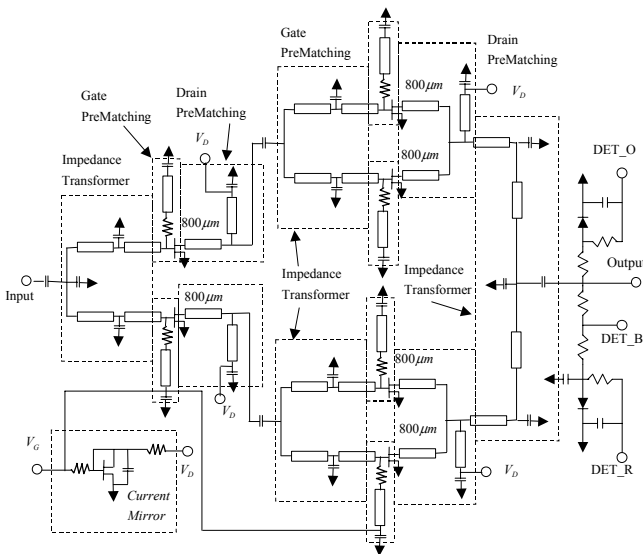


Figure 4. Schematic for the power amplifier

III. POWER AMPLIFIER DESIGN

In the PA design, the DC biasing condition should be selected by the best compromise between gain, output power, and gate conduction current. E-PHEMT based amplifier design requires careful selection of the DC biasing condition since the V_{gs} at G_m peak is fairly close to the V_{TO} . This design selected a 32% I_{max} -biasing level. At this bias level, the major cause of the power limitation is the forward conduction current through the gate.

Figure 3 shows a layout of the single-ended amplifier. A simplified schematic diagram of the single-ended amplifier is shown in Figure 4. It consists of a 2-stage, power amplifier design with two 800 μ m E-PHEMT in the first stage driving four 800 μ m E-PHEMTs in the final stages. The 800 μ m E-PHEMT cells are configured internally as eight, 0.25 x 100 μ m gate fingers, and simulated with a large-signal model [6-8]. The input, inter stage and output matching circuits are composed of pre-matching circuits and impedance transformers. Pre-matching circuits decreases the frequency dependence of input and output impedance. In addition a constant resistance network is employed for the input side of the FET and a parallel resonant stub is employed for the output side of the FET [9]. As an impedance transformer, a Chebyshev low-pass filter configuration is employed [10]. A reactive output matching network provides the final stage with optimum load impedance for maximum output power across the band. The optimum load was determined by using a load-pull simulation based on the large-signal model.

The E-PHEMTs are biased with a positive gate voltage provided by the current mirror topology shown in Figure 4. A current mirror makes circuit biasing less sensitive to process variation of the threshold voltage (V_{th}), than a resistor-ladder-network or external fixed supply. A resistor forms a constant current source to set the bias of the current mirror FET.

The result is a high gain, single DC supply power amplifier that operates from 7 to 18 GHz. The MMIC has a partial input and output match to 50 Ω (-5dB to -12 dB return loss). It is unconditionally stable over all frequencies and bias conditions. V_d bias can be applied from either side. Gate voltage is internally set using a current mirror but can be overridden with the V_g pin to optimize for linear or saturated power amplification. A reference and output detector allows differential output power detection over 15 dB of range.

IV. PACKAGE DESIGN

The Package is designed with a 5x5mm dimension and full surface mount capability. It takes into full account the parasitic involved with routing a high frequency signal up and through a ground plane transition. Built with Rogers 4350 material with metal backing it is fully compatible with modern low cost, high volume assembly and test in panel form.

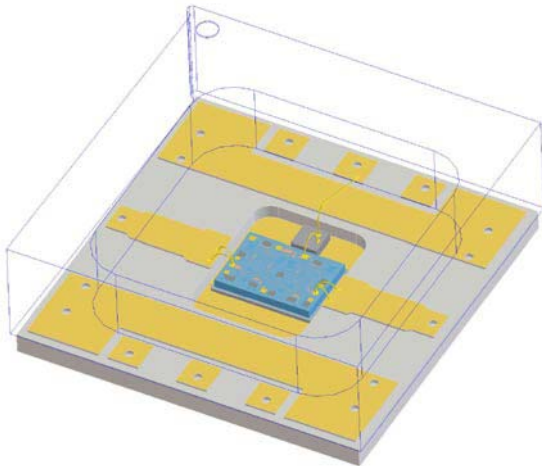


Figure 5. DC-20 GHz low cost package

The I/Os of the package are designed using extensive EEs of HFSS three dimensional simulations were used to carefully design the input and output coplanar to via to micro-strip transitions. The result is a package I/O is capable of maintaining better than 15 dB return loss to 40 GHz. Capacitive compensation is built into the MMIC and the package micro-strip launch to compensate for the bond wire inductance.

The MMIC is assembled using automated bonders in the package while still in panel form. Then lids are epoxy attached forming an air cavity above the device for maximum performance. Last, the panel is 100% tested at microwave frequencies to ensure performance for the customer.

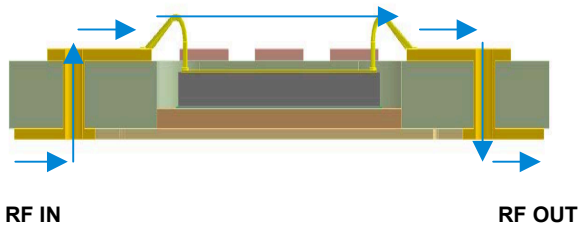


Figure 6. DC-20 GHz low cost package

V. MEASURED RESULTS

For the small-signal measurement, the PA was biased at $V_{ds}=6V$ and $I_d=35\% I_{max}$, and tested on-wafer environment. The small-signal data for the single-ended amplifiers is shown in Figure 7 over the 3 to 21 GHz frequencies. The PA demonstrated a gain of typically 18 dB from 7 to 18 GHz.

Measured output power (P-1) and the power added efficiency (PAE) at 1dB gain compression are shown in Figure 8. The amplifier demonstrated more than 30dBm output power at 1dB gain compression point (P-1) over the 7 to 18GHz frequencies. Measured output power (Pout), Gain, and PAE versus input power at Frequency=9GHz. $V_{ds}=6V$, $I_{ds}=35\% I_{max}$ are shown in Figure 9. The amplifier showed 30dBm P-1 with 25% PAE. In this condition, the amplifier requires 1mA forward conduction gate current.

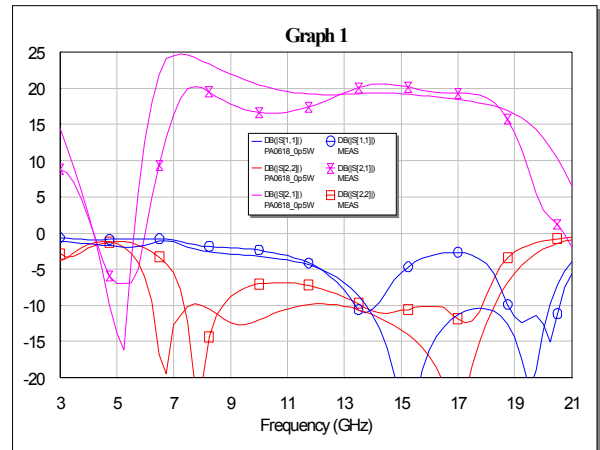


Figure 7. Measured and simulated small-signal performances of the power amplifier, $V_{ds}=5V$, $I_{ds}=35\% I_{max}$

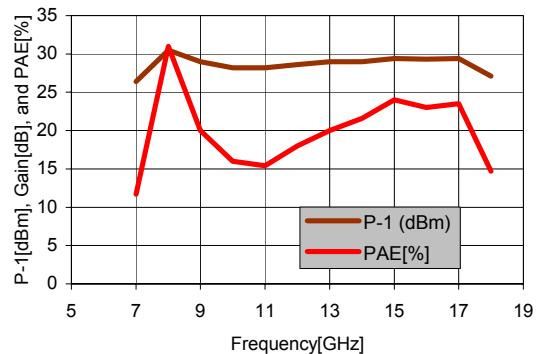


Figure 8. Measured output power and PAE at 1dB gain compression for the power amplifier. $V_{ds}=6V$, $I_{ds}=35\% I_{max}$

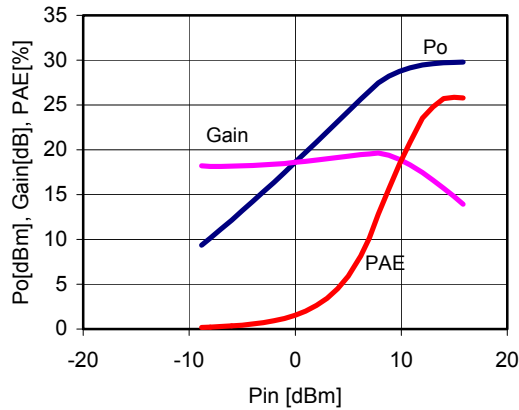


Figure 9. Measured output power (P_{out}), Gain, and PAE versus input power (P_{in}) at Frequency=9GHz. $V_{ds}=6V$, $I_{ds}=35\% I_{max}$

Table 2. Summary of MMIC performance

Sym	Parameters/Conditions	Unit	Typ.	Min/Max
V_d	Drain Supply Voltage	V	5	6
V_g	Gate Voltage (Optional)	V	0.8	
I_D	Drain Supply Current	mA	660	750
Gain	Small-signal Gain	dB	18	15
RL_{in}	Input Return Loss	dB	-5	
RL_{out}	Output Return Loss	dB	-9	
P-1dB	Power @ 1dB Gain Comp	dBm	29	27
Isol	Reverse Isolation	dB	-30	-25
IIP3	Input 3 rd Order Int Point	dBm	+39	
Vdet	Power Detector Voltage	V/W	0.2	

VI. SUMMARY

A 7-18 GHz E-PHEMT power amplifier in SMT package has been built and demonstrated. It provides state-of-the-art 30 dBm power (1W) and 18 dB gain with integrated matching and power detection. It is designed for low cost utilizing a innovative SMT package and volume 6" fabrication facility. The MMIC provides a cost effective alternative to discrete FET designs and chip-and-wire hybrid MMICs. This amplifier provides the best combination of cost, performance, and ease of application than any known product advertised or published.

The authors wish to thank all the people and companies that made this product. This includes: San Jose, California, USA: Hue Tran, Julie Kessler, Mike Vice, Khai Chia, Floyd Oshita, Ro Buted, Irene Armenta, Bob Myers, M. Bruner, Frank Ha Ft. Collins, CO, USA: Chun Lin, Ceceli Wilhelmi Penang, Malaysia: CK Tan, Jimmy Foo United Kingdom: Alan Rixon, Robert Brophy

REFERENCES

- [1] D-W Wu, R. Parkhurst, S-L Fu, J. Wei, C-Y Su, S-S Chang, D. Moy, W. Fields, P. Chye, R. Levitsky, "A 2W, 65% PAE Single-Supply Enhancement-Mode Power PHEMT for 3V PCS Applications" 1997 IEEE MTT-S Digest, pp. 1319-1322, June 1997.
- [2] S. Kumar, M. Vice, H. Morkner, W. Lam, "Enhancement mode GaAs PHEMT LNA with Linearity Control (IP3) and phased matched Mitigated Bypass Switch and Differential Active Mixer," 2003 IEEE MTT-S Digest, pp. 1577-1580, June 2003.
- [3] B-E Seow, L. Nguyen, M. Vice, E. Chan, Y-H Chow, "A high isolation enhancement mode GaAs PHEMT buffer amplifier," 2003 NCTT Proceedings, pp. 58-62, January 2003.
- [4] T. Moriuchi, W. Abey, R. Hajji, W. Kennan, T. Nakamura, S. Maruyama, T. Kitawada, Y. Nonaka, E. Mitani, "A single supply miniature PA MMIC for multi-mode digital handsets using quasi-enhancement mode PHEMT," 2000 GaAs IC Symposium, pp. 29-32, November 2000.
- [5] K. Fujii, H. Morkner, "E-PHEMT, Single Supply, Power Amplifier for Ku Band Applications" 2003 MTT-S Digest, pp. 859-862, June 2003.
- [6] D.E. Root, "Measurement-based mathematical active device modeling for high frequency circuit simulation," IEICE Trans. Electron., vol. E82-C, no. 6, pp. 924-936, June 1999
- [7] J. Wood, and D.E. Root, "Bias-dependent linear scalable millimeter-wave FET model," IEEE Trans. On MTT, vol. 48, no. 12, pp. 2352-2360, December 2000
- [8] K. Fujii, F.M. Gannouchi, T. Yakabe, H. Yabe, "A comprehensive nonlinear GaAs FET model suitable for active and passive circuits design," IEICE Trans. on electron., Vol. E84-C, no. 7, pp. 881-890, July 2001
- [9] Y. Itoh, M. Mochizuki, M. Nii, Y. Kohno, and T. Takagi, "An ultra-broadband monolithic lossy match power amplifier using pre-matching circuits," IEICE Trans. Vol. J78-C-I, no. 12, pp. 664-676, Dec. 1995
- [10] G. L. Matthaei, "Tables of Chebyshev impedance-transforming networks of low-pass filter form," Proc. IEEE, pp. 939-963, 1964.
- [11] Patent: H. Morkner, M. Frank, "A Amplifier/Switch topology for Microwave Applications", 8 Claims, Filed at U.S. Patent Office, Nov 1998
- [12] Henrik Morkner, M. Frank, K. Negus, T. Kao, "A Novel Integrated Microwave Bias Network For Low Cost Multistage Amplifiers", 1997 IEEE MTT-S International Microwave Symposium, TU1A-3, June 1997
- [13] H. Morkner, "Miniature 3V GaAs LNA, VGA, and PA for Low Cost .5-4 Ghz Wireless Applications", 1997 Wireless Symposium, Feb. 1997, pp. 190-195.