A CDMA and AMPS Handset Power Amplifier based on Load Modulation Technique

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ABSTRACT — A new MMIC PA for Cellular & AMPS handsets based on the asymmetric power combining scheme of Doherty amplifier has been developed to boost the efficiency at a low power level. The amplifier has two modes of operation, low and high power modes. At a low power mode, only the main amplifier generates output power and at a high power mode, both the main and auxiliary amplifiers are operational, combining the power efficiently by the load modulation. For the CDMA environment, the amplifier at the low power mode exhibits PAE of 35% and ACLR less than 31dBc at 18.6dBm and the high power mode exhibits PAE of 37.7% and ACLR of 31dBc at 28.4dBm. For the AMPS mode operation, the amplifier delivers 21dBm with PAE of 41.7% and 30.3dBm with 43% in low mode and high mode, respectively.

Ⅰ. Introduction.

There are increasing demands on highly efficient linear amplifiers for mobile handsets. The usual power amplifier delivers maximum efficiency only at near the maximum rated power level of the device (~28dBm), and the efficiency drops drastically to a low value as the output power level is reduced. In the typical CDMA system, the operational output power is less than 17dBm and the power amplifier operates mostly at a low efficiency region. Since the power amplifier in mobile handset consumes a large portion of battery power, it is desirable to have a high efficiency at backed-off power region to extend battery life time. One of the efficiency boosting methods at a low power is load modulation technique described by Doherty [1].

This work presents a new handset power amplifier based on the load modulation technique. At a low power level, only the main amplifier generates output. At a high power level, the main and auxiliary amplifiers generate output together, and the asymmetric powers are combined by the Doherty circuit. The load modulation network is constructed using passive element's single π-network, instead of λ/4 transmission line, for miniaturizing the amplifier module size. The power amplifier delivers a highly efficient power operation at a low power level while maintaining a comparable efficiency at a high power level.

Ⅱ. Power Amplifier based on Load Modulation Technique of Doherty amplifier concept.

Figure 1 shows an operational diagram of the load modulation technique. I1 is main amplifier's current source and I2 is auxiliary amplifier's current source. If I1 and I2 are turned-on, the parallel combined impedance of the two is matched to Ro and λ/4 impedance transformer does not modulate the load impedance of the main amplifier. However, if I2 is off, Z_1' becomes (N+1)Ro and according to the output level of the auxiliary amplifier, the main amplifier's load impedance is modulated. The load modulation ratio is determined by the size ratio of the auxiliary amplifier to the main amplifier (=N).

In the case of N=1, the amplifier is the classical Doherty amplifier which has high efficiency at 6dB back-off point from maximum power. In the cellular mobile system, power amplifier is usually operated under 17dBm while the peak power is about 28dBm. Therefore, the power amplifier should have high efficiency at about 12dB back-off point from the maximum power [2]. The high efficiency at the lower power below 17dBm can be achieved by generating the power by the main amplifier only with N=3. For the higher power,

the auxiliary amplifier is turned on, and both main and auxiliary amplifiers generate output power. Also, to simplify the circuit topology, the impedance levels of the main amplifier and auxiliary amplifier are designed to be 200ohm and 66.7 ohm by the ratio(N=3) for 50ohm output matching.

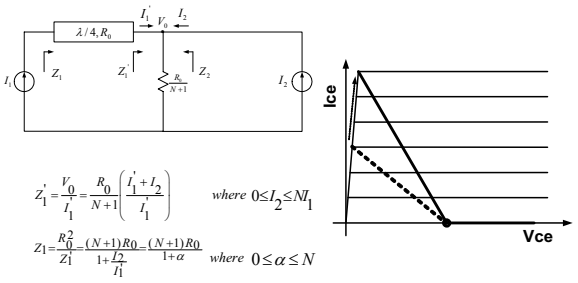


Figure 1 Operational Diagram of the Load Modulation Technique

Figure 2 is diagram of the load modulation amplifier. For the conventional Doherty amplifier, the main amplifier needs λ/4 transmission line for load modulation. But the line is so big that it cannot be employed in miniaturized commercial amplifier modules for mobile handsets. In this work, the line is replaced by lumped element's single π-network [3]. When the auxiliary amplifier is turned off, the output impedance (Z_{aux}') of the auxiliary amplifier circuit should be high, close to open circuit to prevent any power loss through the amplifier path [4]. Therefore, the auxiliary amplifier's matching needs multi-section topologies for power matching at on-state, and high impedance at off-state. The off-state impedance is about 600ohm, which is a near open. Because the amplification chain paths for the main amplifier and auxiliary amplifier have different phase delays, input matching networks of the two amplifiers have to compensate the phase difference.

Ⅲ. Implementation of the Load Modulation Power Amplifier in MMIC Form

Figure 3 is photographs of the MMIC chip and module for test on PCB board. The PA (power Amplifier) MMIC chip is fabricated using a commercial InGaP/GaAs HBT foundry process and the chip size is as small as 0.9 mm X 1.2 mm. A 2um X 40 um X 1 finger unit-cell is used for power device. Since output power at the low power mode is generated by the main amplifier, device size ratio of the main amplifier to the auxiliary amplifier is set to N=3: 16cells for the main amplifier and 48cells for the auxiliary power. Each path consists of 2 stage amplifiers. Mode control switch is integrated in the MMIC chip. The auxiliary amplifier is off at the low power mode and both amplifiers are turned on at the high power mode. The input circuit and output load modulation circuit are realized on PCB board to tune the phase delay and reduce RF output loss.

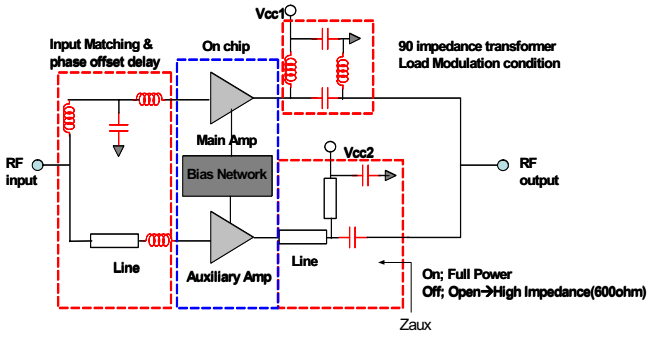


Figure 2 Diagram of the Load Modulation Amplifier (N=3)

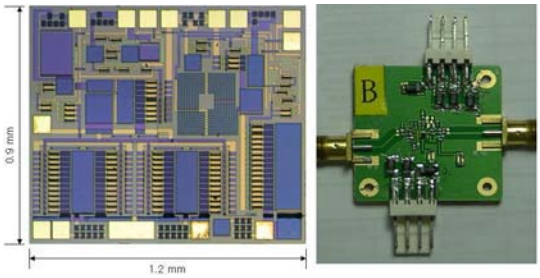
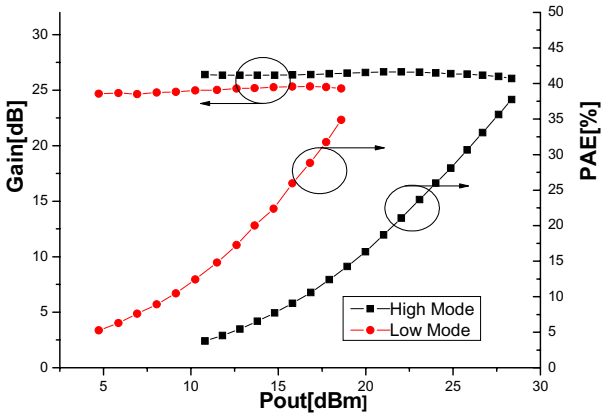


Figure 3 Photographs of MMIC chip and PCB Pattern

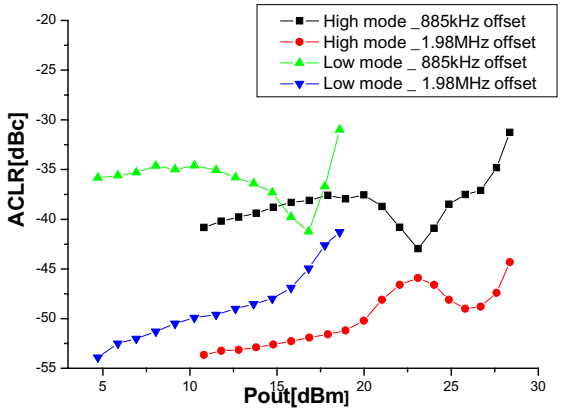
Ⅳ. Measurement Results.

Figure 4 shows RF power and linearity performances of the amplifier for reverse-link IS-95A signal with chip rate of 1.2288Mcps at 824MHz. When the mode selection voltage (Vmode) is 3V, which is the low power mode, the auxiliary amplifier is turned-off, and total quiescent bias current is 12 mA with Vcc=3.4V. PAE of the amplifier is 35 % at Pout of 18.6dBm, and ACLRs (Adjacent Leakage power ratio) are below 31dBc and 41.3dBc at 885KHz and 1.98MHz offsets, respectively. When the Vmode is 0V, which is the high powe mode, the auxiliary amplifier is turned-on and both the main and

auxiliary amplifiers contribute to the output power. The amplifier has efficiencies of 14%, 37.7% at Pout of 18.6dBm and 28.4dBm, respectively, and ACLRs of below 31dBc, 44.3dBc at 885 KHz and 1.98 MHz offsets, respectively. The total quiescent bias current is 81 mA. The control currents for the low and high modes are 0.5mA and 0mA, respectively. Figure 5 shows the CDMA spectra at peak powers of the high and low modes, respectively.



(a)

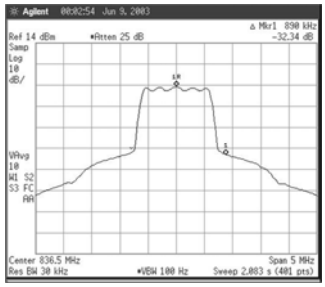


(b)

Figure 4 The RF power and Linearity performances of the power amplifier with load Modulation Technique (N=3)

(a) Gain & PAE @824MHz IS95A_reverse link.

(b) ACLR @824MHz IS95A reverse link. Offsets of 824KHz and 1.98MHz



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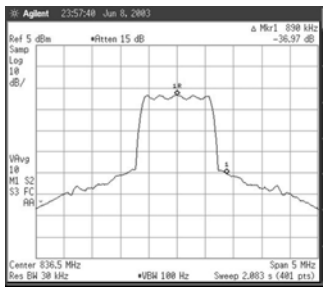


(b)

Figure 5 Measured spectra at peak powers of the high and low modes.
(a) High power Mode @Pout=28 dBm
(b) Low power Mode @Pout=16dBm

Figure 6 shows one-tone continuous signal measurements of P1dB of the amplifier for AMPS mode operation. The amplifier delivers 21dBm with PAE of 41.7%, 30.3dBm with 43% in low mode and high mode, respectively. Figure 7 shows the small signal gains and input VSWR's for the two mode operations. The input return losses are below -20dB in both modes from 800MHz to 880MHz and small signal gains are 26dB and 21.5 dB in high and low modes, respectively.

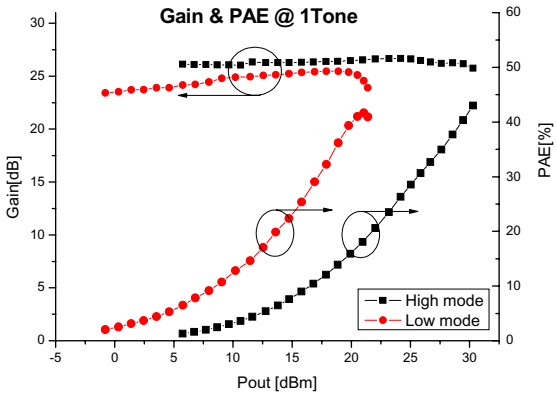
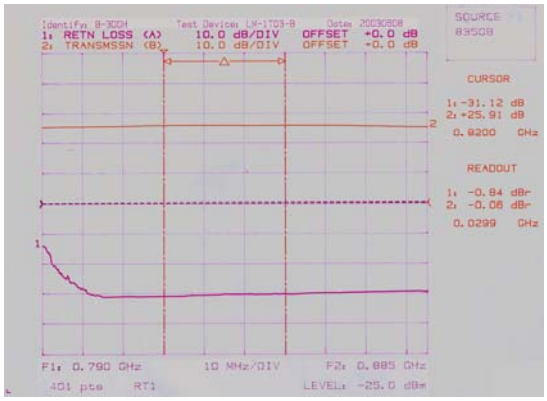
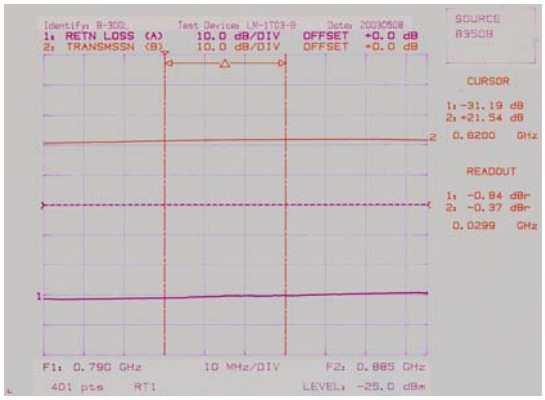


Figure 6 Single tone continuous signal measurement for AMPS mode operation.



(a)



(b)

Figure 7 Small signal Gain and Input Return loss (a) High power mode. (b) Low power mode.

Ⅴ. Conclusion.

It has been shown that a handset power amplifier based on load modulation technique can deliver highly efficient operation at low output power levels, backed-off from maximum output power, without degrading any high power RF performances. The λ/4 transmission line load modulation circuit of the main amplifier's output is replaced by passive π-network and the amplifiers are designed for matching to 50 Ohm directly to achieve a compact PA module. For the CDMA environment, the amplifier at the low power mode exhibits PAE of 35% and ACLR less than 31dBc at 18.6dBm and the high power mode exhibits PAE of 37.7% and ACLR of 31dBc at 28.4dBm. For the AMPS mode operation, the amplifier delivers 21dBm with PAE of 41.7% and 30.3dBm with 43% in low mode and high mode, respectively.

ACKNOWLEDGEMENT

This work is supported by the Agency for Defense Development and Brain Korea 21 projects of the ministry of education in Korea.

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