A Universal Large-Signal Model for Hetero Field Effect Transistors

I. Kallfass*, C. Schick*, H. Schumacher*, T. J. Brazil**
* Department of Electron Devices and Circuits, University of Ulm
Albert-Einstein-Allee 45, 89069 Ulm, Germany
ikall@ebs.e-technik.uni-ulm.de
**Department of Electronic and Electrical Engineering
University College Dublin, Dublin 4, Ireland

***Abstract*— The authors present an analytic, empirical large-signal model for the efficient simulation of Hetero Field Effect Transistors. The model has been extracted and verified for a 0.15μm AlGaAs/InGaAs/GaAs pHEMT as well as for a 0.2μm InP/InGaAs/InP pHEMT technology. It uses a new set of charge-conservative capacitance expressions as well as a dispersion model for accurate description of both static and dynamic IV characteristics. A large voltage regime is covered, ranging from the sub-threshold to forward gate conduction and linear to saturation operating regions. Typical HFET effects like self-heating, gain compression, impact ionization as well as particularities of capacitance characteristics are included. Model verification is carried out for static IV, high-frequency S-parameters as well as one- and two-tone power measurements at microwave frequencies for both types of transistors.**

I. INTRODUCTION

The HEMT transistor, due to its unequalled combination of high-frequency-, low-noise- and power capabilities, is still the device of choice in many demanding micro- and millimeterwave applications, and in very high bitrate fiberoptic front-ends. To use the devices in circuit design, efficient large-signal simulation models are required which accurately describe nonlinearities at high power levels and under various operating conditions. For that purpose, equivalent circuit-based models which employ analytic and global equations are still best suited, providing the best trade-off between large-signal accuracy, computing efficiency, global validity and physical interpretability. These properties are still not reached by other modelling approaches such as Volterra series, table-based or purely physical models. However, in state-of-the-art pseudomorphic and metamorphic HEMT devices using InP- or GaAs-based heterostructures, several physical effects, introducing strong nonlinerities and deviations from ideal device characteristics, start to play a non-negligible role and need to be included in the circuit models. Among these are frequency dispersion effects such as self-heating, hot carrier generation, trapping effects etc., which mainly affect the drain current-voltage (IV) characteristics. Also, compared to MOSFETs, HEMT devices tend to exhibit more pronounced nonlinearities with respect to transconductance characteristics (e. g. gain compression due to parasitic channels) as well as gate capacitance.

The presented model incorporates empirical expressions for all of the above effects and can therefore be applied to a wide variety of different HEMT devices. Here, we present its application to the 0.15μm pseudomorphic AlGaAs/InGaAs/GaAs pHEMT foundry process offered by United Monolithic Semiconductors (UMS) [1] with a transit frequency of $f_T = 110$ GHz as well as a 0.2μm InP/InGaAs/InP pHEMT process with an f_T of up to 120 GHz, developed by Innovative Processing AG (IPAG) [2]. It should be noted that, in each case, the same model topology and nonlinear equations have been employed, proving the model's universal validity for HEMT devices, all the more since it was originally developed and applied to a strained-Si/SiGe HEMT process [3].

II. MODEL TOPOLOGY AND EXTRACTION METHODOLOGY

The equivalent circuit (excluding the de-embedding network) is shown in Figure 1. Its nonlinear elements are the gate diodes, the static drain current source I_{ds}, gate capacitors $C_{gs}$and C_{gd} as well as the dispersion source I_{dsx}.

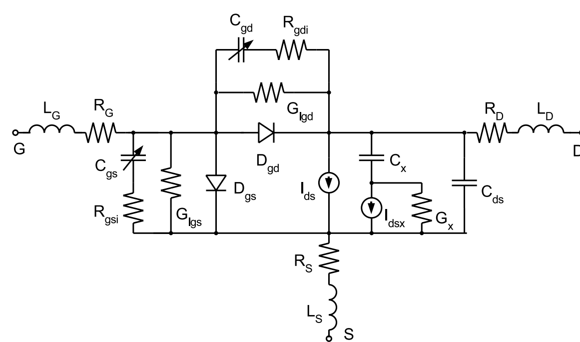


Fig. 1. HFET equivalent circuit with nonlinear capacitance and dispersion elements.

Parameter extraction is performed as follows: After de-embedding the internal transistor structure from the influence of contact pad parasitics, the series resistors R_g, R_d and R_s as well as series inductors are extracted via the cold-FET method according to [4]. The static model is then built from

DC gate- and drain current measurements. For the dynamic model, the small-signal elements of the intrinsic transistor are obtained analytically from measured S-parameters [5]. Applying these equations under bias conditions over the whole IV-plane yields their respective voltage-dependence which, in turn, is described by large-signal equations.

III. Nonlinear Model Elements

A. Static Model

Together with the series resistors R_g, R_d and R_s, the static model is formed by the nonlinear gate-source- and gate-drain diodes and the main nonlinear element, the drain current source. The Schottky diode model includes non-ideal forward conduction, leakage current and reverse breakdown (which, under normal operating conditions, will only occur in the gate-drain path). Drain current characteristics are described using a modified COBRA model [6]:

$$I_{ds} = \beta \cdot V_{eff}^{\overline{\frac{\lambda}{1+\mu V_{ds}^2+\xi V_{eff}^{\eta}}}} \cdot tanh\left(\alpha V_{ds}\left(1+\zeta V_{eff}\right)\right) \qquad (1)$$

$$V_{eff} = \frac{1}{2}\left(V_{gs} - V_{t1} + \sqrt{\left(V_{gs}-V_{t1}\right)^2+\delta^2}\right) \qquad (2)$$

$$V_{t1} = \left(1+\beta^2\right)V_{to} - \gamma V_{ds} \qquad (3)$$

This compact and efficient model allows for the inclusion of typical HFET effects like deviation from square-law (λ) in the 2-dimensional electron gas channel (2DEG), transconductance compression (ξ, η) due to parasitic channels and the onset of impact ionization current (μ). The unitless parameter η has been added for the description of gain compression together with ξ. They are extracted from transfer characteristics in saturation and beyond $V_{gs}|_{g_{m,max}}$. An additional modification has been introduced to account for self-heating in the GaAs pHEMT under static and very low frequency conditions, using the approach taken in [7], which derives drain current as a function of temperature based on the fact that the carrier saturation velocity varies approximately with T^{-1}:

$$I_{ds} = \frac{I_{ds'}}{1+\pi_{eff}^{-1} I_{ds'} V_{ds}} \qquad (4)$$

In this equation, $I_{ds'}$ denotes the current of equation 1. Since temperature is not a model parameter in our approach, parameter π_{eff}^{-1} has to be extracted from measurements. The value of π_{eff}^{-1} may be found by extracting the COBRA expression for devices with very small total gate width, where current reduction due to self-heating may be neglected and π_{eff}^{-1} has no significant impact. Applying this parameter set to larger devices using e.g. linear scaling, one can then fit π_{eff}^{-1} to describe the current reduction in larger devices. That way, the model becomes scalable with respect to gate width. For modelling the dynamic IV characteristics of the GaAs pHEMT, π_{eff}^{-1} is set to zero. Also, in the InP HEMT, self-heating plays a minor role and needs not be included in the model. The resulting match between measured and modelled drain current characteristics of a 2x50μm gate width GaAs HEMT and 2x40μm InP HEMT are shown in Figure 2.

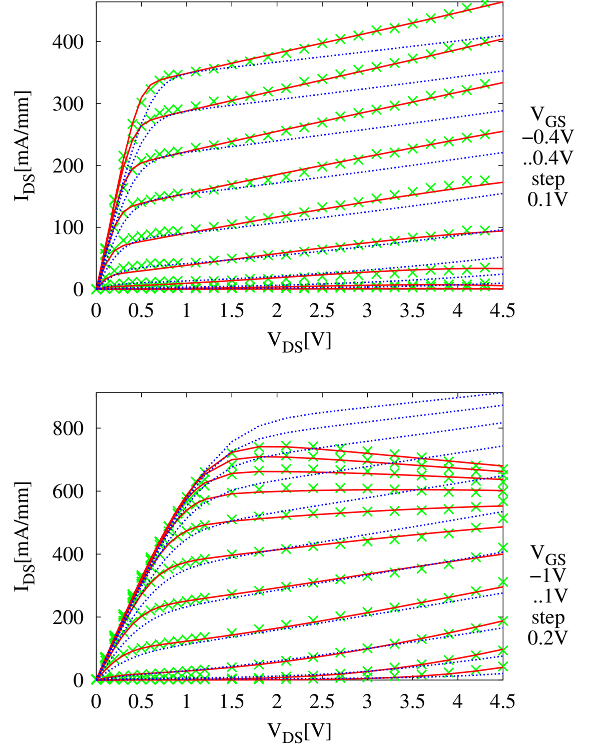


Fig. 2. Static drain current characteristics of a 2x40μm InGaAs/InP pHEMT (top) and a 2x50μm AlGaAs/GaAs pHEMT (bottom) using the modified COBRA expression. Symbols are measured-, solid lines are modelled DC values. Dotted lines are dynamic IV curves obtained from numerical integration of dynamic trans- and output conductance.

For both transistor types, the covered voltage regime extends from sub-threshold to onset of gate conduction in terms of V_{GS} and from the linear- well into the saturated region in terms of V_{DS}. In the GaAs HEMT, with the low thermal conduction coefficient of the GaAs substrate, the self-heating effect is very pronounced. The InP-based device, however, due to the low bandgap energy of InP, exhibits an early onset of hot carrier generation current. Both of these effects in the static drain current characteristics can be covered by the model, but are among the effects which disappear in the dynamic IV characteristics, discussed in the next chapter.

B. Dynamic Nonlinearities

Nonlinear elements in the dynamic model are the dispersion source I_{dsx} as well as gate-source- and gate-drain capacitance. All other elements are modelled as being linear, which is an allowable simplification for the benefit of reduced model complexity. To make the model even more accurate at microwave

frequencies, nonlinearities of the non-quasi static resistors R_{gsi} and R_{gdi} as well as nonlinear time delay τ could be included, too. The respective voltage-dependencies of these elements are known from the multi-bias small-signal model extraction.

Dynamic IV characteristics may be obtained via pulsed-IV measurements, avoiding the influence of frequency dispersion effects with associated time constants exceeding the minimal pulse width. In our approach, similar to building table-based spline models (e.g. [8]), the extracted high-frequency transconductance $g_{m,ac}$ and output conductance $g_{ds,ac}$ information from multi-bias S-parameters are used to integrate for a dynamic nonlinear current source

$$I_{ds,ac} = I_{ds0} + \int_C g_{m,ac}\partial V_{gs} + g_{ds,ac}\partial V_{ds} \qquad (5)$$

Due to the path dependence of the numerical integration of $g_{m,ac}$ and $g_{ds,ac}$, a quantifiable error will be introduced to the resulting dynamic IV behaviour. The integration path C and quiescent point I_{ds0} for integration are chosen so as to minimize the introduced error. In Figure 2, the dynamic IV characteristics obtained from numerical integration of dynamic small-signal characteristics are included. The nonlinear current source I_{dsx} in the equivalent circuit is attributed the value of $I_{dsx} = I_{ds,ac} - I_{ds,dc}$, resulting in the intended circuit behaviour both under static and dynamic conditions.

The voltage dependence of the gate-source- and gate-drain capacitance is described by charge-conservative equations:

$$\begin{aligned} C_{gs}(V_{gs}, V_{ds}) \;=\;& C_{pgs} + \frac{C_{gs1}}{(1-\frac{V_{gs}}{V_{bi}})^m} \\ &+ C_{gs2}(1 + tanh(\kappa(V_{gs} - V_{t2}))) \\ &+ C_{gs3}V_{ds}\frac{1}{cosh^2(\nu(V_{gs} - V_{t3}))} \\ &+ C_{gs4}V_{ds} \end{aligned} \qquad (6)$$

$$\begin{aligned} C_{gd}(V_{gd}, V_{ds}) \;=\;& C_{pgd} + \frac{C_{gd1}}{(1-\frac{V_{gd}}{V_{bi}})^m} \\ &+ C_{gd2}(1 + tanh(\theta(V_{gd} - V_{t5}))) \\ &- \frac{C_{gs3}}{\nu}tanh(\nu(V_{gd} + V_{ds} - V_{t3})) \\ &- C_{gs4}(V_{gd} + V_{ds}) \end{aligned} \qquad (7)$$

The novelty lies in the V_{ds}-dependent terms, which allow for typical HFET capacitance behaviour. In saturation, before the onset of gate conduction, one observes a decreasing C_{gs} with increasing V_{gs}, analoguous to the reduction of transconductance. This indicates the formation of a parasitic MESFET channel below- or an ungated electron accumulation in the supply layer above the 2DEG. In fact, the parameters concerned, C_{gs2}, ν and V_{t3} can be partially linked to g_m characteristics. For example, V_{t2} is found to coincide with the gate-source voltage for maximum transconductance: $V_{t2} \approx V_{gs}|_{g_{m,max}}$. The condition of charge-conservation (e.g. [9]) then basically dictates the C_{gd}-terms, which are found to very well fit the extracted C_{gd} data. In the GaAs HEMT, C_{gs} and C_{gd} are not equal for zero drain bias, indicating an intentional e-beam gate placement closer to the source contact. Extracted and modelled capacitance data is shown in Figure 3.

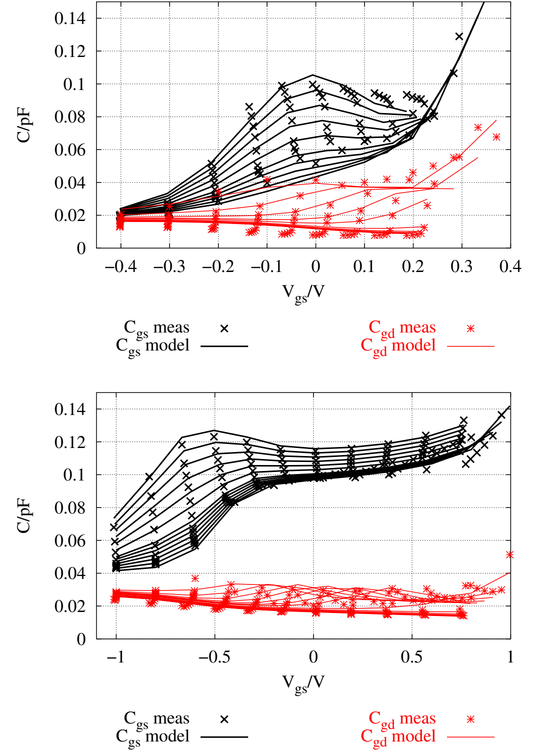


Fig. 3. Nonlinear capacitance of the 2x40μm InP HEMT (top) and the 2x50μm GaAs HEMT (bottom) as a function of V_{gs} with parameter V_{ds} ranging from linear to saturation conditions (compare respective DC regimes).

IV. Model Verification

The model is implemented in the Advanced Design System (ADS) simulation platform as a user-compiled model. Linear scaling is applied to allow for different gate widths. First, the model is used in an S-parameter simulation up to 50 GHz in a bias point in saturation ($g_{m,max}$) and compared to measurements (Figure 4).

For large-signal verification, the model is used to simulate gain compression and the creation of harmonic frequencies in a one-tone measurement with increasing input power levels and compared to measurements. Figure 5 shows the result for a 8 GHz input frequency and the InP HEMT biased at $g_{m,max}$ ($V_{GS} = 0.1V$). For both devices, 1dB compression points (CP_{1dB}) and one-tone second order intercept points (IP_2) are derived and listed in the table below. Two-tone measurements are carried out with a tone spacing of 100 kHz and third-order intermodulation points can be compared. In Figure 6, the

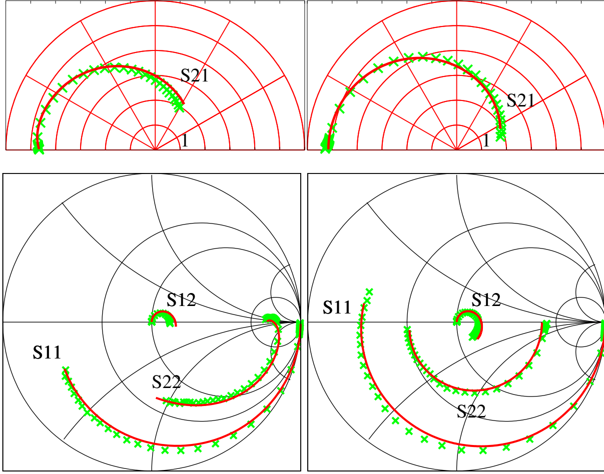
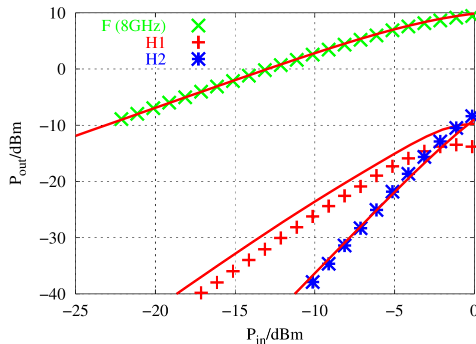


Fig. 4. S-parameter verification in a frequency range from 50 MHz to 50 GHz. 2x40μm InP pHEMT: S_{21} (top left) $S_{11}/S_{12}/S_{22}$ (bottom left), 2x50μm GaAs pHEMT: S_{21}(top right) $S_{11}/S_{12}/S_{22}$ (bottom right).

comparsion of measurement and simulation is shown for the GaAs HEMT device biased at $g_{m,max}$ ($V_{GS} = -0.2V$) with input tones at 16 GHz and 16.0001 GHz. All power levels are referenced to the device in- and output plane. Simulation accuracy for all figures is found to be within 1.0 dB. Similar results are found for different fundamental frequencies and bias conditions.

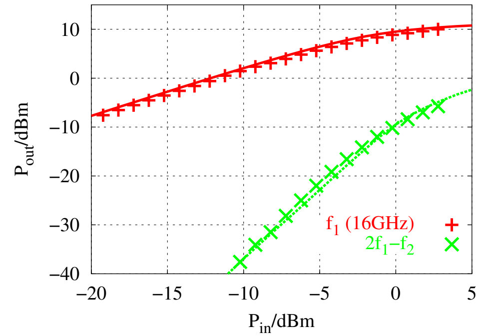


Device	Fund	ICP_{1dB}/dBm		IIP_2/dBm	
		meas	model	meas	model
InP	8 GHz	-6.0	-5.0	10.5	9.8
GaAs	8 GHz	-1.1	-1.0	13.9	13.0

Fig. 5. Measured and simulated gain compression and creation of harmonics at 8 GHz fundamental frequency in a 2x40μm InP HEMT (top). Input related 1dB compression- and 1-tone second order intercept points (bottom).

V. Conclusion

The presented model is found to be well suited for simulating the characteristics of various HFET technologies, both for static characteristics and under dynamic small- and large-signal conditions at microwave frequencies. The nonlinear equations employ a relatively small number of extraction parameters which makes the model easily adaptable to technological process variations. Being computationally efficient and robust with respect to convergence, it is ideally suited for use in analog circuit design, enabling reliable design and realization of integrated circuits using today's leading HFET processes.



Device	Fund	IIP_3/dBm	
		meas	model
InP	16 GHz	6.1	6.1
GaAs	16 GHz	9.3	9.5

Fig. 6. 2-tone measurement of a 2x50μm GaAs HEMT at 16 GHz (top). Third-order intercept points (bottom). Tone spacing is 100 kHz.

VI. Acknowledgment

We express our gratitude to Innovative Processing AG and United Monolithic Semiconductors for providing the transistor samples of their HEMT processes for characterisation- and model extraction purposes.

References

[1] www.ums-gaas.com
[2] D. Keiper, P. Velling, A. Brennemann, M. Agethen, C. van den Berg, R. M. Bertenburg, "MOVPE growth of InAlAs using TBAs and DitBuSi for HEMT applications," *Journal of Crystal Growth*, vol. 248, pp. 153–157, February 2003.
[3] I. Kallfass, T. J. Brazil, B. OhAnnaidh, P. Abele, T. Hackbarth, M. Zeuner, U. König, H. Schumacher, "Large Signal Modelling including Low-Frequency Dispersion of N-channel SiGe MODFETs and MMIC Applications," *Solid-State Electronics*, vol. 48, August 2004.
[4] G. Dambrine, A. Cappy, F. Heliodore, E. Playez, "A New Method for Determining the FET Small-Signal Equivalent Circuit," *Trans. Microwave Theory and Techniques*, vol. 36, pp. 1151–1159, July 1988.
[5] M. Berroth, R. Bosch, "High-Frequency Equivalent Circuit of GaAs FET's for Large-Signal Applications," *Trans. Microwave Theory and Techniques*, vol. 39, pp. 224–229, February 1991.
[6] V. I. Cojocaru, T. J. Brazil, "A Scalable General-Purpose Model for Microwave FET's Including DC/AC Dispersion Effects," *IEEE Trans. Microwave Theory and Techniques*, vol. 45, pp. 2248–2255, December 1997.
[7] P. C. Canfield, S. C. F. Lam, D. J. Allstot, "Modelling of Frequency and Temperature Effects in GaAs MESFETs," *J. Solid-State Circuits*, vol. 25, pp. 299–306, February 1990.
[8] K. Koh, H. M. Park, S. Hong, "A Spline Large-Signal FET Model Based on Bias-Dependent Pulsed I-V Measurement," *Trans. Microwave Theory and Techniques*, vol. 50, pp. 2598–2603, November 2002.
[9] A. Siligaris, M. Vanmackelberg, G. Dambrine, N. Vellas, F. Danneville, "A new empirical non-linear model for SOI MOSFETs," *Proc. 10th GaAs Symposium*, pp. 101–104, October 2002.