Fabrication of Very High Performance 50nm T-gate metamorphic GaAs HEMTs with exceptional uniformity.

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Abstract— **We report on the fabrication of 50nm metamorphic GaAsHEMTs with a very high yield and uniformity as determined by DC characterisation, and excellent RF figures of merit. The T-gates were realised using a combination of high resolution electron beam lithography using a bi-layer (rather than the usual tri-layer) of PMMA/Co-polymer and a selective wet etch to form the gate recess. With an electrical yield greater than 95 %, the devices displayed a threshold voltage of -0.445V with a standard deviation of ± 0.005V. The transconductance of the devices was 1169mS/mm 83 mS/mm and demonstrated a cut-off frequency, f_T of 330GHz.**

I. Introduction

Due to their excellent performance, High Electron Mobility Transistors (HEMTs) based on InP are of great interest for the fabrication of high-speed electronics for applications such as 160Gbit/s data communications [1] and environmental monitoring using the G band [2].

However InP substrates fragile, which can limit the yield and are not available in as large diameter as GaAs substrates, which reduces the economies of scale. Metamorphic devices fabricated on GaAs are capable of providing comparable performance to InP-based HEMTs but with the benefits of a GaAs substrate. This makes metamorphic GaAs HEMT technology ideally suited for the fabrication of millimetre-wave monolithic integrated circuits (M^3ICs). These circuits require a technology that can produce active devices capable of operating at frequencies in excess of 100GHz with highly uniform characteristics across the wafer.

In this work, uniformity improvements were achieved by modifying the gate resist stack. For relatively modest 120 nm gate length T-gates, it has been noted previously that the thickness of the gate resist plays a key role in the quality of the gate lithography.[3] The converntional resist stack for a PMMA/co-polymer T-gate consist of a tri-layer of PMMA/P(MMA/MAA)/PMMA. [4] The thickness of each of the three layer of the conventional resist stack were measured when spun within a source-drain gap using AFM The thickness of the upper layer of resist was twice as thick as the same resist spun on a planar substrate. This contributed to a total thickness of 550nm, which is 90nm thicker than on planar substrate. This layer was originally included to aidaid T-gate lift-off by providing a well defined undercut profile. In this work, the top layer of resist is ommited to provide a more uniform resist stack across the width of the device with no detremintal effects on the lift-off process. The reduction in resist thickness allows a highly uniform T-gate with a foot-print of 50nm to be realised.

The gate recess etch was performed using a highly selective succinic acid based etch which stops on an $In_0.52Al_0.48As$ etch stop layer therefore providing accurate control of the depth of the recess etch.

II. Fabrication

Devices were fabricated on a metamorphic GaAs wafer. The design of the layer structure consisted of a highly n-doped 20nm $In_{0.53}$ $Ga_{0.47}As$ cap, a $In_{0.52}Al_{0.48}As$ barrier layer with a thickness of 8nm and a spacer layer with a thickness of 4nm. The channel comprised of a 20nm thick $In_{0.53}$ $Ga_{0.47}As$ layer. This gives a gate to channel separation of 12nm making the material suitable for the fabrication of scaled 50nm gate length devices. All lithography steps were performed using electron beam lithography. Mesa isolation was performed using a non-selective wet etch. The ohmic contacts were metallised by electron beam evaporation using a Ni:Ge:Au metallisation scheme. The ohmic contacts were annealled at 280°C resulting producing a contact resistance of 0.07Ω.mm.

As disscussed in the introduction the T-shaped gates were formed using a bi-layer of high molecular weight PMMA and a co-polymer of PMMA and PMAA. The layers of resist were spun between source and drain contacts the thickness of each layer was measured by AFM and were found to be 70nm

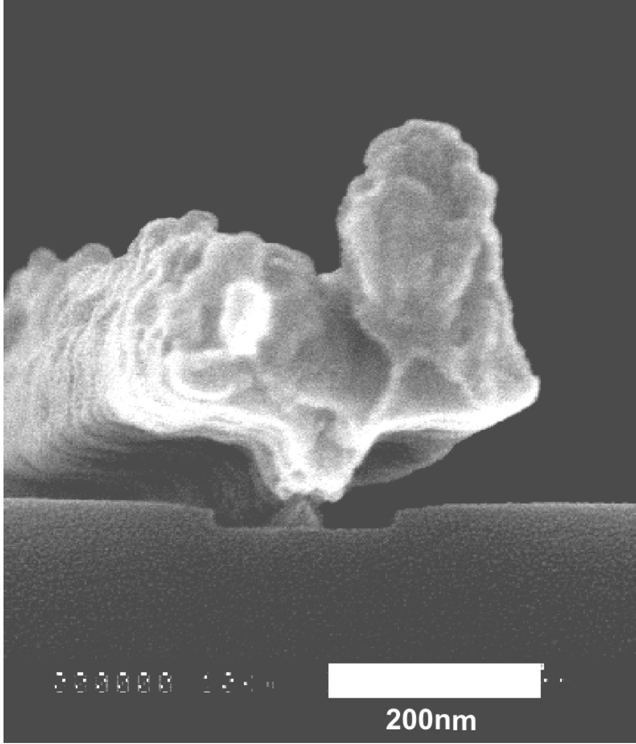

Fig. 1. SEM Cross–section of fabricated 50nm T-gate

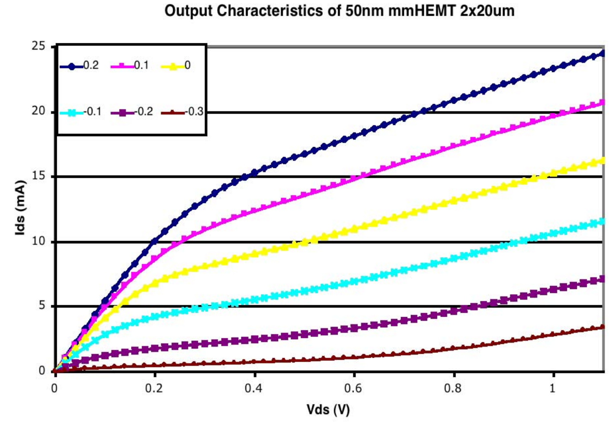

Fig. 2. Output Characteristics of 2x20μm 50nm metamorphic HEMT

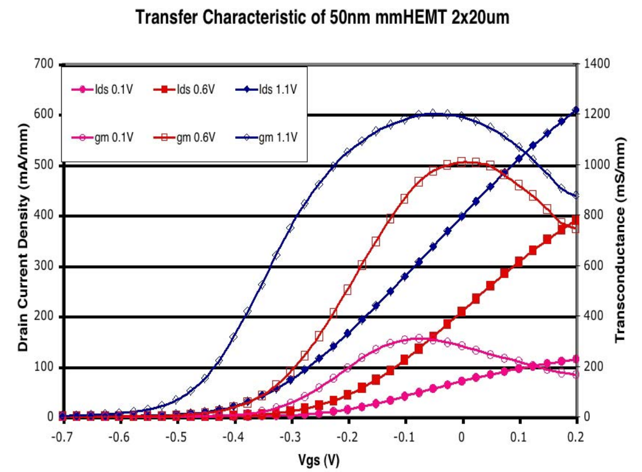

Fig. 3. Transfer Characteristics of 2x20μm 50nm metamorphic HEMT

and 250nm for the PMMA and co-polymer layer respectively . This gives a total resist thickness of 320nm allowing metal with a thickness of up to 200nm to be evaporated and lifted off without problems. The gate lithography was performed using a Leica EBPG-5HR electron beam tool using a spot size of 12nm. This tool operated with an acceleration voltage of 100kV in order to minimise scattering through the resist which has the effect of increasing the effective spot size of the beam.

The gate recess was formed using a succinic acid based selective wet etch. The length of the recess offset was controlled by the etch time. The recess offset of these devices was 10nm, this was length was determined by experiment to give the best transfer characteristics for this layer structure. The gates were formed by evaporating and lifting off Ti:Pt:Au film with a total thickness of 200nm. Fig. 1 shows a cross-section of the gate region of a typical device. It can be seen that the foot-width of the device is 50nm with a clear separation between the gate-head and the doped cap. The devices were completed with the addition of 400nm thick Co-Planar Waveguide (CPW) bond pads to allow on wafer characterisation .

III. Results

The devices were characterised on-wafer using Cascade Microtech V-band probes and an HP4155C parameter analyser. The electrical yield was greater than 95%.

Fig. 2 shows the output charcteristic of a 2x20μm device measured with V_{ds} varying from 0 to 1.1V and stepping the gate voltage, V_{gs} from 0.2 to -0.3V in -0.1V steps. The transfer characteristic measured with V_{gs} varied from -0.7V to 0.2V is given in Fig. 3. The output characteristic illustrates the low access resistance and the excellent pinch off characteristic of the device. The transfer characteristic shows the maximum transconductance of 1200mS/mm at drain bias of 1.1V. The peak transconductance of this particular device is 1200mS/mm which is achieved at a gate voltage of -0.05V.

The threshold voltage across the wafer were measured by taking the threshold voltage, V_{th} to be 2% of I_{dss}. The histogram of these values is shown in Fig. 4, the large majority of devices tested had a threshold voltage in the range of -0.425V to -0.475V. The average threshold voltage of the devices is -0.445V with a standard deviation of 0.005V this is, to the author's knowledge, the most uniform threshold voltage demonstrated for HEMT of this gate length. The average

transconductance was found to be 1169± 83mS/mm across the wafer.

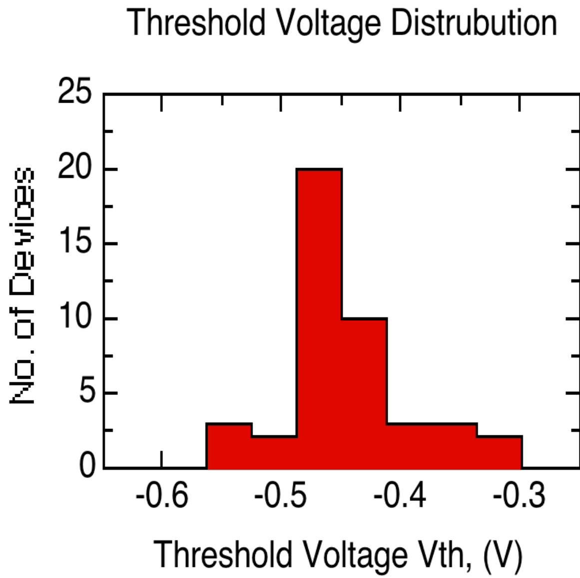

Fig. 4. Histogram of the Threshold Voltage of forty device measures across the wafer

The devices were then characterised between 0.04 and 60GHz using an Anritsu 360B VNA. A small signal model was produced using the "cold-FET" technique to accurately determine the parasitic elements of the device. [5]. This model is used to remove the effects of the CPW waveguides, the de-embedded short circuit current gain, H_{21}, and the unilateral power gain, U, are shown in Fig. 5. Extrapolating these to unity gain gives a cut-off frequency, f_T, of 330GHz and a maximum frequency of oscillation [6], f_{max}, of 260GHz. The unilateral power gain, U, was extrapolated rather than the commonly used MAG to avoid simulating the devices to very high frequencies to find the conditional stable region (k>1) which can introduce errors into extrapolated value of f_{max}These results show that excellent yield and uniformity can be achieved with this technology without compromising key RF figures of merit.

IV. Conclusion

This work demonstrates the fabrication and the characterisation of highly uniform metamorphic HEMTs with a T- shaped gates with a length of 50nm. These devices exhibited very high yield and the lowest threshold voltage spread reported for 50nm HEMT devices. This high uniformity was achieved by a combination of uniform gate lithography and the use of a highly selective gate recess etch. The uniform gate lithography was achieved by the careful control of the resist thickness along the width of the device, this was primarily achieved by the removal of the upper layer of the standard tri-layer

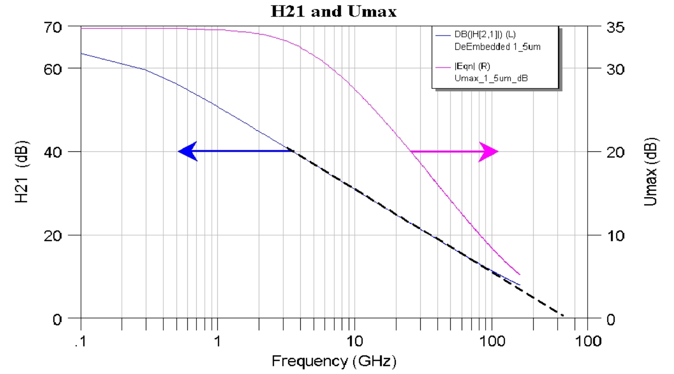

Fig. 5. De-embedded H21 and Umax of a 2x20μm 50nm metamorphic HEMT showing an fT and fmax of 330GHx and 260GHz respectively.

resist stack. The threshold voltage across the wafer was -0.475±0.005V. In addition the devices displayed an f_T of 330GHz. This combination of high speed perfromance and uniformity make this technology an ideal candidate for the use in M^3ICs operating above 100GHz.

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