C Band DROs Using Microwave Bipolar Devices

C.Florian*♠, M.Pirazzini°♠, G.Vannini°, A.Santarelli*, M.Borgarino♣, C. Angelone♦, M.Paparo♦, F.Filicori*

*DEIS, University of Bologna, Bologna, 40136 Viale Risorgimento 2, Italy, cflorian@deis.unibo.it

°Department of Engineering, University of Ferrara, Ferarra, 44100 Via Saragat 1, Italy, gvannini@ing.unife.it

♣Engineering Faculty, University of Modena and Reggio Emilia , Modena, 41100 Via Vignolese 905 , Italy

♦STMicroelectronics Catania Site, Catania, 95121 Stradale Primosole 50, Italy

♠MEC srl MicroWave Electronics for Communications, 40123 Viale C.Pepoli 3/2, Italy mec.design@mec-mmic.com

Abstract — **A silicon self-aligned-emitter bipolar process from STMicroelectronics for very high efficiency handsets power applications has been used to build two Dielectric Resonator Oscillators. Despite this technology addresses the mobile telephony frequency range at 1.8GHz, the oscillators generate a stable reference at 6GHz and 7.5GHz with good phase noise performance. A low frequency noise model has been identified and implemented in a Gummel Poon BJT nonlinear model. A design technique to optimize stability and phase noise performances has been used. The DROs exhibit phase noise of -116dBc/Hz and -107dBc/Hz at 10KHz offset from the carrier at 6GHz and 7.5GHz, respectively.**

I. Introduction

The need for stable frequency references in space, wireless communication and military systems drives nowadays toward extremely high quality performances in the oscillator design. Obviously, not only the stability performances are addressed, but also the final circuit dimensions and its reliability are an issue of first concern. Unfortunately, as far as the ultimate low phase noise performances is the goal of the project, the best choice at this stage is to use an external resonator with an high Q factor. In fact, although many new monolithic technologies are focused to realize passive elements with higher quality factors, the intrinsic lossy characteristics of the semi-insulating monolithic substrates limit the achievable Q factors for capacitors and inductors to a few tens. On the other side, when using an external resonator (like cavity, coaxial, mechanical or dielectric resonators) unloaded Q factors of some thousands at X band are easily achievable. Obviously, the drawback of this choice is the increasing dimensions of the system (no more monolithic) and the increased complexity of the system assembly.

Besides the choice of an high quality-factor resonator, the low-frequency (LF) noise of the active device adopted for the oscillator design has direct consequences on the phase noise performances of the circuit [1]. However, the choice of an high quality-factor resonator and a low LF noise technology, is a necessary, but not always sufficient condition for low phase noise performances. In fact, the conversion factor (pushing factor [1]) from LF noise to phase noise around the carrier can be largely modified by smart choices in the oscillator design [2][3]: the large-signal design technique applied to optimize the performances of the presented circuits is described in [2] and [3]. The goal of this project was to build up a very low phase noise oscillator using a bipolar technology made available by STMicroelectronics [4], achieving the highest reachable frequency.

II. Technology

We used a self-aligned-emitter bipolar process by STMicroelectronics (HSB3) for the design of the oscillators' negative resistance part [4]. HSB3 is an high-performance low-cost silicon bipolar technology born for high-efficiency low-voltage RF power amplifiers at 900 MHz and 1.8-1.9GHz mobile telephony bands. With this work we tried to extend the technology applications to high frequency oscillators. The technology provides oxide trench isolation, three metal layers, optional gold metal layer, poly resistors and MIM capacitors ($0.7fF/\mu m^2$). On-chip spiral inductors with Q values up to 9 at 1.9GHz are also available. The static current gain β is about 150, the transition frequency f_T is around 40GHz and the VCE breakdown is 3.3V. From these data it is clear how the upper frequency limit for the oscillator design is not set by the active device transition frequency, but by the typical loss of silicon substrates that makes the passive element Q factor and self-resonance frequency become critical as the operating frequency increases. Another challenging point using this technology at high frequency (3-4 times the normally addressed frequency of 1.9GHz) is the absence of via holes: the ground plate is located in the upper surface and needs to be externally grounded through bonding wires to an external reference. Therefore, the associated series inductances in the ground path can give non-trivial problems in terms of stability, especially in the emitter grounding path.

III. Nonlinear And LF Noise Model Identification

The active device chosen for the oscillator implementation is a 4 emitter fingers of 0.2μm by 48μm: this means a total emitter area of 38.4 μm^2. The device was measured and characterized at the Bologna University Telecommunication Labs, and a non linear Gummel-Poon model was identified using the Agilent-ICCAP CAD software.

The model was then implemented in the Agilent ADS2002 environment, the CAD software used for the

oscillators design. Static and dynamic simulation tests (under small and large signals) with the identified model provided good agreement with on wafer measurements on test devices (see figure 1).

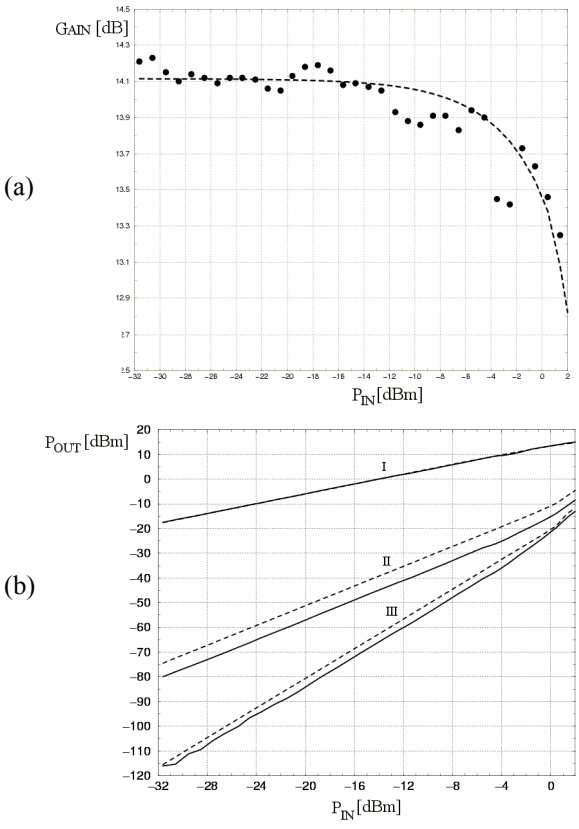

Fig. 1. (a) Prediction of the Gain Compression @2GHz, V_{be}=0.8V, V_{ce}=2V. (b) Prediction of Harmonic Distortion @2GHz, V_{be}=0.8V, V_{ce}=2V.

On wafer LF noise measurements on some test devices were carried out at the University of Modena to identify an LF noise model which is described in [5] and [6]. The short circuit current configuration of the model noise sources [6] has been chosen (figure 2): the model sources and their correlation are identified by measuring the spectral densities S_{IB} and S_{IC} and S_{IBIC*} (figure 2), that are referred to the base and collector short circuit noise currents and their cross-spectrum respectively. As described in equations 1, 2, 3, four different contributions were identified: shot, flicker and two different g-r noise sources were used to fully reproduce the device LF noise behaviour.

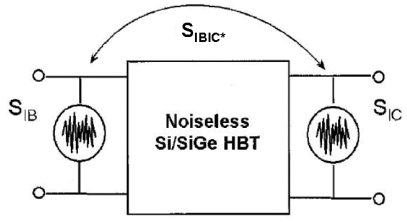

Fig. 2. Implemented Noise Model

$$S_{iB} = 2qI_B + \frac{K_{1/fB}}{f} + \frac{K_{g-r1B}}{1+\left(\frac{f}{f_{c1B}}\right)^2} + \frac{K_{g-r2B}}{1+\left(\frac{f}{f_{c2B}}\right)^2} \quad (1)$$

$$S_{iC} = 2qI_C + \frac{K_{1/fC}}{f} + \frac{K_{g-r1C}}{1+\left(\frac{f}{f_{c1C}}\right)^2} + \frac{K_{g-r2C}}{1+\left(\frac{f}{f_{c2C}}\right)^2} \quad (2)$$

$$S_{iBiC*} = white + \frac{K_{1/fBC*}}{f} + \frac{K_{g-r1BC*}}{1+\left(\frac{f}{f_{c1BC*}}\right)^2} + \frac{K_{g-r2BC*}}{1+\left(\frac{f}{f_{c2BC*}}\right)^2} \quad (3)$$

Fig. 3. Expressions of the Noise Spectral Densities

The noise model was implemented by embedding ADS2002 noise sources in the previous mentioned nonlinear Gummel-Poon model.

IV. Oscillators Design And System Implementation

The oscillators design was carried out with the Agilent ADS2002 nonlinear simulator. The circuit topology is a classical series feedback configuration similar to those described in [1] and [5]. We designed two different oscillators at 6 GHz and 7.5GHz. At the moment we haven't been able to go up to the X band, because the losses in the substrate make it difficult to achieve the required loop gain at high frequency. As shown in figure 3, the negative resistance part of the circuit is implemented by means of a monolithic die in HSB3 technology.

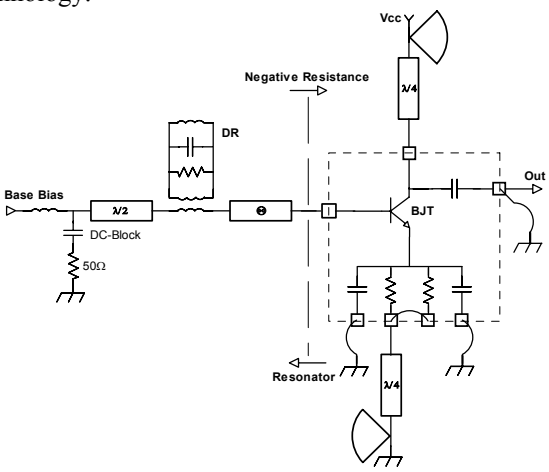

Fig. 3. DRO schematic representation. The part inside the dashed line is the silicon monolithic circuit.

An integrated MIM capacitor in series with the transistor emitter is adopted to obtain the negative resistance, while an integrated resistor is placed in series with the emitter DC path to stabilize the bias point. The collector LC matching network is composed of a series integrated MIM capacitor and a bonding wire shunted from the die output pad to the external ground reference.

We didn't use any integrated inductor for the matching networks because of their self-resonance frequency close

to the operating circuit frequency. For the same reason, and due to their low Q factor at these frequencies, we didn't use integrated inductors for the bias decoupling networks, that are all external on the alumina substrate.

The resonator stabilizing part of the circuit is built by means of a Murata DR (12000 unloaded Q factor) electromagnetically coupled with a 50 Ohm microstrip line on the alumina substrate which is wire bonded directly to the transistor base pad. The line is 50 Ohm terminated for RF signals, by means of a bias tee at its other end, while it is used to drive the base bias current too. The length of the microstrip line between the DR and the transistor base, in addition with the length of the wire bonding, are design parameters: controlling those lengths we can vary the loop-gain phase.

The DR-microstrip line coupling was modeled by means of an RLC equivalent circuit [7] identified by a set of scattering parameter measurements on a suitable jig set-up with a throu line and the DR placed near it. To obtain an exhaustive set of different coupling factors between the DR and the line, many measurements were performed with the DR puck placed at different distances from the line and with different quartz spacers under the DR puck.

As stated before, the presence of an high Q resonator and the choice of a low flicker noise technology can't always guarantee ultimate phase noise performances. In fact, if the circuit is not suitably designed, the actual oscillation frequency, which doesn't necessary coincide with the highly stable intrinsic resonance frequency of the resonating element, could also be considerably dependent on other circuit elements (active device, load, power supply, etc..) that are subject to "drift" phenomena or other possible sources of perturbations like the LF noise sources of the active device. For the design of the HSB3 DROs, the simplified stability analysis based on the describing function approach proposed in [2] and [3] has been implemented and automated in suitable simulation linear and nonlinear Harmonic Balance benches: this design flow allows a quantitative evaluation of the stabilizing effect introduced in the oscillator by the resonating element and provides an effective criterion for the optimization of frequency (and amplitude) stability performances.

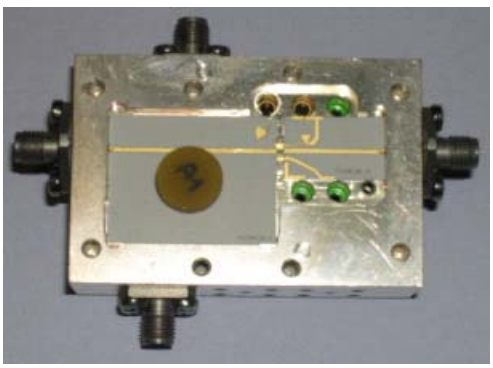

Fig. 4. Photograph of the system: the monolithic die and the alumina microstrip circuits are attached on an aluminum jig. The DR is placed over the microstrip line for a strong coupling.

As shown in figure 4, the system is realized in an aluminum jig with SMA connectors for bias and signal access. The monolithic silicon die, 220µm thick with an area of 992µm by 701µm, is attached with epoxy conductive glue to the jig structure. Two pieces of 25mils tick alumina are attached near the die in the same manner.

The die is wire bonded through many wires to the external part of the system. In figure 5, it is possible to distinguish the wires connecting the output microstrip line (right), the DR-coupled line (left), the external high-impedence bias networks for the collector (upper right) and the emitter (upper left) supply voltages: those networks are implemented with λ/4 high impedence line followed by radial stubs.

As the transistor has got two symmetrical emitter pads, two series capacitors are needed for the negative resistance topology: those capacitors are grounded to two external gold preforms by means of three bonding wires to minimize the series inductance that modifies the emitter reactance designed to synthesize the negative resistance characteristic. The jig is closed with an aluminum top in order to minimize radiation losses and protect the DR from spurious coupling with external signals. A bias tee is connected to the left side SMA connector in order to present at the end of the DR-coupled microstrip line a 50 Ohm termination for the RF signals and a high impedence bias circuit for the base current.

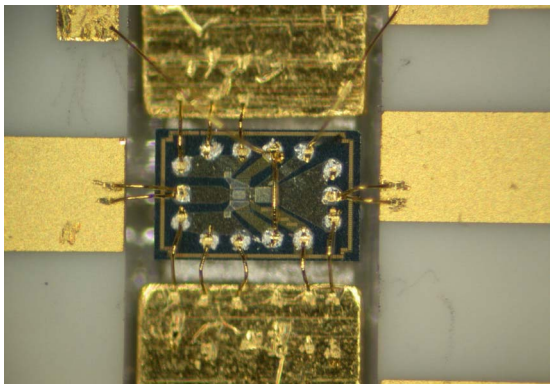

Fig. 5. Photograph of the negative resistance monolithic die attached on the jig bottom surface and wire-bonded to microstrip signal lines, bias lines on alumina substrate and gold preforms for external grounding reference.

V. Performance Measurements

The circuits were tested and measured at the Bologna University Labs. For both of the negative resistance circuits the active device was biased at 150uA base current and 1.8 V_{CE}, that correspond to a 25mA collector current. For the 6GHz oscillator we obtained 6.34 dBm output power with 19dBc suppression of the second harmonic. In the 7.5GHz DRO the fundamental output level is 2.34dBm with a second harmonic suppression of 30dBc. Phase noise measurements were performed with the test jig closed inside aluminum shielding box to prevent from coupling with outside signal noise sources

(Figure 6). The device was battery biased to avoid supply low frequency noise injecting into the circuit.

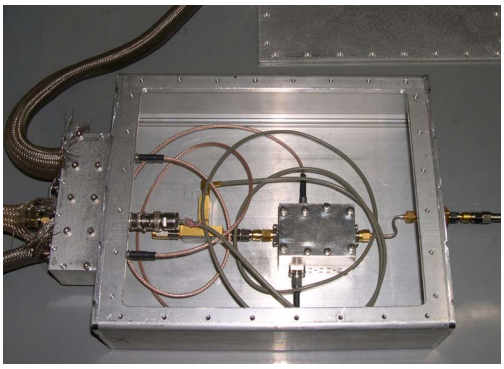

Fig. 6. Measurement setup with the DUT inside a Shieding box.

Phase noise performances obtained are -116dBc/Hz at 10KHz offset from the carrier for the lower frequency oscillator, and -107dBc/Hz at 10KHz from the carrier for the 7.5GHz oscillator. Measured output power (figure 7) and phase noise performances (see figure 8) at 10KHz from the carrier are in good agreement with the simulated ones. In fact referring to the output spectrum of the 7.5 GHz DRO in figure 7, the simulated results were practically identical to the measurements: 2.42dBm Vs 2.34dBm for the fundamentals and -27.1dBm Vs -28dBm for the second harmonics.

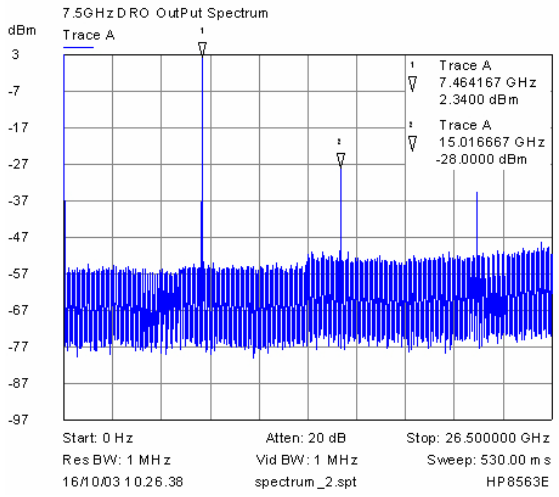

Fig. 7. 7.5GHz DRO Output Spectrum

VI. Conclusions

A 6GHz and a 7.5GHz DR-oscillators have been implemented using a silicon bipolar technology tailored for 1.9GHz high efficiency low-voltage power amplifier design. A nonlinear design technique based on the describing function approach was adopted for the oscillators design. The DROs exhibit phase noise levels of -116dBc/Hz and -107dBc/Hz at 10kHz offset, that are good enough for many space and communication applications.

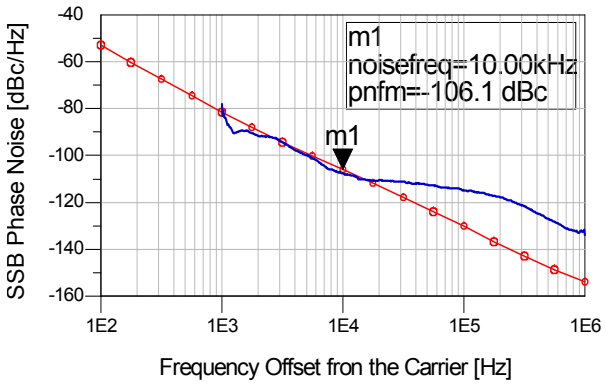

Fig. 8. Phase noise performances: simulations and measurements agree almost perfectly from 1KHz to 10KHz. From 10KHz to 1MHz the measurement is affected by the spectrum analyzer threshold level.

VII. Acknowledgement

The authors wish to acknowledge the assistance and support of SIAE Microelettonica for the modules assembly and ST Microelectronics (Catania site) for providing the devices and foundry support.

This project was founded by MIUR (Italian Ministry of Education, University and Research) under the projects: *"Strutture e metodologie di progettazione per sistemi microelettronici di prossima generazione"* in cooperation with ST microelectronics and *"Non-linear noise models and design of low-phase noise oscillators for high performance communication systems"*

References

[1] M. Regis, O. Llopis, J. Graffeuil, "Nonlinear Modeling And Design Of Bipolar Transistors Ultra-low Phase-noise Dielectric-Resonator Oscillators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 10, pp. 1589-1593, October 1998.

[2] F. Filicori and G. Vannini, "Frequency Stability in Resonator-Stabilized Oscillators," *IEEE Trans.on Circutis and System.,* vol. 37, no. 11, pp. 1440-1444, November 1990.

[3] F. Filicori, V.A. Monaco, G. Vannini, "A Design Method for Parallel Feedback Dielectric Resonator Oscillators," *Proc. Of the 19th European Microwave Conference*, London, England, September 1989.

[4] F. Carrara, A. Scuderi, G. Tontodonato, G.Palmisano, "A Very High Efficiency Silicon Bipolar Transistor," *IEEE Electron devices Meeting 2001. IEDM Technical Digest,* pp. 40.1.1-40.1.4, December 2001.

[5] L.Bary, G. Cibiel, I. Telliez, J. Rayssac, A. Rennane, C. Boulanger, O. Llopis, M. Borgarino, R. Plana, J. Graffeuil, "Low frequency noise characterization and modeling of microwave bipolar devices : application to the design of low phase noise oscillator," *IEEE RFIC Symposium 2002 Digest,* pp.359-362, June 2002.

[6] M. Borgarino, L. Bary, D. Vescovi, R.Menozzi, A. Monroy, M. Laurens, R. Plana, F. Fantini, J. Graffeuil, "The Correlation Resistance for Low-Frequency Noise Compact Modeling of Si/SiGe HBTs"

[7] D. Kajfez and P. Guillon, *Dielectric Resonators*, Artech House, Dedham, MA, 1986.